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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	microprocessor			No	TN-SH7-415A/E	
THEME	Guidance of SH7706 hardware manual correction	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use	4. Change of Mask 5. Change of Production Line		
PRODUCT NAME	SH7706(HD6417706)	Lot No. All	Reference Documents	SH7706 Hardware manual Rev.2.0 ADE-602-235A	Rev. 1.0	Effective Date Manual revise

There is the following correction in SH7706 hardware manual.

1.Errata

Page	Item	Error	Right
184	Explanation of bits 6, 5, 4, and 3 "0101" portions	0101: The row address begins with A10. (TheA10 value is output at A1 when the row address is output. 128M(2M×16bits ×4banks), 64M(1M×16bits×4banks))	0101: The row address begins with A10. (TheA10 value is output at A1 when the row address is output. 128M(2M×16bits×4banks), 64M(2M×8bits×4banks))
11-5	Figure 11.2 WTCNT,WTCSR address	Address: H'FFFFFE84 Address: H'FFFFFE86	Address: H'FFFFFF84 Address: H'FFFFFF86
17-10	17.1.6 Explanation of bits 15	When ASEMDO = 1, these bits are always read as 1 and must only be written with 0.	When ASEMDO = 1, these bits are always read as 1.
18-4	18.3.2 Port C Data Register (PCDR)	PCDR is initialized to H'00 by a power-on reset, after which the general input port function(pullup MOS on) is set as the initial pin function, and the corresponding pin levels are read. It retains its previous value in standby mode and sleep mode, and in a manual reset.	PCDR is initialized to H'00 by a power-on reset.
18-6	18.4.2 Port D Data Register (PDDR)	PDDR is initialized to H'00 by a power-on reset, after which the general input port function(pullup MOS on) is set as the initial pin function, and the corresponding pin levels are read. It retains its previous value in standby mode and sleep mode, and in a manual reset.	PDDR is initialized to H'00 by a power-on reset.

Page	Item	Error	Right
18-7	18.5.2 Port E Data Register (PEDR)	PEDR is initialized to H'00 by a power-on reset, after which the general input port function(pullup MOS on) is set as the initial pin function, and the corresponding pin levels are read. It retains its previous value in standby mode and sleep mode, and in a manual reset.	PEDR is initialized to H'00 by a power-on reset.
18-11	18.8.2 Port H data Register (PHDR)	PHDR is initialized to H'00 by a power-on reset, after which the general input port function(pullup MOS on) is set as the initial pin function, and the corresponding pin levels are read. It retains its previous value in standby mode and sleep mode, and in a manual reset.	PHDR is initialized to H'00 by a power-on reset.
18-12	18.9 Port J	Each pin has an input pullup MOS, which is controlled by Port J Control Register (PJCR) in PFC.	(delete)
24-4	Table 24.4 Note	Note: * The Min value depends on the clock mode used. See table 10.3, Available Combinations of Clock Mode and FRQCR Values.	(delete)
24-31	Figure24.31 Synchronous DRAM Burst Read Bus Cycle (RAS Down, Same Row Address, CAS Latency = 2)		Tnop cycle is deleted. tAD, tCSD3, tRWD, tRASD, tDQMD, and tDAKD1 are specified from the head of Tc1 cycle.

2.List of registers (p.596)

23.3 Register States in Processing Mode (The shaded columns show the change part)

Register Name	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep	Module
PTEH	Undefined	Undefined	Held	Held	Held	CCN
PTEL	Undefined	Undefined	Held	Held	Held	
TTB	Undefined	Undefined	Held	Held	Held	
TEA	Undefined	Undefined	Held	Held	Held	
MMUCR	Initialized *1	Initialized *1	Held	Held	Held	
BASRA	Undefined	Undefined	Held	Held	Held	
BASRB	Undefined	Undefined	Held	Held	Held	
TRA	Undefined	Undefined	Held	Held	Held	
INTEVT	Undefined	Undefined	Held	Held	Held	
BRSR	Initialized *1	Initialized *1	Held	Held	Held	UBC
BRDR	Initialized *1	Initialized *1	Held	Held	Held	
FRQCR	Initialized *2	Held	Held	Held	Held	CPG
WTCNT	Initialized *2	Held	Held	Held	Held	
WTCSR	Initialized *2	Held	Held	Held	Held	
RSECAR	Held *3	Held *3	Held	Held	Held	RTC
RMINAR	Held *3	Held *3	Held	Held	Held	
RHRAR	Held *3	Held *3	Held	Held	Held	
RWKAR	Held *3	Held *3	Held	Held	Held	
RDAYAR	Held *3	Held *3	Held	Held	Held	
RMONAR	Held *3	Held *3	Held	Held	Held	
TCPR_2	Undefined	Undefined	Held	Held	Held	TMU
INTEVT2	Undefined	Undefined	Held	Held	Held	INTC
SAR_0	Undefined	Undefined	Held	Held	Held	DMAC
DAR_0	Undefined	Undefined	Held	Held	Held	
DMATCR_0	Undefined	Undefined	Held	Held	Held	
SAR_1	Undefined	Undefined	Held	Held	Held	
DAR_1	Undefined	Undefined	Held	Held	Held	
DMATCR_1	Undefined	Undefined	Held	Held	Held	
SAR_2	Undefined	Undefined	Held	Held	Held	
DAR_2	Undefined	Undefined	Held	Held	Held	
DMATCR_2	Undefined	Undefined	Held	Held	Held	
SAR_3	Undefined	Undefined	Held	Held	Held	
DAR_3	Undefined	Undefined	Held	Held	Held	
DMATCR_3	Undefined	Undefined	Held	Held	Held	
SDIR *4	Held	Held	Held	Held	Held	UDI

Note *1 Some bits are not initialized.

*2 Not initialized by a power-on reset generated by the WDT.

*3 Some bits are initialized.

*4 Initialized on asserting state of $\overline{\text{TRST}}$ or on Test-Logic-Reset state of TAP.

3. AC Characteristics (p.607)

Table 24.5 Summarize clock timing in one table as follows. (The shaded columns show the change part)

Table 24.5 Clock timing

Item	Symbol	min	max	Unit	Figure
EXTAL clock input frequency(clock mode 0)	f_{EX}	25	66.67	MHz	24.1
EXTAL clock input cycle time(clock mode 0)	t_{EXcyc}	15	40	ns	
EXTAL clock input frequency(clock mode 1)	f_{EX}	6.25	16.67	MHz	
EXTAL clock input cycle time(clock mode 1)	t_{EXcyc}	60	160	ns	
EXTAL clock input low pulse width	t_{EXL}	1.5	—	ns	
EXTAL clock input high pulse width	t_{EXH}	1.5	—	ns	
EXTAL clock input rise time	t_{EXR}	—	6	ns	
EXTAL clock input fall time	t_{EXF}	—	6	ns	
CKIO clock input freqency	f_{CKI}	25	66.67	MHz	24.2
CKIO clock input cycle time	t_{CKIcyc}	15	40	ns	
CKIO clock input low pulse width	t_{CKIL}	1.5	—	ns	
CKIO clock input low pulse width	t_{CKIH}	1.5	—	ns	
CKIO clock input rise time	t_{CKIR}	—	6	ns	
CKIO clock input fall time	t_{CKIF}	—	6	ns	
CKIO clock output freqency	f_{OP}	25	66.67	MHz	24.3
CKIO clock output cycle time	t_{cyc}	15	40	ns	
CKIO clock output low pulse width	t_{CKOL}	3	—	ns	
CKIO clock output high pulse width	t_{CKOH}	3	—	ns	
CKIO clock output rise time	t_{CKOR}	—	5	ns	
CKIO clock output fall time	t_{CKOF}	—	5	ns	
Power-on oscillation settling time	t_{OSC1}	10	—	ms	24.4
$\overline{\text{RESETP}}$ setup time	t_{RESPS}	20	—	ns	24.4, 24.5
$\overline{\text{RESETM}}$ setup time	t_{RESMS}	0	—	ns	
$\overline{\text{RESETP}}$ assert time	t_{RESPW}	20	—	t_{cyc}	
$\overline{\text{RESETM}}$ assert time	t_{RESMW}	20	—	t_{cyc}	
Standby return oscillation settling time1	t_{OSC2}	10	—	ms	24.5
Standby return oscillation settling time2	t_{OSC3}	10	—	ms	24.6
Standby return oscillation settling time3	t_{OSC4}	11	—	ms	24.7
PLL synchronization settling time 1 (at the releas from standby mode)	t_{PLL1}	100	—	ìs	24.8, 24.9
PLL synchronization settling time 1 (at the modification of multiplication rate)	t_{PLL2}	100	—	ìs	24.10
IRQ/IRL interruput determination time (RTC is used in the standby mode)	t_{IRLSTB}	100	—	ìs	24.10