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Product Category	MPU/MCU		Document No.	TN-RX-A034A/E	Rev.	1.00
Title	Errata to RX210 Group User's Manual regarding Timing of On-Chip Peripheral Modules		Information Category	Technical Notification		
Applicable Product	RX210 Group	Lot No. All	Reference Document	RX210 Group User's Manual: Hardware Rev.1.10 (R01UH0037EJ0110)		

This document describes corrections to the RX210 Group User's Manual: Hardware Rev.1.10.

The corrections are indicated in red in the list below.

[Corrections]

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The characteristics in the SCI module in Table 41.35 Timing of On-Chip Peripheral Modules (1) are corrected as follows.

Table 41.35 Timing of On-Chip Peripheral Modules (1)
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, Ta = –40 to +105°C
High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	—	t_{Pcyc}	Figure 41.38
		Clock synchronous			6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	16	—	t_{Pcyc}	C = 30 pF Figure 41.39
		Clock synchronous			4	—		
	Output clock pulse width		2.7 V ≤ VCC ≤ 5.5 V	t_{SCKW}	0.4	0.6	t_{Scyc}	
			1.8 V ≤ VCC < 2.7 V		0.4→0.35	0.6→0.65		
			1.62 V ≤ VCC < 1.8 V		0.4→0.35	0.6→0.65		
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	40→65		
			1.8 V ≤ VCC < 2.7 V		—	40→85		
			1.62 V ≤ VCC < 1.8 V		—	40→95		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	40→65	—	ns	
			1.8 V ≤ VCC < 2.7 V		40→75	—		
			1.62 V ≤ VCC < 1.8 V		40→80	—		
	Receive data setup time (slave)	Clock synchronous			40	—		
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

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The characteristics in the RSPI module in Table 41.36 Timing of On-Chip Peripheral Modules (2) are corrected as follows.

Table 41.36 Timing of On-Chip Peripheral Modules (2) (1/2)
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, Ta = –40 to +105°C
High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	4	4096	t_{Pcyc}	C = 30 pF Figure 41.41
		Slave			8	4096		
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ → $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ → $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	10→15		
			1.62 V ≤ VCC < 1.8 V		—	10→20		
		Input			—	1	μs	

Table 41.36 Timing of On-Chip Peripheral Modules (2) (2/2)

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	15→50	—	ns	C = 30 pF Figure 41.42 to Figure 41.45
			1.8 V ≤ VCC < 2.7 V		20→65	—		
			1.62 V ≤ VCC < 1.8 V		20→75	—		
		Slave			20 – t_{Pcyc} → 25 – t_{Pcyc}	—		
	Data input hold time	Master		t_H	0 → t_{Pcyc}	—	ns	
		Slave			20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	86→50	ns	
			1.8 V ≤ VCC < 2.7 V		—	86→55		
			1.62 V ≤ VCC < 1.8 V		—	86→60		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 40 → 3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V			3 × t_{Pcyc} + 40 → 3 × t_{Pcyc} + 85		
			1.62 V ≤ VCC < 1.8 V			3 × t_{Pcyc} + 40 → 3 × t_{Pcyc} + 95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/ fall time	Output		t_{Dr}, t_{Df}	—	20	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	4→6	t_{Pcyc}	C = 30 pF Figure 41.44 and Figure 41.45
			1.8 V ≤ VCC < 2.7 V		—	4→7		
			1.62 V ≤ VCC < 1.8 V		—	4→7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	3→5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	3→6		
			1.62 V ≤ VCC < 1.8 V		—	3→6		

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The characteristics in the Simple SPI module in Table 41.37 Timing of On-Chip Peripheral Modules (3) are corrected as follows.

Table 41.37 Timing of On-Chip Peripheral Modules (3)
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = – 40 to +105°C
High drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 41.41
	SCK clock cycle input (slave)			8→6	65536		
	SCK input clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK input clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK output clock high pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.4→0.35	0.6→0.65		
		1.62 V ≤ VCC < 1.8 V		0.4→0.35	0.6→0.65		
	SCK output clock low pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.4→0.35	0.6→0.65		
		1.62 V ≤ VCC < 1.8 V		0.4→0.35	0.6→0.65		
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	40→65	—	ns	C = 30 pF Figure 41.42 and Figure 41.43 → Figure 41.42 to Figure 41.45
		1.8 V ≤ VCC < 2.7 V		40→75	—		
		1.62 V ≤ VCC < 1.8 V		40→80	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V ≤ VCC ≤ 5.5 V		—	40→65		
		1.8 V ≤ VCC < 2.7 V		—	40→85		
		1.62 V ≤ VCC < 1.8 V		—	40→95		
	Data output hold time		t_{OH}	–10	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	5→6	t_{Pcyc}	C = 30 pF Figure 41.44 and Figure 41.45
	Slave output release time		t_{REL}	—	5→6	t_{Pcyc}	