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RENESAS TECHNICAL UPDATE

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Title	Errata to RX210 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX210 Group	Lot No. All	Reference Document	RX210 Group User's Manual: Hardware Rev.1.10 (R01UH0037EJ0110)		

This document describes corrections to RX210 Group User's Manual: Hardware Rev.1.10.

The changes are indicated in red in the list below.

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  The voltage regulator control register (VRCR) is added to Table 5.1 as follows:

Corrections

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK	Reference Section
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8	3ICLK		section 8., section 35
0008 0200h	SYSTEM	Voltage regulator control register	VRCR	8	8	3ICLK		section 9
0008 03FEh	SYSTEM	Protect register	PRCR	16	16	3ICLK		section 12

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The numbers of access states of interrupt source priority register 000 to interrupt source priority register 249 (IPR000 to IPR249) and port input data registers (PIDR) in Table 5.1 are corrected as follows:

Before correction

Module Symbol	Register Name	Register Symbol	Number of Access States	
			ICLK ≥ PCLK	ICLK < PCLK
ICU	Interrupt source priority register 000	IPR000	3 ICLK for reading, 2 ICLK for writing	
:	:	:	:	
ICU	Interrupt source priority register 249	IPR249	3 ICLK for reading, 2 ICLK for writing	
PORT0	Port input data register	PIDR	2, 3PCLKB	2ICLK
:	:	:	:	:
PORTJ	Port input data register	PIDR	2, 3PCLKB	2ICLK

Corrections

Module Symbol	Register Name	Register Symbol	Number of Access Cycles	
			ICLK ≥ PCLK	ICLK < PCLK
ICU	Interrupt source priority register 000	IPR000	2ICLK	
:	:	:	:	
ICU	Interrupt source priority register 249	IPR249	2ICLK	
PORT0	Port input data register	PIDR	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
:	:	:	:	:
PORTJ	Port input data register	PIDR	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

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The description in 9.2.2 System Clock Control Register 3 (SCKCR3) is corrected as follows:

Before correction

When changing the source of the system clock while the CPU is running on the low-speed on-chip oscillator after a reset, be sure to write 00h to address 0008 0200h before writing any setting data to this register.

[Write procedure]

(1) Enabling writing to the registers associated with the PRCR.PRC2 bit

Write A504h to the protect register (PRCR).

(2) Writing 00h to address 0008 0200h

(3) Disabling writing to the registers associated with the PROCR.PRC2 bit

Write A500h to the protect register (PRCR).

Corrections

When changing the source of the system clock while the CPU is running on the low-speed on-chip oscillator after a reset, be sure to write 00h to VRCR register before writing any setting data to this register.

[Write procedure]

(1) Enabling writing to the registers associated with the PRCR.PRC2 bit

Write A504h to the protect register (PRCR).

(2) Writing 00h to VRCR register.

(3) Disabling writing to the registers associated with the PRCR.PRC2 bit

Write A500h to the protect register (PRCR).

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9.2.3 “Voltage Regulator Control Register (VRCR)” is added as follows:

9.2.3 Voltage Regulator Control Register (VRCR)

Address(es) 0008 0200h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

VRCR is an 8-bit readable and writable register. After the reset state is released, write 00h to this register before changing the clock source of the system clock.

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9.2.14 “Main Clock Oscillator Forced Oscillation Control Register (MOFCR)” is corrected as follows:

Corrections

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3 to b1	MODRV[2:0]	Main Clock Oscillator Drive Capability Switch	b3 b1 0 0 0: 16-MHz to 20-MHz non-lead type ceramic resonator 1 1 1: 16-MHz to 20-MHz lead type ceramic resonator Settings other than the above are prohibited.	R/W
b5, b4	MODRV2[1:0]	Main Clock Oscillator Drive Capability Switch 2	b5 b4 0 1: 1 MHz to 8 MHz 1 0: 8.1 MHz to 15.9 MHz 1 1: 16 MHz to 20 MHz Settings other than the above are prohibited.	R/W
b6	MOSEL	Main Clock Oscillator Switch	0: Resonator 1: External oscillator input	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

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The second note in 9.8.5 is corrected as follows:

Before correction

The SOSCCR.SOSTP bit should be used to set the sub-clock as the system clock; and the RCR3.RTCEN bit should be used to set the sub-clock as the realtime clock count source.

Corrections

To use the sub-clock as the system clock and as the count source for the realtime clock simultaneously, after the sub-clock starts oscillating and the oscillation stabilization wait time has elapsed, the SOSCWTCR.SSTS[4:0] bits must be set to 00000b. To set these bits, perform the initial setting procedure below. After setting the SSTS[4:0] bits, perform the clock setting procedure shown in section 25.3.2.

Initial setting procedure

(1) Wait for the oscillation stabilization wait time of the sub-clock[*1] to elapse.
(2) Set the SOSCCR.SOSTP bit to 1.
(3) Read the SOSCCR.SOSTP bit and confirm that it is 1.
(4) Set the RCR3.RTCEN bit to 0.
(5) Read the RCR3.RTCEN bit and confirm that it is 0.
(6) Wait for at least five cycles of the sub-clock to elapse.
(7) Set the RCR3.RTCDV[2:0] bits.
If the RCR3.RTCDV[2:0] bits are set in this step, they do not need to be reset in section 25.3.2, Clock Setting Procedure.
(8) Set the SOSCWTCR.SSTS[4:0] bits to specify the wait time necessary for sub-clock oscillation.
(9) Set the SOSCCR.SOSTP bit to 0 (sub-clock oscillator is operating).
(10) Wait for the oscillation stabilization wait time of the sub-clock[*1] to elapse.
(11) Read the SOSCCR.SOSTP bit and confirm that it has been rewritten to 0, then set the RCR3.RTCEN bit to 1 (sub-clock oscillator is operating).
(12) Read the RCR3.RTCEN bit and confirm that it has been rewritten to 1, then set the SOSCCR.SOSTP bit to 1.
(13) Read the SOSCCR.SOSTP bit and confirm that it has been rewritten to 1, then wait for at least five cycles of the sub-clock to elapse.
(14) Set the SOSCWTCR.SSTS[4:0] bits to 00000b.
(15) Set the SOSCCR.SOSTP bit to 0.
(16) Wait for at least two cycles of the sub-clock to elapse.
(17) Read the SOSCCR.SOSTP bit and confirm that it has been rewritten.

Note 1. For details on the oscillation stabilization wait time of the sub-clock, see section 11.2.8, Sub-Clock Oscillator Wait Control Register (SOSCWTCR).

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The note below is added to 9.8.5.

Corrections

- The RCR3.RTCDV[2:0] bits must also be set when operating the sub-clock oscillator. Set these bits while the sub-clock oscillator is stopped. Do not rewrite these bits while the sub-clock oscillator is operating.

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Corrections

The description in 11.2.18 “Flash HOCO Software Standby Control Register (FHSSBYCR)” is corrected as follows:

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SOFTCUT[2:0]	Software Cut 0	[Chip versions A and C] b2 b0 1 1 0: Power is supplied to flash memory but not supplied to HOCO in software standby mode. The voltage detection circuit (LVD) is stopped and the low power consumption function by the power-on reset circuit (POR) is enabled.	R/W

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The procedure examples for switching modes in 11.5.1 are corrected as follows:

Before correction

(1) Switching from Normal Power Consumption Mode to Low Power Consumption Mode
Example: From middle-speed operating mode 1A to low-speed operation mode 1
(High-speed operation in the operating power consumption control mode used before mode-switching)
↓
Set to switch from the HOCO clock to the LOCO clock (clock source and frequency division ratio)
↓
Write to OPCCR
↓
(Low-speed operation in the switched operating power consumption control mode)

(2) Switching from Low Power Consumption Mode to Normal Power Consumption Mode
Example: From low-speed operation mode 2 to middle-speed operation mode
(Low-speed operation in the operating power consumption control mode used before mode-switching)
↓
Write to OPCCR
↓
Set to switch from the LOCO clock to the HOCO clock (clock source and frequency division ratio)
↓
(High-speed operation in the switched operating power consumption control mode)

Corrections

(1) Switching from Normal Power Consumption Mode to Low Power Consumption Mode
Example: From high-speed operating mode to low-speed operation mode 1
(High-speed operation in the operating power consumption control mode used before mode-switching)
↓
Set to switch from the HOCO clock to the LOCO clock (clock source and frequency division ratio)
↓
Write to OPCCR
↓
Confirm that the OPCCR.OPCMTSF flag is 0
↓
(Low-speed operation in the switched operating power consumption control mode)

(2) Switching from Low Power Consumption Mode to Normal Power Consumption Mode
Example: From low-speed operation mode 2 to high-speed operating mode
(Low-speed operation in the operating power consumption control mode used before mode-switching)
↓
Write to OPCCR
↓
Confirm that the OPCCR.OPCMTSF flag is 0
↓
Set to switch from the LOCO clock to the HOCO clock (clock source and frequency division ratio)
↓
(High-speed operation in the switched operating power consumption control mode)

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The description in 19.3.7 Pull-Up Control Register (PCR) is corrected as follows:

Before correction

While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.

PCR retains pull-up state even when a transition to deep software standby mode is made.

When a pin is set as an external bus pin, a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR.

Corrections

While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.

PCR retains pull-up state even when a transition to deep software standby mode is made.

When a pin is used as an external bus pin other than the WAIT# pin, a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of the PCR register.

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The description for general I/O ports in Table 19.3 is corrected as follows:

Before correction

Pin Name	Description
Port 0 to 5 Port A to E, H, J	Connect these pins to Vcc via a pull-up resistor or to Vss via a pull-down resistor.

Corrections

Pin Name	Description
Port 0 to 5 Port A to E, H, J	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2

Note 1. Clear the PORTn.PMR bit, the PmnPFS.ISEL bit and the PmnPFS.ASEL bit to 0.

Note 2. In the case of release when the setting is for output, the port is an input over the period from release from the reset state to the pin becoming an output. Since the voltage on the pin is undefined while it is an input, this may lead to an increase in the current drawn.

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21.6.24 “Point for Caution Regarding MTU5.TCNT and MTU5.TGR Registers” is added as follows:

Corrections

21.6.24 Point for Caution Regarding MTU5.TCNT and MTU5.TGR Registers

Do not set an MTU5.TGRm (m = U, V, W) bit to the value of the corresponding MTU5.TCNTm (m = U, V, W) register plus one while counting by the MTU5.TCNTm (m = U, V, W) register is stopped. If an MTU5.TGRm (m = U, V, W) bit is set to the value of the corresponding MTU5.TCNTm (m = U, V, W) register plus one while counting by the MTU5.TCNTm (m = U, V, W) register is stopped, a compare-match will be generated even though counting is stopped.

In this case, if the corresponding MTU5.TIER.TGIE5m (m = U, V, W) bit is also set to 1 (enabling interrupts), a compare-match interrupt will also be generated. If the value of the timer compare match clear register is also 1 (enabled), the timer is automatically cleared to 0000h when the compare-match is generated, regardless of whether interrupts from the MTU5.TCNTm (m = U, V, W) are enabled or disabled.

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The description about counter clear is corrected in Table 23.2 as follows:

Before correction

Item	Unit 0			Unit 1		
Counter mode	8 Bits		16 Bits	8 Bits		16 Bits
Channel	TMR0	TMR1	TMR0+TMR1	TMR2	TMR3	TMR2+TMR3
Counter clear	TMR0.TCORA TMR0.TCORAB TMRI0	TMR0.TCORA TMR0.TCORAB TMRI1	TMR0.TCORA+ TMR1.TCORA TMR0.TCORB+ TMR1.TCORB TMRI0	TMR2.TCORA TMR2.TCORAB TMRI2	TMR3.TCORA TMR3.TCORAB TMRI1	TMR2.TCORA+ TMR3.TCORA TMR2.TCORB+ TMR3.TCORB TMRI0

Corrections

Item	Unit 0			Unit 1		
Counter mode	8 Bits		16 Bits	8 Bits		16 Bits
Channel	TMR0	TMR1	TMR0+TMR1	TMR2	TMR3	TMR2+TMR3
Counter clear	TMR0.TCORA TMR0.TCORB TMRI0	TMR1.TCORA TMR1.TCORB TMRI1	TMR0.TCORA+ TMR1.TCORA TMR0.TCORB+ TMR1.TCORB TMRI0	TMR2.TCORA TMR2.TCORB TMRI2	TMR3.TCORA TMR3.TCORB TMRI3	TMR2.TCORA+ TMR3.TCORA TMR2.TCORB+ TMR3.TCORB TMRI2

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The description about the RTCDV[2:0] bits in 25.2.19 RTC Control Register 3 (RCR3) is corrected as follows:

Before correction

RTCDV[2:0] Bits (Sub-clock Oscillator Drive Ability Control)

It must be noted that the oscillation accuracy of the sub-clock oscillator is affected if the RTCDV[2:0] bits are set to 001b (low CL drive power) with an on-chip debugging emulator is attached. The oscillation accuracy is not affected when the RCR3.RTCDV[2:0] bits are set to 110b (standard CL drive power).

Corrections

RTCDV[2:0] Bits (Sub-clock Oscillator Drive Ability Control)

These bits control the drive ability of the sub-clock oscillator. When connecting a standard CL crystal unit, set these bits to 110b (drive ability for standard CL). When connecting a low CL crystal unit, set these bits to 001b (drive ability for low CL). Set the RTCDV[2:0] bits while the SOSCCR.SOSTP bit is 1 and the RCR3.RTCEN bit is 0.

(1) Notes on using a low CL crystal unit

When the RCR3.RTCDV[2:0] bits are 001b (drive ability for low CL), the oscillator is susceptible to noise. Especially when the signal level of any pin near the XCIN or XCOUT pin is changed, the oscillation accuracy of the sub-clock oscillator may be affected. The accuracy is affected differently depending on the board traces and how the signal level of any pin near the XCIN or XCOUT pin is changed. When designing a board using a low CL crystal unit, refer to the application note “Design Guide for Low CL Sub-clock Circuits” (R01AN1187EJ) to reduce the influence from the noise.

The following are examples that may significantly affect oscillation accuracy:

- When connecting an on-chip debugging emulator to the FINED pin

  Since the FINED pin (FINE interface pin) is near the XCIN and XCOUT pins, the oscillation accuracy of the sub-clock oscillator is affected when using the FINED pin during debugging. When using the FINED pin during debugging, keep using the low CL crystal unit and set the RCR3.RTCDV[2:0] bits to 110b (drive ability for standard CL). However, this measure may affect the reliability of the crystal unit. Therefore, use this measure only when using an on-chip debugging emulator. Set the RCR3.RTCDV[2:0] bits to 001b (drive ability for low CL) in mass production programs.
- When supplying an external clock to the main clock oscillator

  When inputting an external clock to the EXTAL pin, the oscillation accuracy of the sub-clock oscillator may be affected.

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Note 2 of the register table in (1) Serial Communications Interface Mode (SMIF in SCMR = 0) in 28.2.6 “Serial Control Register (SCR)” is corrected as follows:

Before correction

Note 2. A 1 can be written only when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written in TE and RE. While the SMR.CM bit is 0, writing is enabled under any condition.

Corrections

Note 2. A 1 can be written only when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written in TE and RE. While the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.

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The clearing condition of TEND flag (Transmission End Flag) in 28.2.7 serial status register (SSR) is corrected as follows:

Before correction

[Clearing condition]

- When data for transmission are written to the TDR while the SCR.TE is 1

When the TEND flag is cleared by writing the data for transmission to the TDR, read the TEND flag and check that it has actually been cleared to 0.

Corrections

[Clearing condition]

When data for transmission are written to the TDR while the SCR.TE is 1

When the TEND flag is cleared by writing transmit data to the TDR register, perform a dummy read of the SSR register in the following order:

(1) Write transmit data to the TDR register.

(2) Read the SSR register and write that value to a general register.

(3) Execute some operations using the read value.

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The description of [4] in Figure 28.10 is corrected as follows:

Before correction

[4] Break output at the end of serial transmission:

To output a break in serial transmission, set the I/O port function corresponding to the TXDn pin to 0 (low level output), and then clear the SCR.TE bit to 0.

Corrections

[4] To output a break in serial transmission, set the I/O port that shares a pin with the TXDn pin to “low output”, and switch from the TXDn pin to the general I/O port before setting the TE bit in the SCR register to 0.

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The description in 28.8.3 is corrected as follows:

Before correction

If the SSn# pin input changes from low to high during transmission or reception, the operation is continued at the clock input through the SCKn pin until the transmission or reception is completed. Input of the clock signal from the SCKn pin is ignored until the input on the SSn# pin subsequently changes from the high to the low level.

Corrections

If the input on the SSn# pin changes from low to high level during transmission or reception, the SMISOn output pin will be placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception will continue at the rate of the clock input through the SCKn pin until processing for the character currently being transmitted or received is completed, after which it stops. At that time, an interrupt (the appropriate one from among TXI, RXI, and TEI) will be generated.

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The description in 28.13.3 is corrected as follows:

Before correction

When the SCR.TE bit is 0 (prohibiting serial transmission), setting the I/O port function makes selection of the level and direction (input or output) of the TXDn pin possible. If this is done, the TXDn pin can be placed in the mark state to send a break at the time of data transmission. Until the SCR.TE bit is set to 1 (permitting serial transmission), the I/O port function is used to set the TXDn pin to output 1 and thus place the transfer circuit in the mark state (state of having the value 1). On the one hand, if a break is to be output at the time of data transmission, the SCR.TE bit is cleared to 0 after the I/O port function settings are used to set up output of a 0 on the TXDn pin. When the SCR.TE bit is cleared to 0, the transmission section is initialized without connection to the current state of transmission, the TXDn pin becomes an I/O port pin, and the output from the TXDn pin changes to 0 or 1 in accord with the settings for the I/O port function.

Corrections

When the SCR.TE bit is 0 (prohibiting serial transmission), setting the I/O port function makes selection of the level and direction (input or output) of the TXDn pin possible. If this is done, the TXDn pin can be placed in the mark state to send a break at the time of data transmission. Until the SCR.TE bit is set to 1 (permitting serial transmission), the I/O port function is used to set the TXDn pin to output 1 and set the pin mode to a general I/O port pin, and thus place the transfer circuit in the mark state (state of having the value 1). On the other hand, to output a break at the time of data transmission, set the TXDn pin to output 0 and make the pin mode settings for a general I/O port pin. When the SCR.TE bit is set to 0, the transmission section is initialized regardless of the current state of transmission.

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The description in the first paragraph of (1) in 28.13.9 is corrected as follows:

Before correction

Before specifying the module stop state or making a transition to software standby mode, stop the transmit operations (TIE = TE = TEIE = 0 in SCR). TSR, TDR, and SSR are reset by clearing the TE bit. The states of the output pins in the module stop state or in software standby mode depend on the port settings, and the output pins are held high after cancellation. If the transition is made during data transmission, the data being transmitted will be undefined.

Corrections

When making settings for the module-stopped state or in transitions to software standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR to 0) after switching the TXDn pin to the general I/O port pin function. Clearing the TE bit to 0 resets the TSR and the TEND bit in the SSR. The states of output pins in the module stop state and software standby mode depend on the port settings. After exiting the module stop state and software standby mode, output pins become high. When transitions to these states are made during transmission, the data being transmitted become indeterminate.

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Before correction

Step [2] is added to Figure 28.69 as follows:

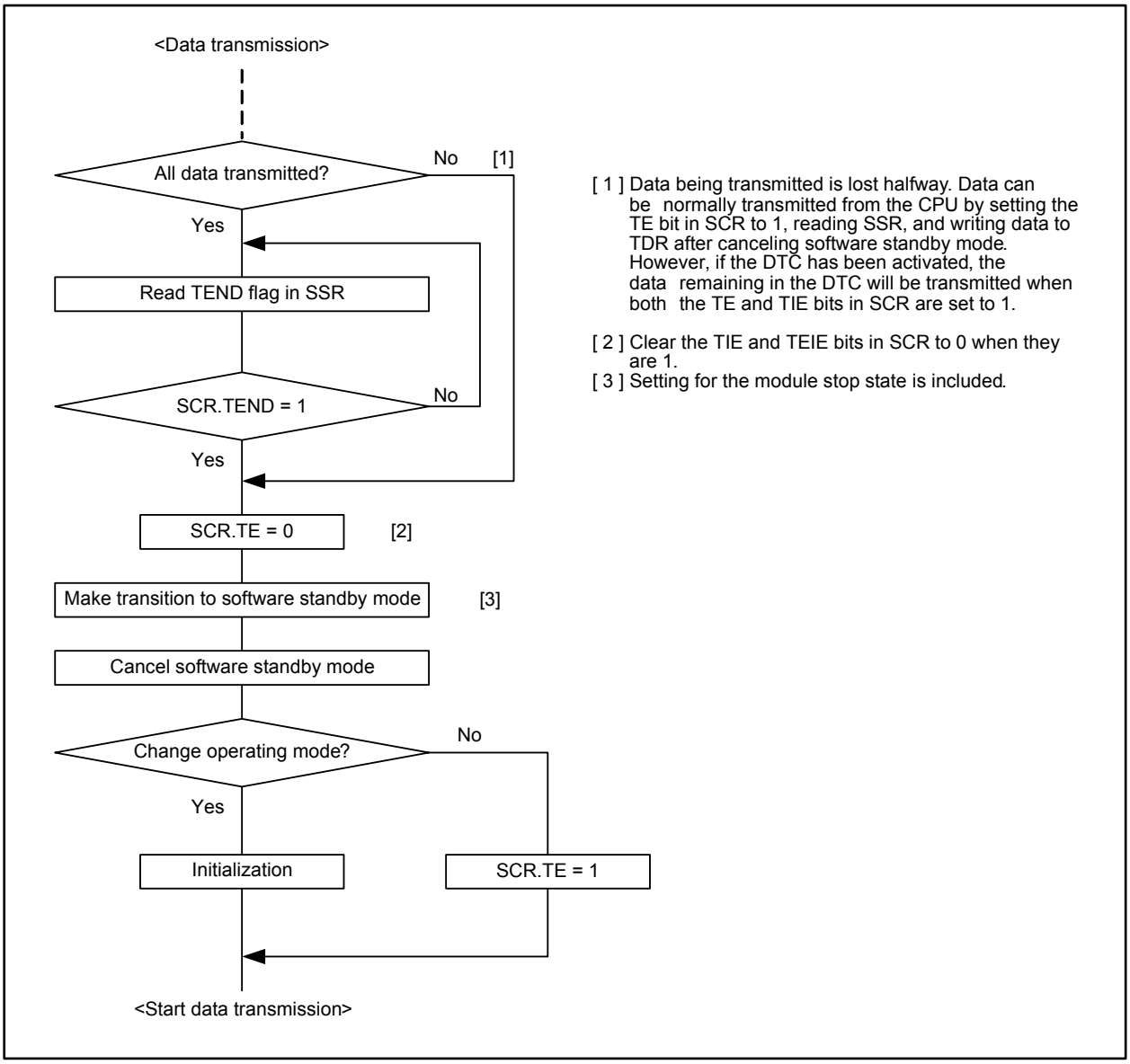

Figure 28.69 Example of Flowchart for Transition to Software Standby Mode during Transmission

Corrections

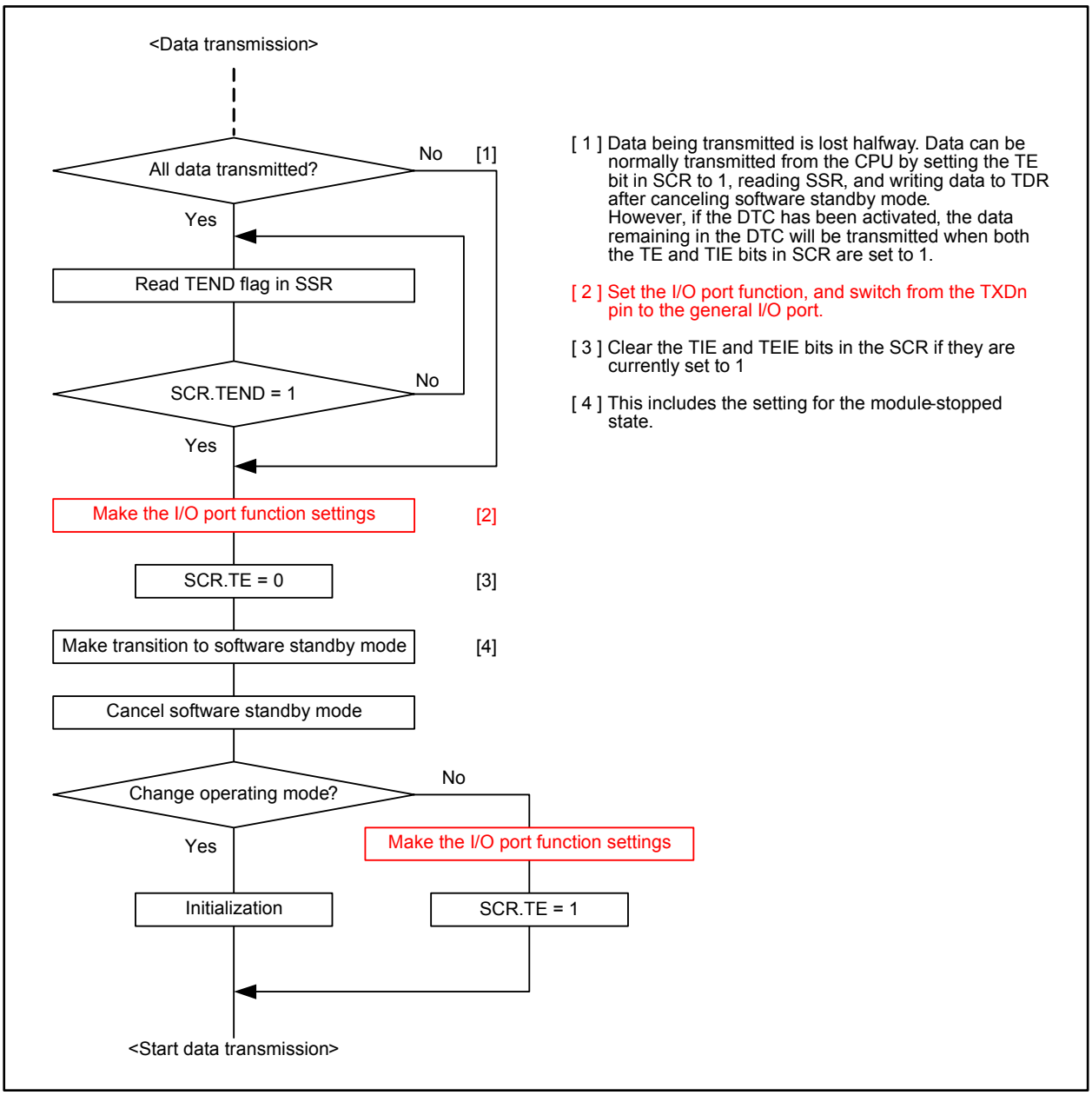

Figure 28.69 Example of Flowchart for Transition to Software Standby Mode during Transmission