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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0234A/E	Rev.	1.00
Title	Errata to the RX113 Group User's Manual: Hardware Rev.1.10		Information Category	Technical Notification		
Applicable Product	RX113 Group	Lot No. All	Reference Document	RX113 Group User's Manual: Hardware Rev.1.10 (R01UH0448EJ0110) Technical Update TN-RX*-A180A/E		

This document describes deletion of specifications from, related modifications to, and errata in the RX113 Group User's Manual: Hardware Rev.1.10.

<Changes to Specifications>

The specifications regarding the general input port PH7 are deleted due to the restriction announced in the technical update: TN-RX*-A180A/E.
The corresponding corrections to the manual are as follows.

Page	Item	Contents
45	Table 1.1 (2/3)	The number of the input ports is changed from 2/2 to 1/1. For details, see next page.
54	Table 1.4 (4/4)	The PH7 pin is deleted from the list of pin functions.
55	Figure 1.3	"PH7/XCIN" on pin number 18 is changed to "XCIN".
56	Figure 1.4	"PH7/XCIN" on pin number G1 is changed to "XCIN".
57	Figure 1.5	"PH7/XCIN" on pin number 9 is changed to "XCIN".
58	Table 1.5 (1/3)	"PH7" on pin number 18 is deleted.
62	Table 1.6 (2/3)	"PH7" on pin number G1 is deleted.
64	Table 1.7 (1/2)	"PH7" on pin number 9 is deleted.
186	9.4.2	Descriptions regarding use as a general port PH7 are deleted.
345	Table 18.1	The row for "PORTH" is deleted.
346	Table 18.2	The row for "PORTH" is deleted.
354	Figure 18.8	The figure for "Port H: PH7" is deleted.
358	18.3.3	The descriptions for the PH7 are deleted.
365	Table 18.5	The descriptions for the PH7 are deleted. For details, see page 3.
1403	Table 43.3	"port PH7" is deleted.
1404	Table 43.4	"port PH7" is deleted.
1404	Table 43.5	"port PH7" is deleted.
1404	Table 43.6	"port PH7" is deleted.
1474	Table 1.1 (2/2)	The row for "PH7" is deleted.

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The numbers of the input ports, pull-up resistors, and open-drain outputs described in Table 1.1, Outline of Specifications (2/3) are changed as follows.

Before correction

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	100-pin /64-pin • I/O: 82/46 • Input: 2/2 • Pull-up resistors: 69/38 • Open-drain outputs: 61/34 • 5-V tolerance: 4/4
		(Omitted)

After correction

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	100-pin/64-pin • I/O: 82/46 • Input: 1/1 • Pull-up resistors: 71/41 • Open-drain outputs: 60/34 • 5-V tolerance: 4/4
		(Omitted)

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The statement regarding PH7 in section 9.4.2, Handling of Pins When Sub-Clock is Not Used is deleted as follows.

Before correction

When the sub-clock is not used, set the SOSCCR.SOSTP bit to 1 (stopped) and set the RCR3.RTCEN bit to 0 (sub-clock oscillator is stopped) (set general port PH7). When this pin is not also used as port PH7, handle it as an unused pin. For handling of unused pins, refer to section 18.5, Handling of Unused Pins.

After correction

When the sub-clock is not to be used, set the SOSCCR.SOSTP bit to 1 (sub-clock oscillator is stopped), set the RCR3.RTCEN bit to 0 (sub-clock oscillator is stopped), leave the XCOUT pin open-circuit, and connect the XCIN pin to VCC or VSS via a resistor.

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The statements regarding PH7 in Table 18.5, Handling of Unused Pins are deleted as follows.

Before correction

Table 18.5 Handling of Unused Pins

Pin Name	Description
	(Omitted)
PH7/XCIN	When the sub-clock is not used, set the RCR3.RTCEN bit to 0 and the SOSCCR.SOSTP bit to 1 (general port PH7). When this pin is not also used as port PH7, handle it in the same way as the input setting of ports 0 to 3, 5, A to F, H, J (PJ0, PJ2, PJ3).
XCOUT	Leave this pin open.
Ports 0 to 3, 5, A to F, H, J (PJ0, PJ2, PJ3)	• Set these pins to input (PORTn.PDR bit = 0) and connect each of them to VCC via a pull-up resistor or to VSS via a pull-down resistor. *1 • Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2
Ports 4, 9, J (PJ6, PJ7)	• Set these pins to input (PORTn.PDR bit = 0) and connect each of them to AVCC0 via a pull-up resistor or to AVSS0 via a pull-down resistor.*1 • Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2
Ports 0 to 5, 9, A to F, H, J (PJ3) (for pins that do not exist on products with fewer than 64 pins)	Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2 (Refer to section 18.4, Initialization of the Port Direction Register (PDR))
	(Omitted)

After correction

Table 18.5 Handling of Unused Pins

Pin Name	Description
	(Omitted)
XCIN	When the sub-clock is not used, set the RCR3.RTCEN bit to 0 and the SOSCCR.SOSTP bit to 1 (sub-clock oscillator is stopped), and then connect this pin to VCC via a pull-up resistor or to VSS via a pull-down resistor.
XCOUT	Leave this pin open.
Ports 0 to 3, 5, A to F, J (PJ0, PJ2, PJ3)	• Set these pins to input (PORTn.PDR bit = 0) and connect each of them to VCC via a pull-up resistor or to VSS via a pull-down resistor.*1 • Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2
Ports 4, 9, J (PJ6, PJ7)	• Set these pins to input (PORTn.PDR bit = 0) and connect each of them to AVCC0 via a pull-up resistor or to AVSS0 via a pull-down resistor.*1 • Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2
Ports 0 to 5, 9, A to F, J (PJ3) (for pins that do not exist on products with fewer than 64 pins)	Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open.*1, *2 (Refer to section 18.4, Initialization of the Port Direction Register (PDR))
	(Omitted)

<Errata>

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The statement of signals assigned to pin number 50 in Table 1.5, List of Pins and Pin Functions (100-Pin LFQFP) is corrected as follows.

Before correction

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
50		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
(Omitted)						

After correction

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	COM3	
(Omitted)						

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The statement of signals assigned to pin number J10 in Table 1.6, List of Pins and Pin Functions (100-Pin TFLGA) is corrected as follows.

Before correction

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
J10		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
(Omitted)						

After correction

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
J10		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	COM3	
(Omitted)						

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The statements of signals assigned to pin numbers 34, 39, and 51 in Table 1.7, List of Pins and Pin Functions (64-Pin LFQFP) are corrected as follows.

Before correction

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
34		PB6/ PC0	MTIOC3D	RXD9/SMOSI9/SSCL9/SSIRXD0	SEG12/ COM5	
(Omitted)						
39		PB0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA/RXD6/SMOSI6/ SSCL6		IRQ2/ADTRG0#
(Omitted)						
51		PE0	MTIOC2A/POE3#	SCK12/CTS9#/RTS9#/SS6#/ SSISCK0	SEG32	IRQ0/AN008
(Omitted)						

After correction

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
(Omitted)						
34		PB6/ PC0	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
(Omitted)						
39		PB0	MTIC5W/MTIOC0C/ RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/ SSCL6		IRQ2/ADTRG0#
(Omitted)						
51		PE0	MTIOC2A/POE3#	SCK12/CTS9#/RTS9#/SS9#/ SSISCK0	SEG32	IRQ0/AN008
(Omitted)						

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"Boot mode (FINE interface)" is added to Table 3.1, Selection of Operating Modes by the Mode Setting Pin as follows.

Before correction

Table 3.1 Selection of Operating Modes by the Mode Setting Pin

Mode Setting Pin		Operating Mode
MD *1	UB#	
Low	Low	Boot mode (USB interface)
Low	High or open	Boot mode (SCI)
High	—	Single-chip mode

Note 1. Do not change the level on the MD pin while the MCU is operating.

After correction

Table 3.1 Selection of Operating Modes by the Mode Setting Pin

Mode Setting Pin		Operating Mode
MD*1	UB#	
Low	Low	Boot mode (USB interface)
Low	High or open	Boot mode (SCI)
High	—	Single-chip mode
Low → High*2	High or open	Boot mode (FINE interface)

Note 1. Do not change the level on the MD pin while the MCU is operating.
Note 2. After release from the reset state while the MD pin is at the low level, switch it to the high level within 20 to 100 ms.

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The following section 3.3.2.3, Boot Mode (FINE Interface) is added to section 3.3.2, Boot Mode.

3.3.2.3 Boot Mode (FINE Interface)

In this mode, the flash memory modifying program (boot program) stored in a dedicated area within the MCU operates. The on-chip ROM (code flash memory and data flash memory) can be modified from outside the MCU by using the FINE. For details, see section 42.8.3, Boot Mode (FINE Interface).
After setting the MD pin to the low level and the UB# pin to the high level or making it open-circuit at the time of release from the reset state and then switching the MD# pin to the high level within 20 to 100 ms, the MCU starts up in boot mode (FINE interface).

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The state “Boot mode (FILE interface)” is added to Figure 3.1, Mode Setting Pin Levels and Operating Modes as shown below.

Before correction

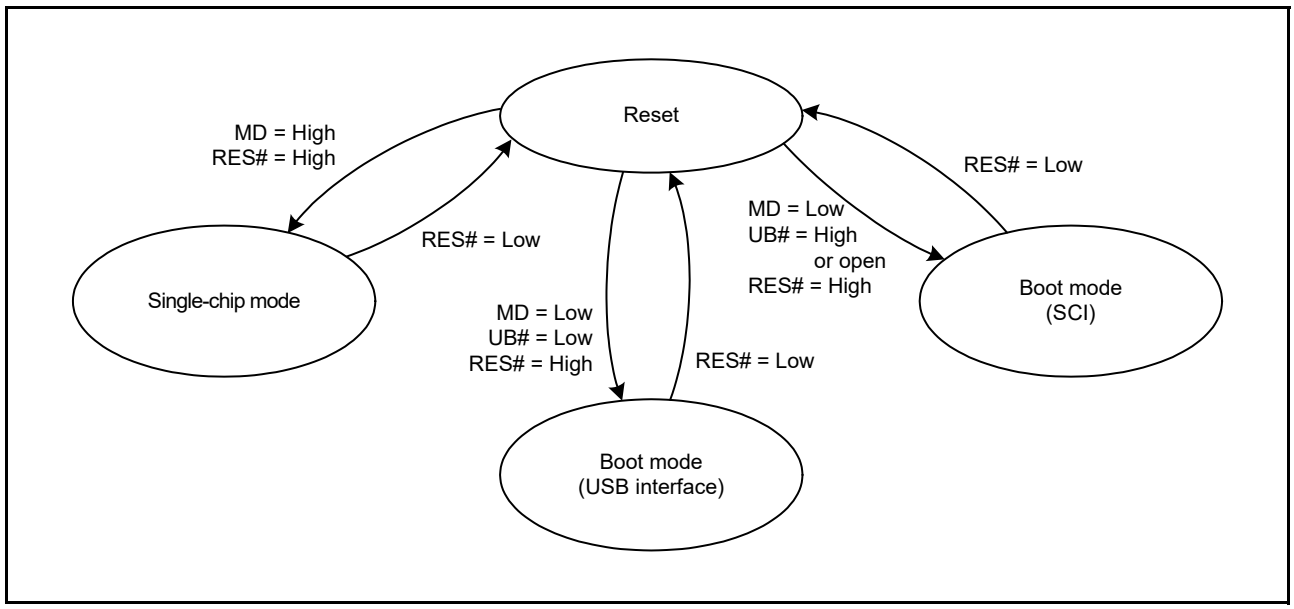
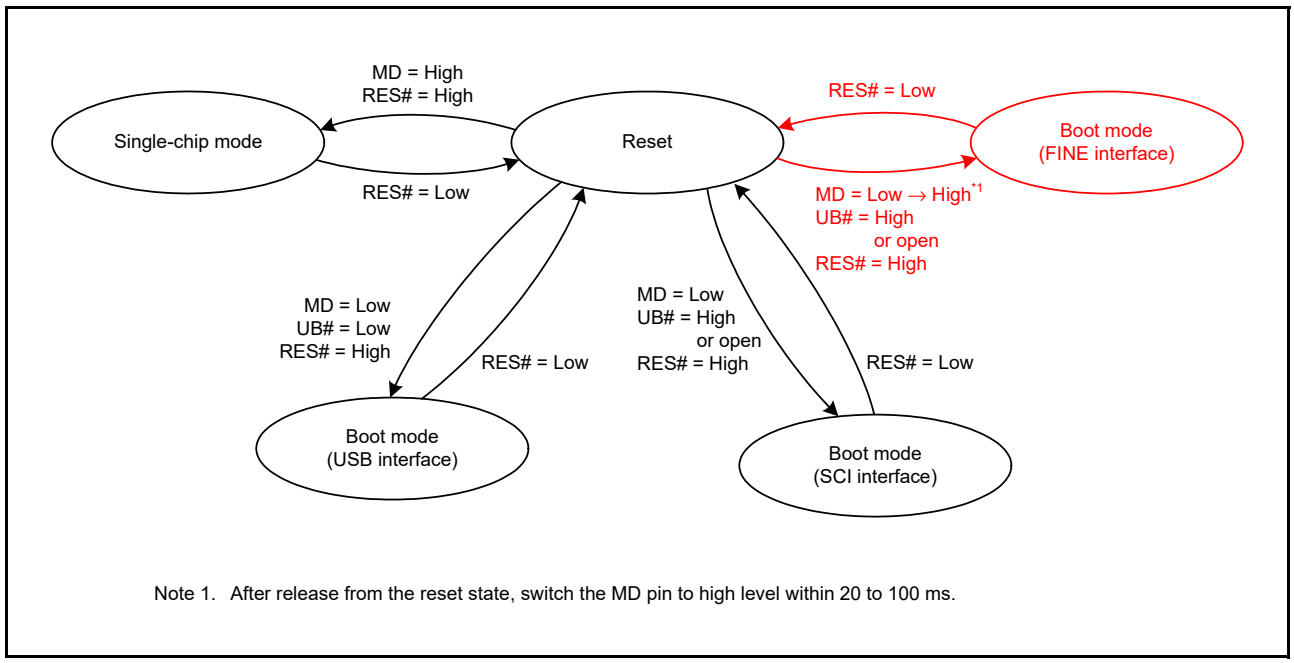


Figure 3.1 Mode Setting Pin Levels and Operating Modes

After correction



Note 1. After release from the reset state, switch the MD pin to high level within 20 to 100 ms.

Figure 3.1 Mode Setting Pin Levels and Operating Modes

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"LPT compare match interrupt via the ELC" is added to note 1 of Table 11.2, Operating Conditions of Each Power Consumption Mode as follows.

Before correction

Note 1. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, and USB interrupts).

After correction

Note 1. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, USB interrupts, and LPT compare match interrupt via the ELC).

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"LPT compare match interrupt via the ELC" is added to note 2 of Figure 11.1, Mode Transitions as follows.

Before correction

Note 2. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, and USB interrupts).

After correction

Note 2. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, USB interrupts, and LPT compare match interrupt via the ELC).

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"LPT compare match interrupt via the ELC" is added as a source for releasing the software standby mode to section 11.6.3.2, Exit from Software Standby Mode as follows.

Before correction

11.6.3.2 Exit from Software Standby Mode

Exit from software standby mode is initiated by an external pin interrupt (the NMI or IRQ0 to IRQ7), peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, and USB interrupts), a RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset. When any trigger which initiates exit from software standby mode is asserted, the oscillators which were operating before entry to software standby mode restart operation. After the oscillation of all these oscillators has been stabilized, operation returns from software standby mode.

- Initiated by an interrupt
  When an interrupt request from among the NMI, IRQ0 to IRQ7, RTC alarm, RTC interval, IWDT, voltage monitoring, and USB interrupts is generated, each of the oscillators which was operating before the transition to software standby mode resumes oscillation. After the oscillation stabilization wait time of each oscillator set by the MOSCWTCR.MSTS[4:0] bits or HOCOWTCR.HSTS[4:0] bits has elapsed, the MCU exits software standby mode and interrupt exception processing starts.

After correction

11.6.3.2 Exit from Software Standby Mode

Exit from software standby mode is initiated by an external pin interrupt (the NMI or IRQ0 to IRQ7), peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, USB interrupts, and LPT compare match interrupt via the ELC), a RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset. When any trigger which initiates exit from software standby mode is asserted, the oscillators which were operating before entry to software standby mode restart operation. After the oscillation of all these oscillators has been stabilized, operation returns from software standby mode.

- Initiated by an interrupt
  When an interrupt request from among the NMI, IRQ0 to IRQ7, RTC alarm, RTC interval, IWDT, voltage monitoring, USB interrupts, and LPT compare match interrupt via the ELC is generated, each of the oscillators which was operating before the transition to software standby mode resumes oscillation. After the oscillation stabilization wait time of each oscillator set by the MOSCWTCR.MSTS[4:0] bits or HOCOWTCR.HSTS[4:0] bits has elapsed, the MCU exits software standby mode and interrupt exception handling starts.

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A symbol for a pull-up resistor is added to Figure 27.2, Sample OTG Connection of USB Connector in Self-Powered State as follows.

Before correction

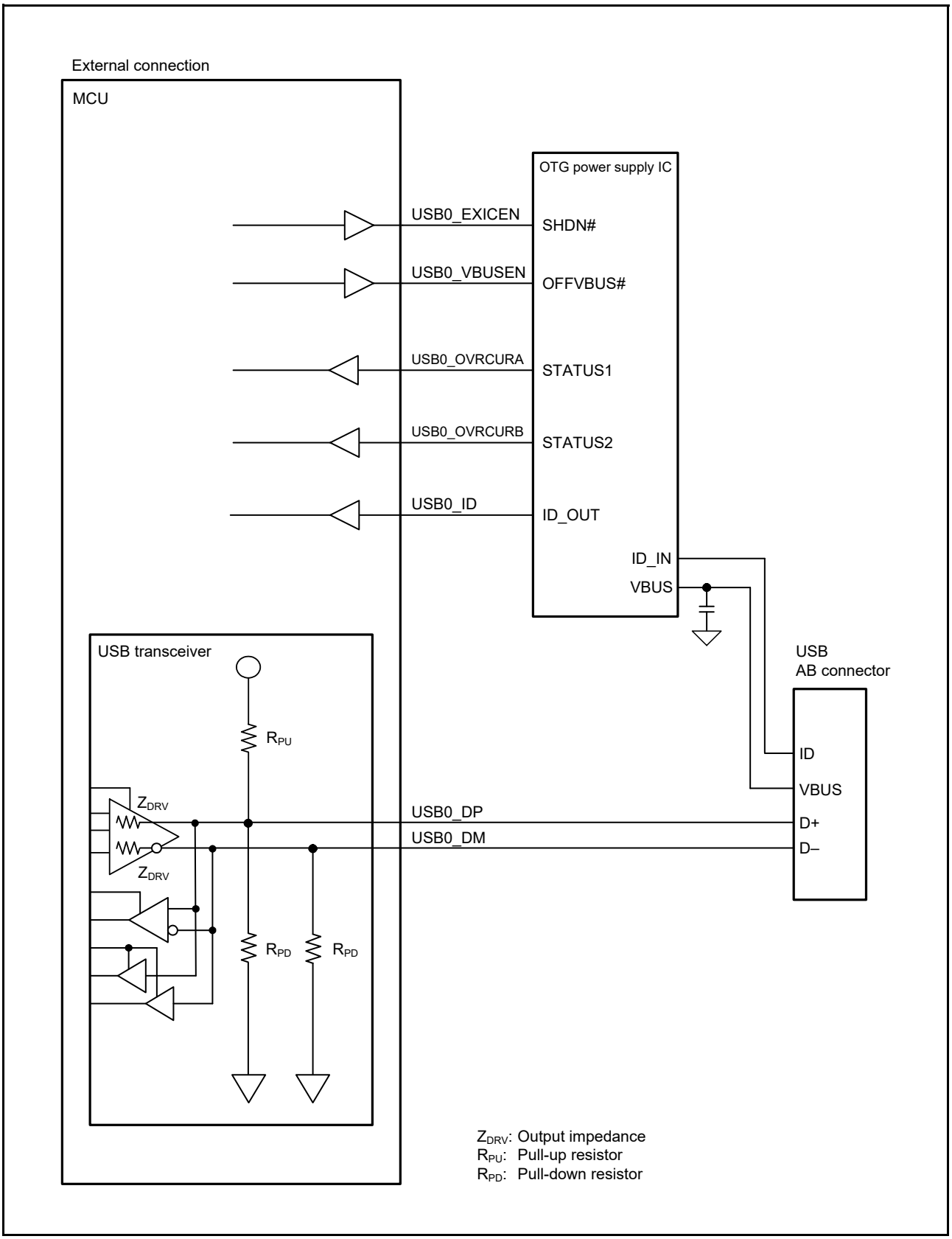

Figure 27.2 Sample OTG Connection of USB Connector in Self-Powered State

After correction

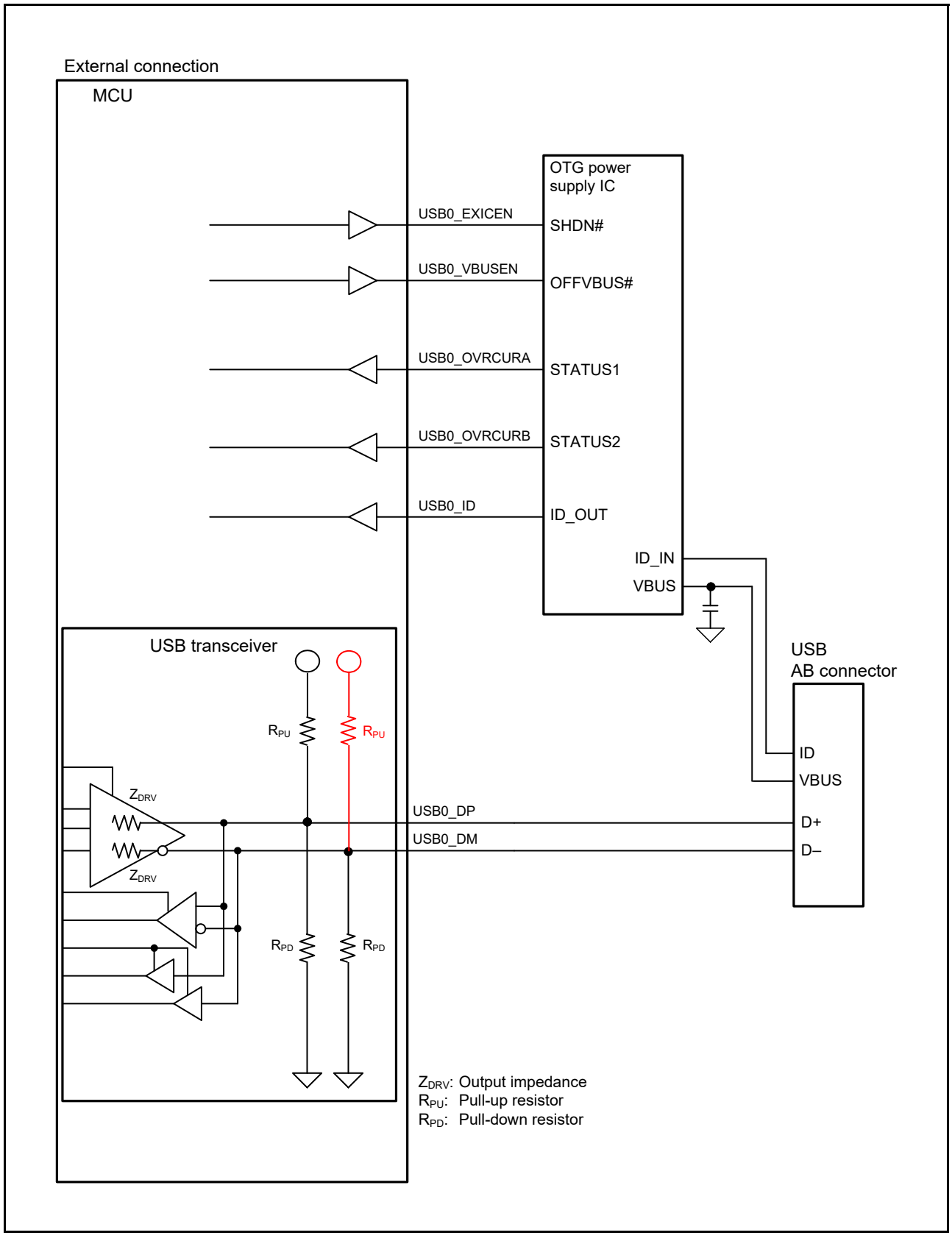

Figure 27.2 Sample OTG Connection of USB Connector in Self-Powered State

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The following descriptions are added to section 28.3.5, SCI Initialization (Asynchronous Mode).

Figure 28.9 shows an example of data transmission when the SCI is set to asynchronous mode according to the flow described in Figure 28.8 after a reset. When the pin function is set to the TXD pin, it is still high-impedance because the SCR.TE bit is 0. When the transmit data is written after setting the TE bit to 1, a data transmission starts. After the TE bit is set to 1, one frame of high is output from TXD pin (internal wait time) and then the data transmission starts.

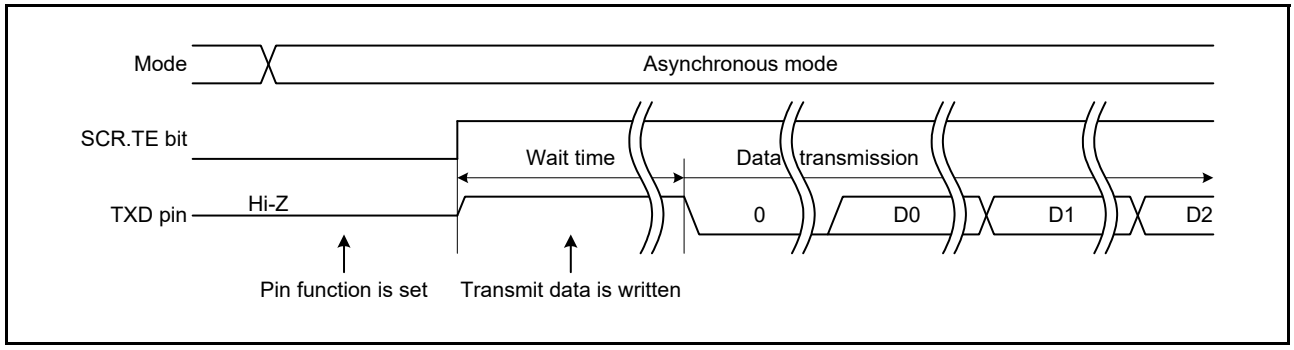

Figure 28.9 Example of Data Transmission Timing in Asynchronous Mode

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Figure 28.37, Example of SCI Initialization Flowchart (Smart Card Interface Mode) is modified as follows.

Before correction

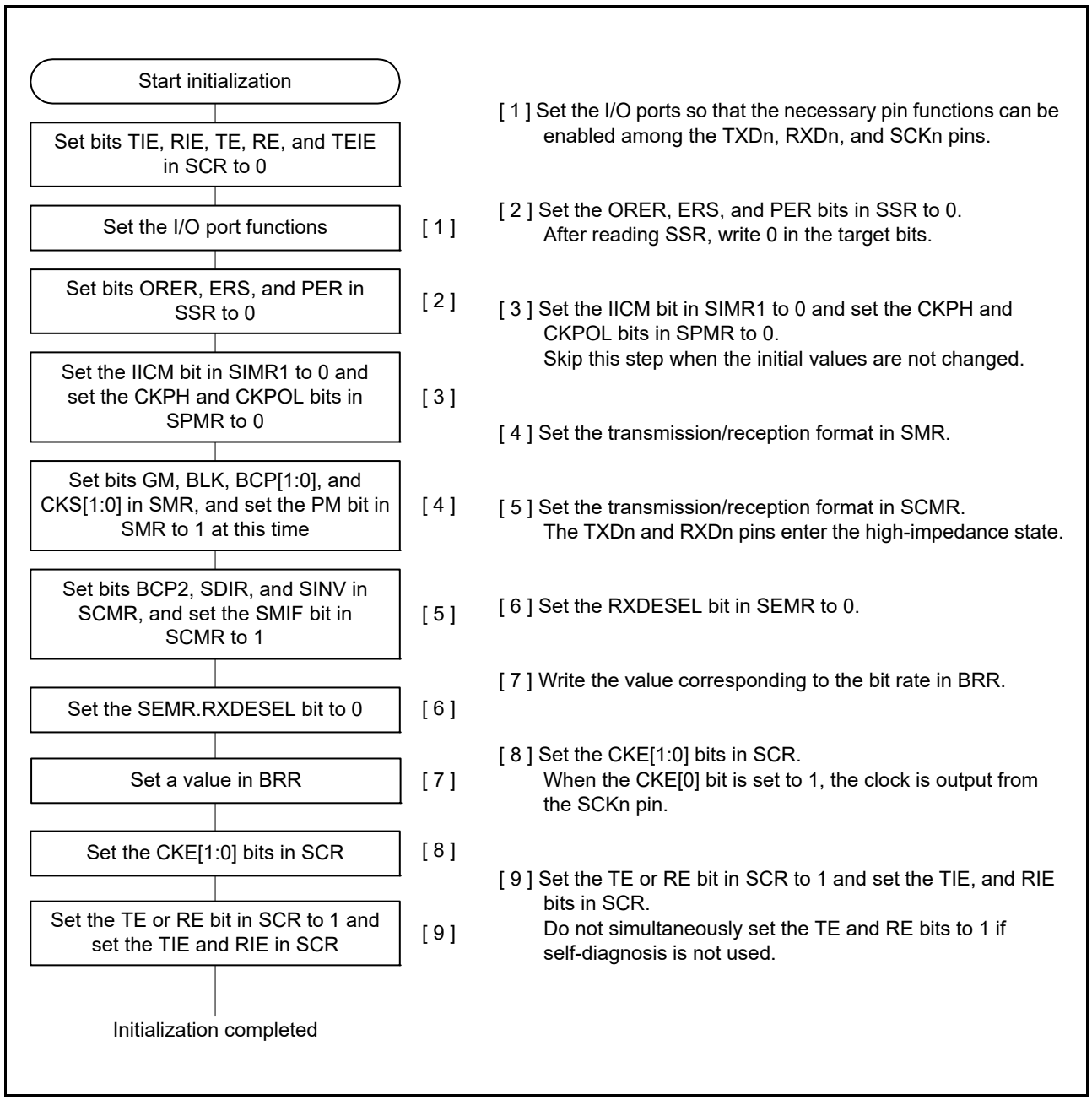

Figure 28.37 Example of SCI Initialization Flowchart (Smart Card Interface Mode)

After correction

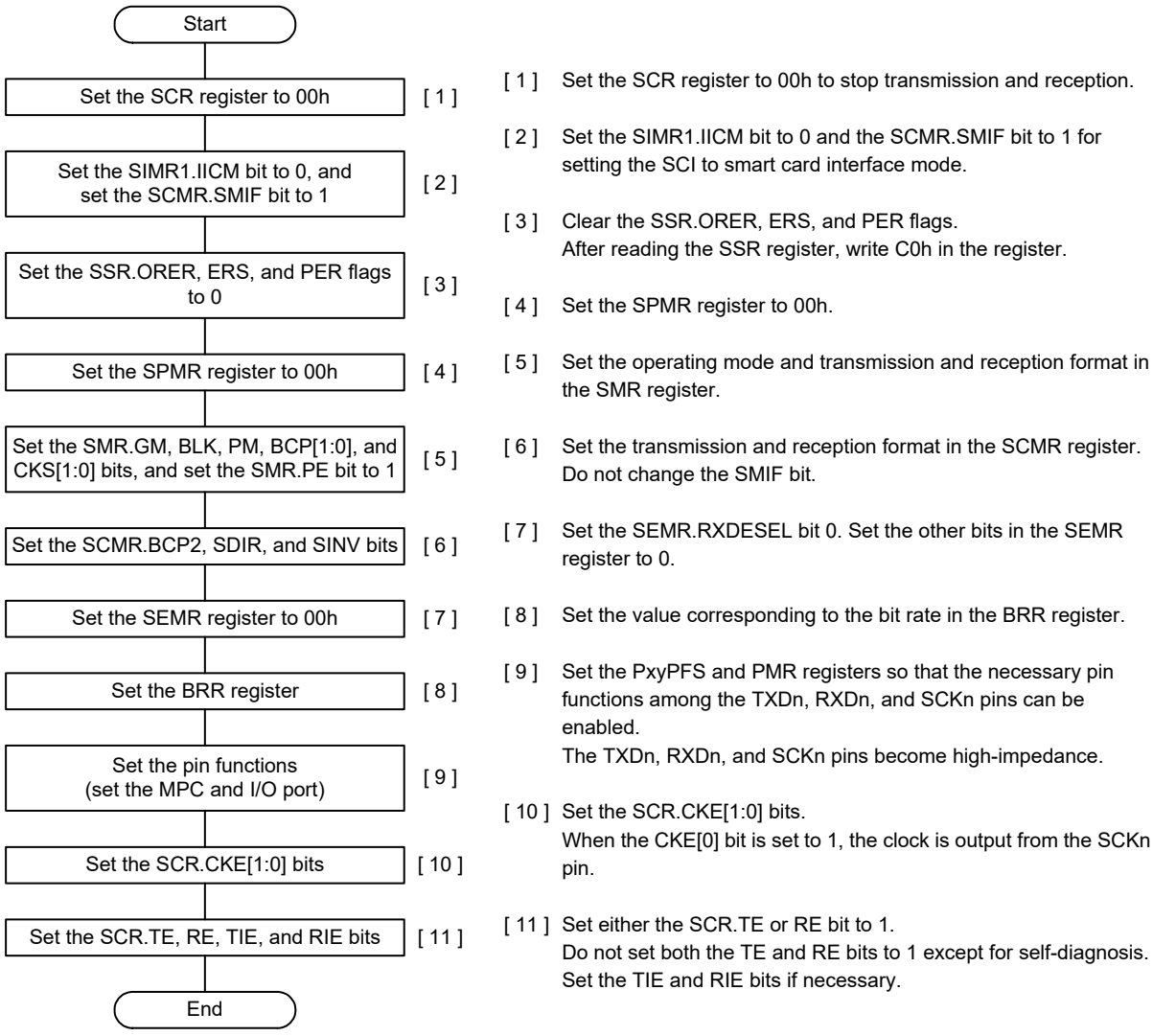

Figure 28.38 Example of SCI Initialization Flowchart (Smart Card Interface Mode)

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The following descriptions are added to section 28.6.5, SCI Initialization (Smart Card Interface Mode).

Figure 28.39 shows an example of data transmission when the SCI is set to smart card interface mode according to the flow described in Figure 28.38 after a reset. When the pin functions are set to the SCK and TXD pins, they are still high-impedance because the SCR.CKE[0] and SCR.TE bits are 0. When the CKE[0] bit is set to 1, clock is output from the SCK pin. When the transmit data is written after setting the TE bit to 1, a data transmission starts. After the TE bit is set to 1, one frame of high-impedance is output from TXD pin (internal wait time) and then the data transmission starts. In smart card interface mode, the clock is continuously output while the CKE[0] bit is set to 1 (clock output) even if both the TE and RE bits are set to 0.

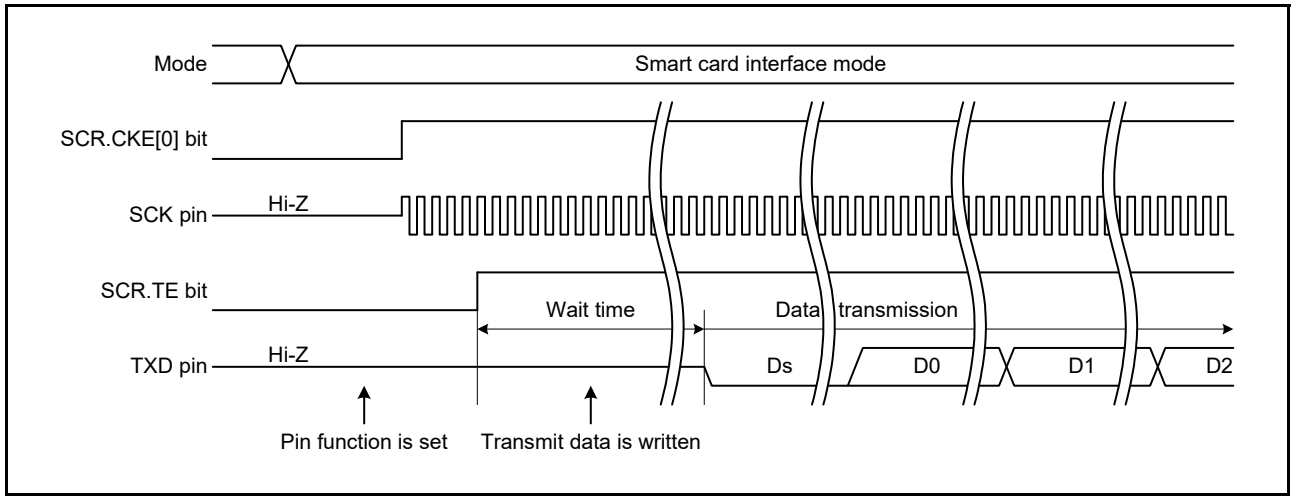

Figure 28.39 Example of Data Transmission Timing in Smart Card Interface Mode

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Descriptions in section 28.6.8, Clock Output Control is modified as follows.

Before correction

28.6.8 Clock Output Control

Clock output can be fixed using the CKE[1:0] bits in the SCR register when the GM bit in the SMR register is 1. Specifically, the minimum width of a clock pulse can be specified.

Figure 28.43 shows an example of clock output fixing timing when the CKE[0] bit is controlled with GM = 1 and CKE[1] = 0.

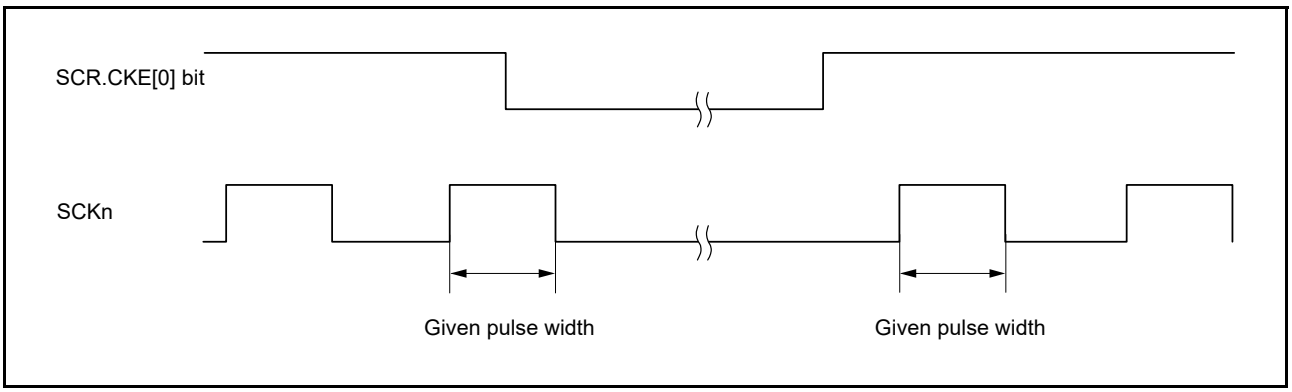

Figure 28.43 Clock Output Fixing Timing

At power-on, use the following procedure to secure the appropriate clock duty cycle.

(1) At Power-On

To secure the appropriate clock duty cycle simultaneously with power-on, use the following procedure.

1. Initially, port input is enabled in the high-impedance state. To fix the potential level, use a pull-up or pull-down resistor.
2. Fix the SCKn pin to the specified output by setting the SCR.CKE[1] bit and I/O port functions.
3. Set SMR and SCMR to enable smart card interface mode.
4. Set the SCR.CKE[0] bit to 1 to start clock output.

After correction

28.6.8 Clock Output Control

Clock output can be fixed to high or low using the SCR.CKE[1:0] bits when the SMR.GM bit is 1. When the CKE[1:0] bits are set to 01b (clock output), the base clock is output from the SCK pin. For the settings of the base clock frequency (bit rate), refer to section 28.2.9, Bit Rate Register (BRR). When the CKE[1:0] bits are set to 00b (output fixed low) or 10b (output fixed to high), the SCK pin can be fixed to low or high.
Figure 28.45 shows a timing chart when the clock output is controlled.
If changing the CKE[1:0] bits while the SMR.GM bit is 0 (non-GSM mode), a pulse of unexpected width may output from SCK pin because the result is immediately reflected to the SCK pin.

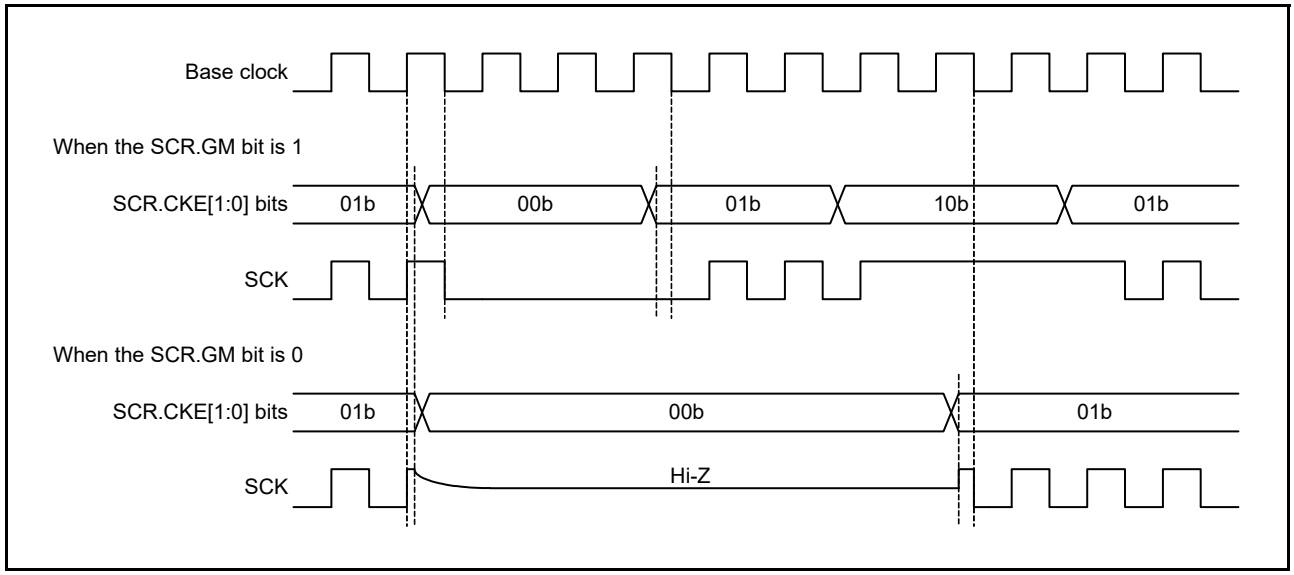

Figure 28.45 Clock Output Control

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The following section 28.7.7, Recovery from Bus Hang-up is added to section 28.7, Operation in Simple I^2C Mode as follows.

28.7.7 Recovery from Bus Hang-up

If the bus is stuck by an abnormal state in SCI because of the communication error, reset the SCI according to the following steps and release the bus.

(1) Set the SCR.TE and RE bit to 0 at the same time to reset SCI.
(2) Set the SIMR3 register to F0h to release the bus.
(3) If the SSR.RDRF flag is 1, dummy-read the RDR register to clear the flag.
(4) Set the SCR.TE and RE bit to 1 at the same time.

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Expressions in section 28.13.14, Note on Transmit Enable Bit (TE Bit) are modified and note 1 is added as follows.

Before correction

When setting the SCR.TE bit to 0 (serial transmission is disabled) while the pin function is “TXDn”, output of the pin becomes high impedance.
Prevent the TXDn line from becoming high impedance by any of the following ways:
(1) Connect a pull-up resistor to the TXDn line.
(2) Change the pin function to “general-purpose I/O port, output” before setting the SCR.TE bit to 0.
Set the SCR.TE bit to 1 before changing the pin function to “TXDn”.

After correction

When setting the pin function to “TXDn” while the SCR.TE bit is 0 (serial transmission is disabled) or setting the TE bit to 0 while the pin function is “TXDn”, output of the TXDn pin becomes high-impedance.
Prevent the TXDn line from becoming high-impedance by any of the following ways:
(1) Connect a pull-up resistor to the TXDn line.
(2) Set the TE bit to 1*1 before changing the pin function to “TXDn”. Change the pin function to “general-purpose I/O port, output” before setting the TE bit to 0.

Note 1. An interrupt is generated when the TE bit is set to 1 while the TXI interrupt is enabled. If this creates a problem, change the pin function to “TXDn” first, and then set the corresponding ICU.IERm.IENj bit to 1.

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Descriptions for the CTSUICOG[1:0] bits in section 35.2.15, CTSU Sensor Offset Register 1 (CTSUSO1) are modified as follows.

Before correction

CTSUICOG[1:0] Bits (CTSU ICO Gain Adjustment)

These bits adjust the output frequency gain of the sensor ICO and the reference ICO. Normally, the value of these bits should be set to 00b for the maximum gain. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, set the gain adjustment bits to adjust the gain appropriately.

After correction

CTSUICOG[1:0] Bits (CTSU ICO Gain Adjustment)

These bits adjust the output frequency gain of the sensor ICO and the reference ICO. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, set the gain adjustment bits to adjust the gain appropriately.

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Descriptions of section 36.8.14, Port Setting When 12-Bit A/D Converter Inputs are Used are modified as follows.

Before correction

36.8.14 Port Setting When 12-Bit A/D Converter Inputs are Used

When the 12-bit A/D converter is used, output from port 4 and port 9 should not be used. This is because an analog power supply is used for parts of the port 4 and port 9 circuits.

After correction

36.8.14 Port Setting When 12-Bit A/D Converter Inputs are Used

When the 12-bit A/D converter is used, output from ports 4, 9, and J (PJ6, PJ7) should not be used. This is because an analog power supply is used for parts of the ports 4, 9, and J (PJ6, PJ7) circuits.

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The register name written in section 37.2.3, DADRm Format Select Register (DADPR) (m = 0, 1) is changed as follows.

Before correction

37.2.3 DADRm Format Select Register (DADPR) (m = 0, 1)

After correction

37.2.3 Data Register Format Select Register (DADPR)

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Expression for the capacitance written in Table 43.14, DC Characteristics (12) is modified as follows.

Before correction

Table 43.14 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

After correction

Table 43.14 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	4.7 µF +50/–70%*1

Note 1. A multilayer ceramic capacitor whose nominal capacitance is 4.7 µF is recommended.

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The maximum specification for slave mode in Table 43.31, Timing of On-Chip Peripheral Modules (2) is deleted as follows.

Before correction

Table 43.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 43.42
		Slave		8	4096		
(Omitted)							

After correction

Table 43.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 43.42
		Slave		8	—		
(Omitted)							

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The maximum specification for slave mode in Table 43.32, Timing of On-Chip Peripheral Modules (3) is deleted as follows.

Before correction

Table 43.32 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 43.42
	SCK clock cycle input (slave)		6	65536	t_{Pcyc}	
(Omitted)						

After correction

Table 43.32 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 43.42
	SCK clock cycle input (slave)		6	—	t_{Pcyc}	
(Omitted)						

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The list of capacitors in Table 43.51, Internal Voltage Boosting Method is modified as follows.

Before correction

Table 43.51 Internal Voltage Boosting Method

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected between CAPH and CAPL pins	C1	0.33	0.47	0.61	µF	
External capacitor connected to V_{L1} pin	C2	0.33	0.47	0.61	µF	
External capacitor connected to V_{L2} pin	C3	0.33	0.47	0.61	µF	
External capacitor connected to V_{L3} pin	C4	0.33	0.47	0.61	µF	
External capacitor connected to V_{L4} pin	C5	0.33	0.47	0.61	µF	

After correction

Table 43.51 Internal Voltage Boosting Method

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Value	Test Conditions
External capacitance connected between CAPH and CAPL pins	0.47 µF ±30%	
External capacitance connected to V_{L1} to V_{L4} pins	0.47 µF ±30%	

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Conditions written in Table 43.52, Internal Voltage Boosting Method LCD Characteristics are deleted and the symbol for the tripler output voltage is corrected as follows.

Before correction

Table 43.52 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	C1 to C4 connected	VLCD = 04h	0.9	1.0	1.08	V	
			VLCD = 05h	0.95	1.05	1.13	V	
			VLCD = 06h	1	1.1	1.18	V	
			VLCD = 07h	1.05	1.15	1.23	V	
			VLCD = 08h	1.1	1.2	1.28	V	
			VLCD = 09h	1.15	1.25	1.33	V	
			VLCD = 0Ah	1.2	1.3	1.38	V	
			VLCD = 0Bh	1.25	1.35	1.43	V	
			VLCD = 0Ch	1.3	1.4	1.48	V	
			VLCD = 0Dh	1.35	1.45	1.53	V	
			VLCD = 0Eh	1.4	1.5	1.58	V	
			VLCD = 0Fh	1.45	1.55	1.63	V	
			VLCD = 10h	1.5	1.6	1.68	V	
			VLCD = 11h	1.55	1.65	1.73	V	
			VLCD = 12h	1.6	1.70	1.78	V	
			VLCD = 13h	1.65	1.75	1.83	V	
Doubler output voltage	V_{L2}	C1 to C3, C5 connected		$2V_{L1}$ - 0.10	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L3}	C1 to C5 connected		$3V_{L1}$ - 0.15	$3V_{L1}$	$3V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}			5	—	—	ms	
LCD output voltage variation range*2	t_{VLWT}	C1 to C4 connected		500	—	—	ms	

After correction

Table 43.52 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	0.9	1.0	1.08	V	VLCD = 04h
		0.95	1.05	1.13	V	VLCD = 05h
		1	1.1	1.18	V	VLCD = 06h
		1.05	1.15	1.23	V	VLCD = 07h
		1.1	1.2	1.28	V	VLCD = 08h
		1.15	1.25	1.33	V	VLCD = 09h
		1.2	1.3	1.38	V	VLCD = 0Ah
		1.25	1.35	1.43	V	VLCD = 0Bh
		1.3	1.4	1.48	V	VLCD = 0Ch
		1.35	1.45	1.53	V	VLCD = 0Dh
		1.4	1.5	1.58	V	VLCD = 0Eh
		1.45	1.55	1.63	V	VLCD = 0Fh
		1.5	1.6	1.68	V	VLCD = 10h
		1.55	1.65	1.73	V	VLCD = 11h
		1.6	1.70	1.78	V	VLCD = 12h
		1.65	1.75	1.83	V	VLCD = 13h
Doubler output voltage	V_{L2}	$2V_{L1}$ – 0.10	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L4}	$3V_{L1}$ – 0.15	$3V_{L1}$	$3V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}	5	—	—	ms	
LCD output voltage variation range*2	t_{VLWT}	500	—	—	ms	

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Conditions written in Table 43.53, Internal Voltage Boosting Method LCD Characteristics are deleted as follows.

Before correction

Table 43.53 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	C1 to C4 connected	VLCD = 04h	0.9	1.0	1.08	V	
			VLCD = 05h	0.95	1.05	1.13	V	
			VLCD = 06h	1	1.1	1.18	V	
			VLCD = 07h	1.05	1.15	1.23	V	
			VLCD = 08h	1.1	1.2	1.28	V	
			VLCD = 09h	1.15	1.25	1.33	V	
			VLCD = 0Ah	1.2	1.3	1.38	V	
Doubler output voltage	V_{L2}	C1 to C5 connected		$2V_{L1}$ - 0.08	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L3}	C1 to C5 connected		$3V_{L1}$ - 0.12	$3V_{L1}$	$3V_{L1}$	V	
Quadruply output voltage	V_{L4}	C1 to C5 connected		$4V_{L1}$ - 0.16	$4V_{L1}$	$4V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}			5	—	—	ms	
Voltage boost wait time*2	t_{VLWT}	C1 to C5 connected		500	—	—	ms	

After correction

Table 43.53 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	0.9	1.0	1.08	V	VLCD = 04h
		0.95	1.05	1.13	V	VLCD = 05h
		1	1.1	1.18	V	VLCD = 06h
		1.05	1.15	1.23	V	VLCD = 07h
		1.1	1.2	1.28	V	VLCD = 08h
		1.15	1.25	1.33	V	VLCD = 09h
		1.2	1.3	1.38	V	VLCD = 0Ah
Doubler output voltage	V_{L2}	$2V_{L1}$ - 0.08	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L3}	$3V_{L1}$ - 0.12	$3V_{L1}$	$3V_{L1}$	V	
Quadruply output voltage	V_{L4}	$4V_{L1}$ - 0.16	$4V_{L1}$	$4V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}	5	—	—	ms	
Voltage boost wait time*2	t_{VLWT}	500	—	—	ms	

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Statements regarding capacitors in Table 43.54, Capacitor Split Method are modified as follows.

Before correction

Table 43.54 Capacitor Split Method

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected between CAPH and CAPL pins	C1	0.33	0.47	0.61	µF	
External capacitor connected to V_{L1} pin	C2	0.33	0.47	0.61	µF	
External capacitor connected to V_{L2} pin	C3	0.33	0.47	0.61	µF	
External capacitor connected to V_{L3} pin	C4	0.33	0.47	0.61	µF	
External capacitor connected to V_{L4} pin	C5	0.33	0.47	0.61	µF	

After correction

Table 43.54 Capacitor Split Method

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Value	Test Conditions
External capacitance connected between CAPH and CAPL pins	0.47 µF ±30%	
External capacitor connected to V_{L1} pin	0.47 µF ±30%	
External capacitor connected to V_{L2} pin	0.47 µF ±30%	
External capacitor connected to V_{L4} pin	0.47 µF ±30%	

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Conditions and notes for voltage written in Table 43.55, Capacitor Split Method LCD Characteristics are deleted as follows.

Before correction

Table 43.55 Capacitor Split Method LCD Characteristics

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Conditions
V_{L4} voltage*1	V_{L4}	C1 to C4 connected	—	VCC	—	V	
V_{L2} voltage*1	V_{L2}	C1 to C4 connected	$2/3V_{L4}$-0.07	$2/3V_{L4}$	$2/3V_{L4}$+0.07	V	
V_{L1} voltage**1	V_{L1}	C1 to C4 connected	$1/3V_{L4}$-0.08	$2/3V_{L4}$	$2/3V_{L4}$+0.08	V	
Capacitor split wait time*1	t_{WAIT}		100	—	—	ms	

After correction

Table 43.55 Capacitor Split Method LCD Characteristics

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{L4} voltage	V_{L4}	—	VCC	—	V	
V_{L2} voltage	V_{L2}	$2/3V_{L4}$ – 0.07	$2/3V_{L4}$	$2/3V_{L4}$ + 0.07	V	
V_{L1} voltage	V_{L1}	$1/3V_{L4}$ – 0.08	$2/3V_{L4}$	$2/3V_{L4}$ + 0.08	V	
Capacitor split wait time*1	t_{WAIT}	100	—	—	ms	