RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A224A/E	Rev.	1.00
Title	Errata to R32C/117 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	R32C/117 Group	Lot No.	Reference Document	R32C/117 Group User's Manual: Hardware Rev. 1.10 (REJ09B0533-0110)		

This document describes corrections to the R32C/117 Group User's Manual: Hardware, Rev. 1.10.
The corrections are indicated in red in the list below.

- Page 25 of 604, register symbol "R3R0" in line 3 of 2.1.1 is corrected as follows:
  "R3R1"

- Page 41 of 604, register name "Increment/Decrement Counting Select Register" in Table 4.13 is corrected as follows:
  "Increment/Decrement Select Register"

- Pages 64 to 65 of 604, register name "CAN0 Acceptance Mask Register 0/1/2/3/4/5/6/7" in Tables 4.36 to 4.37 is corrected as follows:
  "CAN0 Mask Register 0/1/2/3/4/5/6/7"

- Page 67 of 604, reset value "XXXX XX00b" for the C0MSMR register in Table 4.39 is corrected as follows:
  "0000 0000b"

- Page 75 of 604, descriptions for the VDEN bit in Figure 6.4 are modified as follows:

Bit Symbol	Bit Name	Function	RW
VDEN	Low Voltage Detector Enable Bit	0: Low voltage detector disabled 1: Low voltage detector enabled	RW

- Page 77 of 604, description of the third paragraph of 6.2.1 is modified as follows:
  "When the voltage rises to or above Vdet(R) again, the VMF bit becomes 1 (VCC ≥ Vdet) and the LVDF bit becomes 1. At this point, an interrupt request is generated when the LVDIEN bit is 1."

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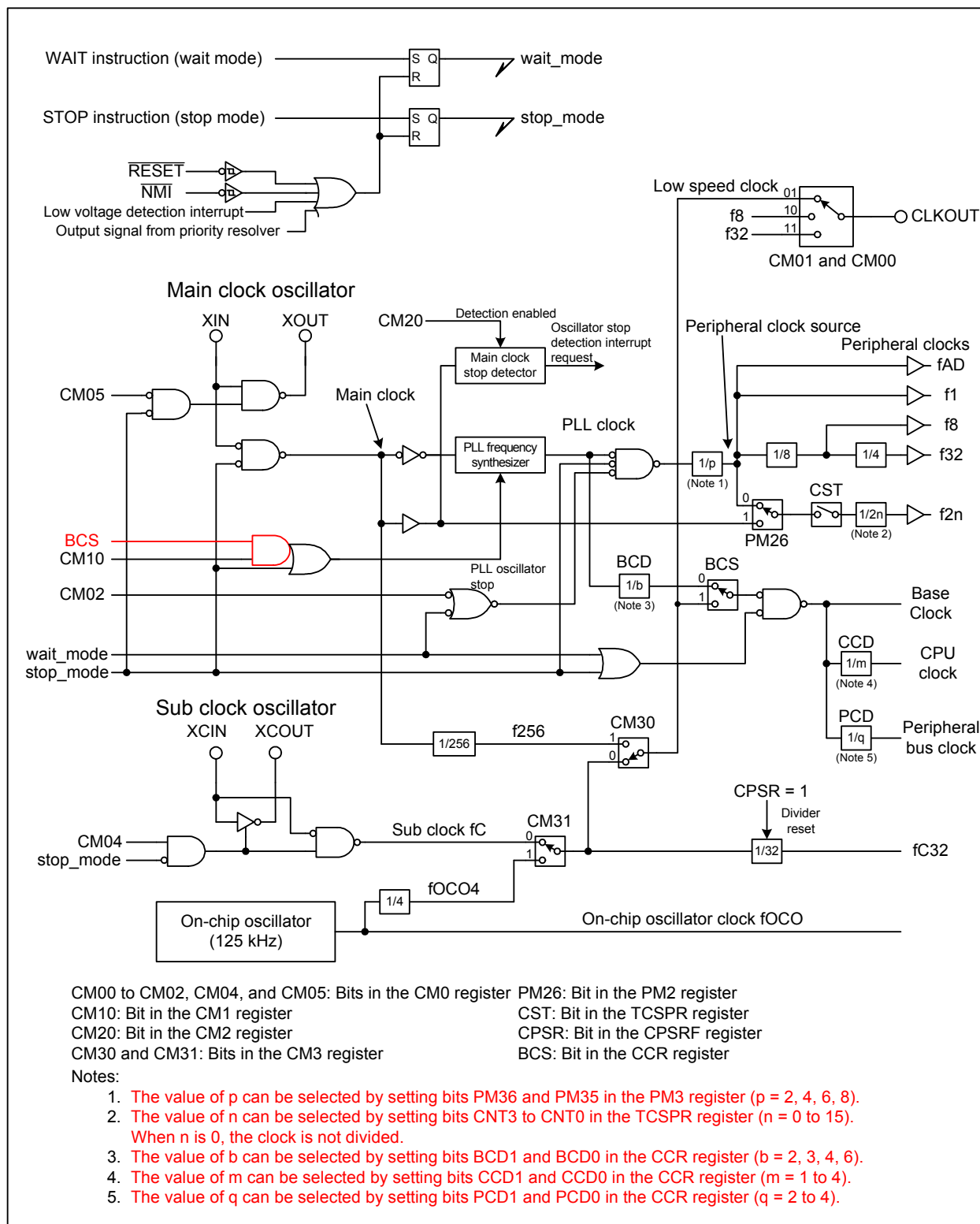•Page 83 of 604, Figure 8.1 is corrected as follows:

Figure 8.1   Clock Generation Circuitry

•Page 85 of 604, bit name "XCIN-XCOUT Drive Power Select Bit" in Figure 8.3 is modified as follows:
   "XCIN-XCOUT Drive Strength Select Bit"

•Page 85 of 604, the following description is added to Note 8 in Figure 8.3:
   "When rewriting this bit while the watchdog timer is running, set it immediately after writing to the WDTS register."

•Page 86 of 604, bit name "XIN-XOUT Drive Power Select Bit" in Figure 8.4 is modified as follows:
   "XIN-XOUT Drive Strength Select Bit"

•Page 86 of 604, description of Note 2 in Figure 8.4 is modified as follows:
   "When the BCS bit in the CCR register is 0 (PLL clock selected as base clock source), the PLL frequency synthesizer does not stop oscillating even if the CM10 bit is set to 1."

•Page 87 of 604, bit symbol "CM02" in Note 3 of Figure 8.5 is corrected as follows:
   "CM20"

•Page 96 of 604, description of the last paragraph of 8.1.4 is modified as follows:
   "The on-chip oscillator clock is stopped after a reset. It starts running when setting the CM31 bit in the CM3 register to 1. It is not necessary to wait for stabilization because the on-chip oscillator instantly starts oscillating."

•Page 97 of 604, description "(Refer to Figure 8.17 "State Transition (when the sub clock is used)")" is deleted from 8.2.

•Page 106 of 604, description of 8.7.2 is modified as follows:
   "The base clock stops in wait mode, so clocks generated by the base clock, the CPU clock and peripheral bus clock, stop running as well. Thus the CPU and watchdog timer, operated by these two clocks, also stop. Since the main clock, sub clock, PLL clock, and on-chip oscillator clock continue running, the peripherals using these clocks also continue operating."

•Page 115 of 604, mathematical symbols in 9.3.1 are corrected as follows:
   • In memory expansion mode

   $$0080000h \leq (CB23 \times 2^{18}) \leq (CB12 \times 2^{18}) \leq (CB01 \times 2^{18}) \leq 3DC0000h$$

   • In microprocessor mode

   $$0080000h \leq (CB23 \times 2^{18}) \leq (CB12 \times 2^{18}) \leq (CB01 \times 2^{18}) \leq 3FC0000h$$

•Pages 118 and 119 of 604, setting ranges for registers CB01, CB12, and CB23 in Figures 9.7 to 9.9 are corrected as follows:
   CB01: "02h to F8h in memory expansion mode" and "02h to FFh in microprocessor mode"
   CB12: "02h to F8h in memory expansion mode" and "02h to FFh in microprocessor mode"
   CB23: "02h to F8h in memory expansion mode" and "02h to FFh in microprocessor mode"

•Pages 118 and 119 of 604, descriptions of Note 2 in Figures 9.7 to 9.9 are modified as follows:
   CB01: "The setting value should be equal to or greater than that of the CB12 register."
   CB12: "The setting value should be equal to or greater than that of the CB23 register and should be equal to or less than that of the CB01 register."
   CB23: "The setting value should be equal to or less than that of the CB12 register."

•Page 122 of 604, bit names of bits ESUR1 and ESUR0, bits ESUW1 and ESUW0, bits EWR1 and EWR0, and EWW1 and EWW0 in Figure 9.12 are modified as follows:
   ESUR1 and ESUR0: "Address Setup Cycles Before Read Setting Bit"
   ESUW1 and ESUW0: "Address Setup Cycles Before Write Setting Bit"
   EWR1 and EWR0: "Read Pulse Width Setting Bit"
   EWW1 and EWW0: "Write Pulse Width Setting Bit"

• Page 138 of 604, description "Bits PRC0 and PRC1 do not automatically become 0. They should be set to 0 by a program." is deleted from Note 1 of Figure 10.1.

• Page 141 of 604, description of Note 1 in Figure 11.1 is modified as follows:
"The peripheral interrupts are generated by the corresponding peripherals in the MCU."

• Page 142 of 604, the second paragraph of (5) in 11.2 is modified as follows:
"The stack pointer (SP) used for this interrupt differs depending on the software interrupt numbers. For software interrupt numbers 0 to 127, when an interrupt request is accepted, the U flag is saved and set to 0 to select the interrupt stack pointer (ISP) during the interrupt sequence. The saved data of the U flag is restored upon returning from the interrupt handler. For software interrupt numbers 128 to 255, the stack pointer does not change during the interrupt sequence."

• Page 144 of 604, description of 11.5 is corrected as follows:
"Each interrupt vector has a 4-byte memory space, in which the start address of the associated interrupt handler is stored. When an interrupt request is accepted, a jump to the address set in the interrupt vector takes place. Figure 11.2 shows an interrupt vector."

• Page 145 of 604, description in the Remarks for the BRK instruction in Table 11.1 is corrected as follows:
"If address FFFFFFE7h is FFh, a jump to the interrupt vector of software interrupt number 0 in the relocatable vector table takes place"

• Page 152 of 604, description for the IR bit below Figure 11.4 is corrected as follows:
"The IR bit becomes 1 (interrupt requested) when an interrupt request is generated; this bit setting is retained until the interrupt request is accepted. When the request is accepted and a jump to the corresponding interrupt vector takes place, the IR bit becomes 0 (no interrupt requested).
The IR bit can be set to 0 by a program. This bit should not be set to 1."

• Page 156 of 604, description of Note 1 in Table 11.7 is corrected as follows:
"These are the values when the interrupt vectors are aligned to the addresses in multiples of 4 in the internal ROM. However, the condition does not apply to the fast interrupt."

• Page 163 of 604, register symbol "IIOiE" in line 16 of 11.13 is corrected as follows:
"IIOiIE"

• Page 167 of 604, description in lines 4 to 6 of 12. Watchdog Timer is corrected as follows:
"Select either an interrupt request or a reset with the CM06 bit in the CM0 register for when the watchdog timer underflows. Once the CM06 bit is set to 1 (reset), it cannot be changed to 0 (watchdog timer interrupt) by a program. It can be set to 0 only by a reset."

• Page 170 of 604, expression "a value more than 00000001h" in the Specification of DMA transfer start-up in Table 13.1 is corrected as follows:
"a value other than 00000000h"

• Page 178 of 604, description of the first paragraph in 13.1 is corrected as follows:
"The transfer cycle is composed of bus cycles to read data from (source read) or to write data to (destination write) memory or an SFR."

• Page 179 of 604, external bus address "00060000h" in Table 13.5 is corrected as follows:
"00080000h"

• Page 184 of 604, source address "FFFFFFFh" in Note 1 of Table 14.1 is corrected as follows:
"FFFFFFFFh"

•Page 184 of 604, bit symbol "IIRLT" in the fifth bullet point of 14.1 is corrected as follows:
   "IRLT"

•Pages 186 and 187 of 604, expression "DMA II transfer complete interrupt vector address" in lines 3 to 4 and the seventh bullet point of 14.1.2 and Figure 14.2 is corrected as follows:
   "jump address for the DMA II transfer complete interrupt handler"

•Pages 186 and 189 of 604, expression "interrupt vector" in Figure 14.2 and 14.1.4 is corrected as follows:
   "interrupt vector space"

•Page 187 of 604, expression "jump address" in the seventh bullet point of 14.1.2 is corrected as follows:
   "start address"

•Page 188 of 604, bit names of the OPER bit and bits CNT0 to CNT2 in Figure 14.3 are modified as follows:
   OPER: "Calculation Result Transfer Select Bit"
   CNT0 to CNT2: "Number of Transfers Setting Bit"

•Page 198 of 604, description of the third bullet point of 16.1 is corrected as follows:
   "One-shot timer mode: The timer outputs pulses after a trigger input until the counter reaches 0000h"

•Page 201 of 604, "Counting" is deleted from bit names of bits TA0UD to TA4UD "Timer A0/1/2/3/4 Increment/ Decrement Counting Select Bit" and the register name "Increment/Decrement Counting Select Register" in Figure 16.7.

•Page 209 of 604, bit name of the MR2 bit in Figure 16.12 is modified as follows:
   "Increment/Decrement Switching Source Select Bit"

•Page 209 of 604, bit symbols "TAiTGH and TAiTGL" in Note 5 of Figure 16.12 are corrected as follows:
   "TAjTGH and TAjTGL"

•Page 210 of 604, pin name "INT2" in Figures 16.13 and 16.14 is corrected as follows:
   "$\overline{\text{INT2}}$"

•Page 228 of 604, description of the first bullet point of 16.3.3.2 is corrected as follows:
   "While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow)."

•Page 228 of 604, expression "TBj interrupt handler" in the eighth bullet point of 16.3.3.2 is changed as follows:
   "timer Bj interrupt handler"

•Page 232 of 604, description of Note 1 in Figure 17.3 is modified as follows:
   "Set this register after setting the PRC1 bit in the PRCR register to 1 (write enabled). Also, rewrite this register while timers A1, A2, A4, and B2 are stopped."

•Page 239 of 604, description "The sum of setting values for registers TAi and TAi1 should be identical to the setting value of the TB2 register in this mode." is deleted from lines 8 to 9 of 17.3.

•Page 243 of 604, bit symbol "INV06" in Note 3 of Figure 17.15 is corrected as follows:
   "INV16"

•Page 244 of 604, register symbol "INV1" in Note 2 of Figure 17.17 is corrected as follows:
   "INVC1"

•Pages 252 and 253 of 604, descriptions for the CRD bit in Figures 18.5 and 18.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
CRD	CTS Function Disable Bit	0: CTS function enabled 1: CTS function disabled	RW

•Page 254 of 604, description of function of the UiIRS bit in Figure 18.7 is modified as follows:
   "0: Transmit buffer is empty (TI = 1)
    1: Transmission is completed (TXEPT = 1)"

•Page 257 of 604, description of function of the SWC bit in Figure 18.11 is modified as follows:
   "0: No wait-state/wait-state cleared
    1: Hold the SCLi pin low after the eighth bit is received"

•Page 258 of 604, expression "UiBRG count source" in the function of bits DL0 to DL2 in Figure 18.12 is
 corrected as follows:
   "baud rate generator count source"

•Page 259 of 604, bit name of the RSTAREQ bit in Figure 18.13 is modified as follows:
   "Repeated START Condition Generate Bit"

•Page 259 of 604, description of function of the SWC9 bit in Figure 18.13 is modified as follows:
   "0: No wait-state/wait-state cleared
    1: Hold the SCLi pin low after the ninth bit is received"

•Page 267 of 604, "TXEPT flag" in Figure 18.20 is corrected as follows:
   "TXEPT bit"

•Page 267 of 604, bit symbol "UiRS" in the fourth dash of Figure 18.20 is corrected as follows:
   "UiIRS"

•Pages 275 and 276 of 604, descriptions of function of the UiIRS bit in Figures 18.25 and 18.26 are corrected as
 follows:
   0: "(an interrupt request is generated when the transmit buffer is empty)"
   1: "(an interrupt request is generated when transmission is completed)"

•Page 311 of 604, description of 19.1.5 is modified as follows:
   "In repeat sweep mode 1, the analog voltage applied to eight selected pins including one to four prioritized
   pins is repeatedly converted into a digital code. Table 19.6 lists specifications of repeat sweep mode 1."

•Page 311 of 604, description in the specification of the function in Table 19.6 is modified as follows:
   "The analog voltage applied to eight selected pins including one to four prioritized pins is repeatedly
   converted into a digital code. The prioritized pins are selected by setting bits SCAN1 and SCAN0 in the
   AD0CON1 register and bits APS1 and APS0 in the AD0CON2 register"

•Page 319 of 604, "AD0i register" in the ninth bullet point of 19.3.2 is modified as follows:
   "AD00 register"

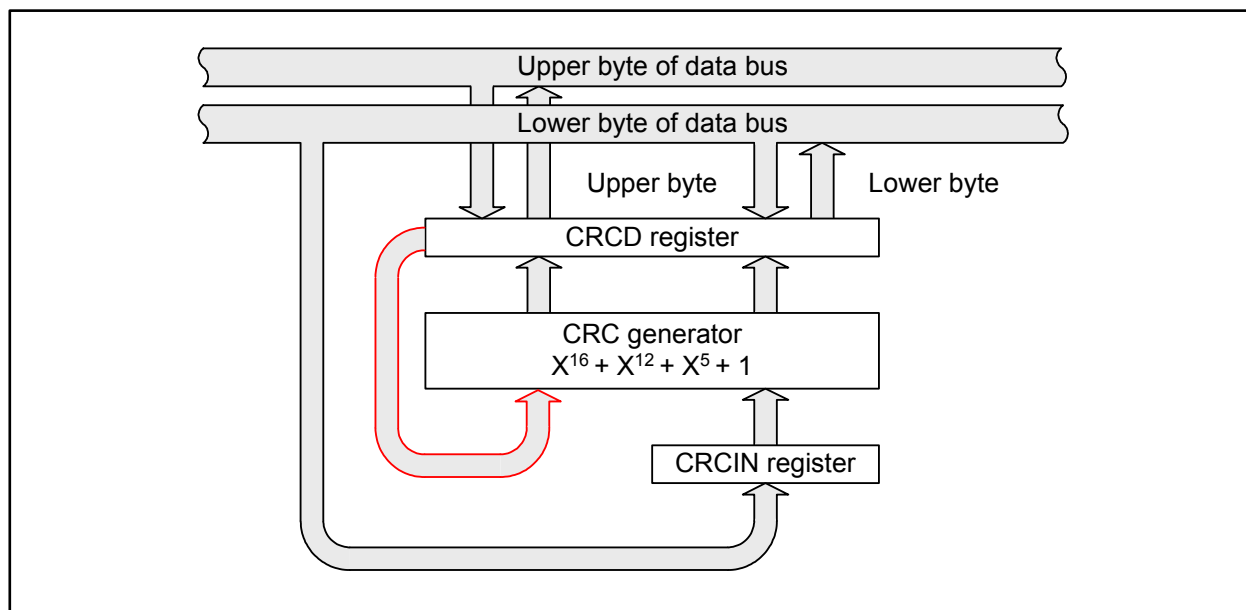•Page 322 of 604, Figure 21.1 is corrected as follows:

Figure 21.1   CRC Calculator Block Diagram

•Page 335 of 604, descriptions for bits UD0 and UD1 in Figure 23.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
UD0	Increment/Decrement Control Bit	b6 b5 0 0 : Increment mode 0 1 : Increment/decrement mode	RW
UD1		1 0 : Two-phase pulse signal processing mode [6] 1 1 : Do not use this combination	RW

•Page 338 of 604, Note 3 "The GOC bit becomes 0 after gating is cleared." is deleted from Figure 23.9.

•Page 344 of 604, description in the second bullet point of the reset conditions in Table 23.2 is modified as follows:
  "An input of low signal into the external interrupt pin ($\overline{INT0}$ or $\overline{INT1}$) as follows:"

•Page 345 of 604, description of the first bullet point of the selectable functions in Table 23.2 is corrected as follows:
  "The base timer starts counting when the BTS or BTiS bit is set to 1. When the base timer reaches FFFFh, it starts decrementing. When the RST1 bit in the GiBCR1 register is 1 (the base timer is reset by matching with the GiPO0 register), the timer counter starts decrementing two counts after the base timer value matches the GiPO0 register setting. When the timer counter reaches 0000h, it starts incrementing again (refer to Figure 23.20)."

•Pages 356, 358, and 361 of 604, expression "Input to the IIOi_j pin" in Figures 23.25 to 23.27 is corrected as follows:
  "IIOi_j pin"

•Pages 363 and 365 of 604, expression "Input to the OUTC2_j pin" in Figures 23.28 and 23.30 is corrected as follows:
  "OUTC2_j pin"

• Page 365 of 604, description "Bits RST2 to RST0 in the G2BCR1 register are set to 000b (base timer is not reset)" in the second dash is deleted from Case 1 in Figure 23.30.
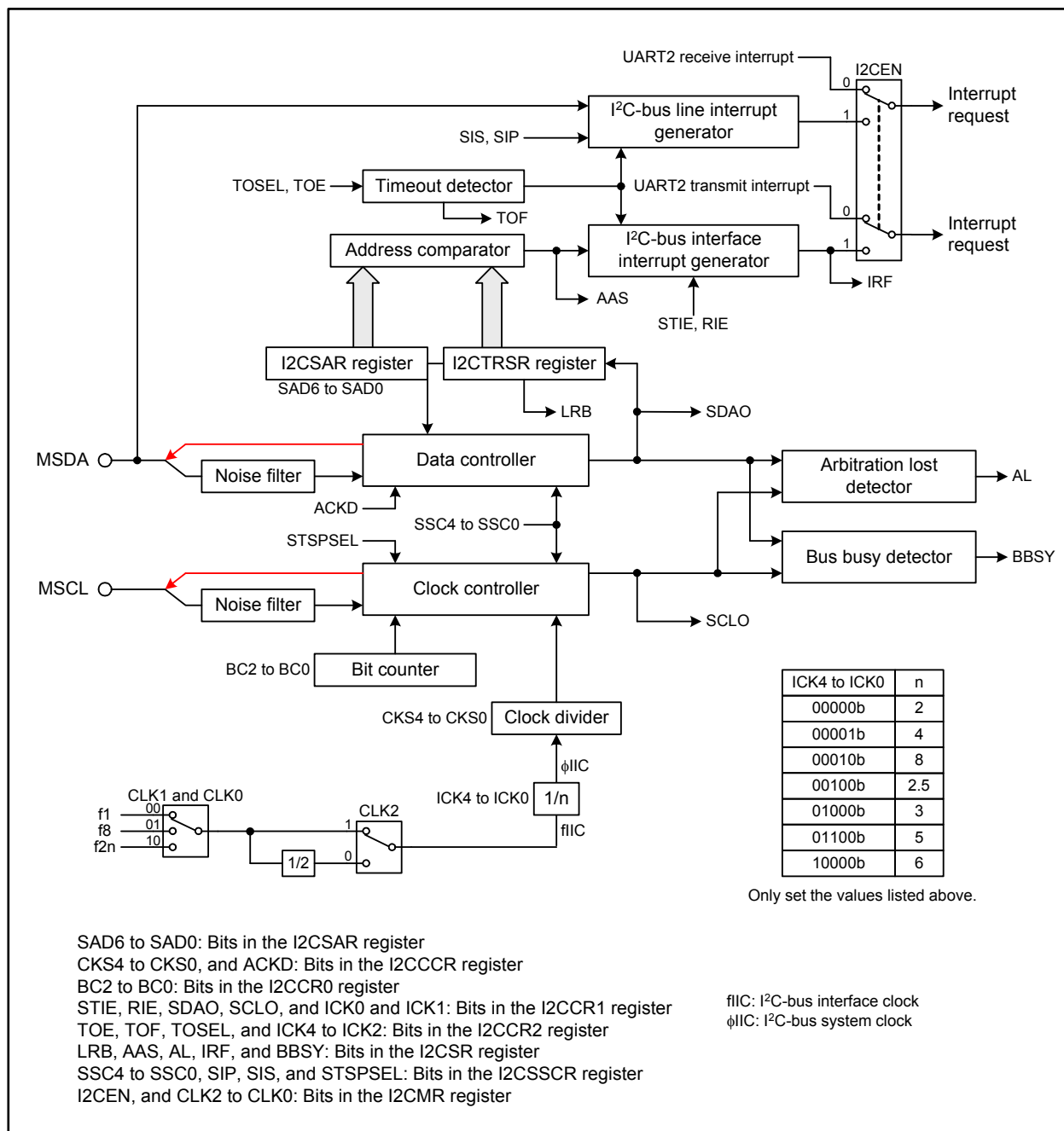
• Page 377 of 604, Figure 24.1 is corrected as follows:

Figure 24.1   Multi-master I^{2}C-bus Interface Block Diagram

• Page 392 of 604, description of the second bullet point of the case that the IRF bit becomes 1 in 24.1.8.5 is modified as follows:

"When data is written to the I2CCCR register (the RIE bit is 1, internal WAIT flag is 1)"

• Page 395 of 604, bit symbol "STR" in line 8 of 24.2 is corrected as follows:

"TRS"

•Page 411 of 604, descriptions for the RBOC bit in Figure 25.2 are modified as follows:

Bit Symbol	Bit Name	Function	RW
RBOC	Forced Recovery From Bus-off Bit [4]	0: Nothing occurred 1: Forced recovery from bus-off [5]	RW

•Page 428 of 604, expression "fCAN (CAN system clock)" in line 5 of 25.1.9.5 is modified as follows:
   "the peripheral bus clock"

•Page 431 of 604, expression "fCAN" in line 6 of 25.1.10.3 is modified as follows:
   "the peripheral bus clock"

•Page 437 of 604, description of function of b7 in Figure 25.17 is corrected as follows:
   b7: "No register bit; the read value is 0"

•Page 441 of 604, description of function of b6-b5 in Figure 25.19 is corrected as follows:
   b6-b5: "No register bits; the read value is 0"

•Page 452 of 604, Note "(4)" for the function of the EDPM bit in Figure 25.28 is moved as follows:

Bit Symbol	Bit Name	Function	RW
EDPM	Error Display Mode Select Bit [3]	0: Output of first detected error code [4] 1: Output of accumulated error code	RW

•Page 461 of 604,description of the first paragraph in 25.2.3 is modified as follows:
   "CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module.
   After a MCU reset, the CAN module starts from CAN sleep mode."

•Page 464 of 604, q value "q = 1, 2, 3, 4" in Figure 25.36 is corrected as follows:
   "q = 2, 3, 4"

•Page 476 of 604, description of the first and second paragraphs in 26. I/O Pins is corrected as follows (refer to
 TN-16C-A200A/E):
   "Each pin of the MCU functions as a programmable I/O port, an I/O pin for integrated peripherals, or a bus
   control pin. These functions can be switched by the function select registers or the processor mode
   registers. This chapter particularly addresses the function select registers. For the use as a bus control pin,
   refer to 7. "Processor Mode" and 9. "Bus".
   The pull-up resistors are enabled for every group of four pins. However, a pull-up resistor is separated from
   other peripherals even if it is enabled, when a pin functions as an output pin." ("or an analog I/O pin" is
   deleted)

•Page 476 of 604, Figure 26.1 is corrected as follows (refer to TN-16C-A200A/E):
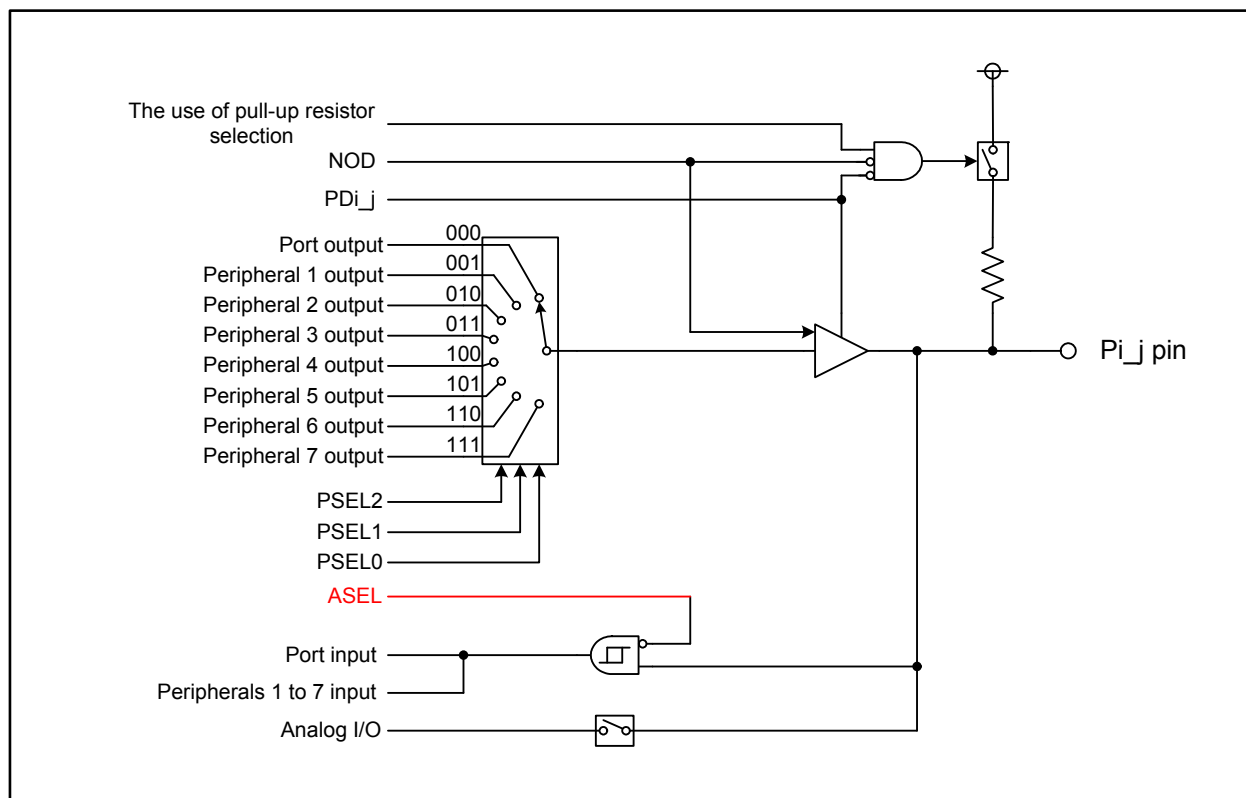

Figure 26.1   Typical I/O Pin Block Diagram (i = 0 to 15; j = 0 to 7)

•Page 476 of 604, description in the last paragraph of 26. I/O Pins is corrected as follows:
"The input-only port P8_5 shares a pin with $\overline{\text{NMI}}$ and has no function select register or bit 5 in the PD8 register. Port P14_1 (or P9_1 in the 100-pin package) also functions as an input-only port. The function select register and bit 1 in the PD14 register are reserved. Port P9 is protected from unexpected write accesses by the PRC2 bit in the PRCR register (refer to 10. "Protection")."

•Page 477 of 604, pin symbols "WR/WR0", "BC1/WR1", "BC2/WR2", and "BC3/WR3" in line 4 of 26.1 are corrected as follows:
"$\overline{\text{WR}}/\overline{\text{WR0}}$", "$\overline{\text{BC1}}/\overline{\text{WR1}}$", "$\overline{\text{BC2}}/\overline{\text{WR2}}$", "$\overline{\text{BC3}}/\overline{\text{WR3}}$"

•Pages 480, 491, and 495 of 604, expressions "IIO0 output" and "IIO1 output" in Figures 26.4, 26.15, and 26.19 are changed as follows:
"IIO0_i output" and "IIO1_i output"

•Page 482 of 604, "PD3_i register" in line 3 of the paragraph below Figure 26.6 is corrected as follows:
"PD3_i bit"

•Page 522 of 604, setting ranges for registers CB01, CB12, and CB23 in Table 27.8 are corrected as follows:
CB01: "02h to F8h"
CB12: "02h to F8h"
CB23: "02h to F8h"

•Page 548 of 604, "Programming and erasure endurance of flash memory" in Table 28.8 is changed as follows:
"Program/erase cycles"

- Page 548 of 604, unit "times" for "Programming and erasure endurance of flash memory" in Table 28.8 is corrected as follows:
    "Cycles"

- Pages 553 and 566 of 604, the following pins are added to the hysteresis for V_{T+} - V_{T-} in Tables 28.16 and 28.42:
    "MSCL" and "MSDA"

- Pages 554 and 567 of 604, expression "Driver power" in Tables 28.17 and 28.43 is modified as follows:
    "Drive strength"

- Page 584 of 604, "counting" is deleted from the UDF register name "Increment/decrement counting select register" in Table 29.1.

- Page 592 of 604, description of the first bullet point of 29.7.3.2 is corrected as follows:
    "While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow)."

- Page 592 of 604, expression "TBj interrupt handler" in the eighth bullet point of 29.7.3.2 is changed as follows:
    "timer Bj interrupt handler"

- Page 597 of 604, "AD0i register" in the ninth bullet point of 29.10.2 is modified as follows:
    "AD00 register"