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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU & MCU		Document No.	TN-RX*-A101A/E	Rev.	1.00
Title	Errata for the Ethernet Controller (ETHERC) and Ethernet Controller Direct Memory Access Controller (EDMAC) in RX62N Group		Information Category	Technical Notification		
Applicable Product	RX62N Group	Lot No. All	Reference Document	RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30 (R01UH0033EJ0130)		

This document describes corrections to section 26, Ethernet Controller (ETHERC) and section 27, Ethernet Controller Direct Memory Access Controller (EDMAC) in RX62N Group, RX621 Group User's Manual: Hardware.

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Descriptions for the TPC bit in the ETHERC mode register (ECMR) are corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b20	TPC	PAUSE Frame Transmission	0: PAUSE frame is not transmitted in a PAUSE period 1: PAUSE frame is transmitted even in a PAUSE period	R/W

After correction

Bit	Symbol	Bit Name	Description	R/W
b20	TPC	PAUSE Frame Transmission	0: PAUSE frame is transmitted even in a PAUSE period 1: PAUSE frame is not transmitted in a PAUSE period	R/W

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Descriptions in the BFR flag are changed as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b5	BFR	Continuous Broadcast Frame Reception	Continuous Broadcast Frame Reception Interrupt (Interrupt Source) Indicates that Broadcast frames have been received continuously.	R/W

After correction

Bit	Symbol	Bit Name	Description	R/W
b5	BFR	Continuous Broadcast Frame Reception Flag	0: Continuous reception of broadcast frames has not been detected. 1: Continuous reception of broadcast frames has been detected.	R/W

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Descriptions for the ETHERC status register (ECSR) are corrected as follows:

Before correction

ECSR indicates the status in the ETHERC. Each state can be notified to the CPU by interrupts. When 1 is written to the PSRTO, LCHNG, MPD, and ICD bits, the corresponding flags can be cleared. Writing 0 does not affect the flags. For bits that generate interrupts, the interrupt can be enabled or disabled by the corresponding bit in the ETHERC interrupt permission register (ECSIPR).

The interrupts generated due to ECSR are indicated in the ETHERC status register source bit (ECI) in ETHERC/EDMAC status register (EESR) of the EDMAC.

After correction

The ECSR register indicates the status in the ETHERC.
When 1 is written to the BFR, PSRTO, LCHNG, MPD, and ICD flags, the flags can be cleared. Writing 0 does not affect the flags.
When any of the flags in the ECSR register becomes 1 while the corresponding bit in the ETHERC interrupt permission register (ECSIPR) is 1 (interrupt notification is enabled), the ECI flag in the ETHERC/EDMAC status register (EESR) becomes 1.

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Descriptions for the BFSIPR bit in the ETHERC interrupt permission register (ECSIPR) are corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b5	BFSIPR	Continuous Broadcast Frame Reception Interrupt Enable	0: Interrupt notification by the corresponding bit in ECSR is disabled 1: Interrupt notification by the corresponding bit in ECSR is enabled	R/W

After correction

Bit	Symbol	Bit Name	Description	R/W
b5	BFSIPR	Continuous Broadcast Frame Reception Interrupt Enable	0: Interrupt notification by the BFR flag is disabled 1: Interrupt notification by the BFR flag is enabled	R/W

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Descriptions for the ETHERC interrupt permission register (ECSIPR) are corrected as follows:

Before correction

ECSIPR enables or disables the interrupt sources indicated by ECSR. Each bit can disable or enable interrupts corresponding to the bits in ECSR.

After correction

The ECSIPR register selects whether to notify the EDMAC of the status indicated by the ESCR register. Each bit corresponds to the flag that has the same number in the ESCR register.

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Descriptions for the ETHERC/EDMAC status register (EESR) are corrected as follows:

Before correction

EESR shows communications status on the EDMAC and the ETHERC.
The information in EESR is reported in the form of interrupt sources. Individual bits are cleared by writing 1 (however, the ECI bit is a read-only bit that is not cleared by writing 1) and are not affected by writing 0. Each interrupt source can be masked by means of the corresponding bit in the ETHERC/EDMAC status interrupt permission register (EESIPR).

After correction

The EESR register shows communications status on the EDMAC and the ETHERC.
Each flag in EESR can be output as an interrupt request signal (EINT) from the EDMAC. Each flag, excluding the ECI flag, becomes 0 by writing 1 and is not affected by writing 0. Each interrupt request can be enabled by means of the corresponding bit in the ETHERC/EDMAC status interrupt permission register (EESIPR).

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b11 to b8, and b3 to b0 in the transmit/receive status copy enable register (TRSCER) are changed to reserved bits, and "RD0.RFS" in the Description column is corrected to "RD0.RFE" as follows:

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	RRFCE	RRF Flag Copy Directive	0: The EESR.RRF flag status is reflected in the RD0.RFE bit of the receive descriptor. 1: The EESR.RRF flag status is not reflected in the RD0.RFE bit of the receive descriptor.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RMAFCE	RMAF Flag Copy Directive	0: The EESR.RMAF flag status is reflected in the RD0.RFE bit of the receive descriptor. 1: The EESR.RMAF flag status is not reflected in the RD0.RFE bit of the receive descriptor.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

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Descriptions for the transmit/receive status copy enable register (TRSCER) are corrected as follows:

Before correction

TRSCER specifies whether the information for the transmit and receive state reported by bits in the ETHERC/EDMAC status register (EESR) is to be reflected in the TFS25 to TFS0 or RFS26 to RFS0 bits of the corresponding descriptor. The bits in TRSCER correspond to bits 11 to 0 in EESR. When a bit is cleared to 0, the transmit status (bits 11 to 8 in EESR) is reflected in the TFS3 to TFS0 bits of the transmit descriptor, and the receive status (bits 7 to 0 in EESR) is reflected in the RFS7 to RFS0 bits of the receive descriptor. When a bit is set to 1, the occurrence of the corresponding source is not reflected in the descriptor. After this LSI is reset, all bits are cleared to 0.

After correction

The TRSCER register specifies whether the information for the receive state indicated by bits in the ETHERC/EDMAC status register (EESR) is reflected in the RFE bit of the receive descriptor as a summary. The bits in the TRSCER register correspond to bits in the EESR register that have the same number. When setting the RMAFCE or RRFCE bit to 0, the corresponding receive status (bit 7 or bit 4 in the EESR register) is reflected in the RFE bit of the receive descriptor. When setting the RMAFCE or RRFCE bit to 1, the corresponding receive status is not reflected.
After this MCU is reset, all bits are 0.

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Descriptions for the receive missed-frame counter register (RMFCR) are corrected as follows:

Before correction

RMFCR indicates the number of frames that could not be stored in the receive buffer and so were discarded during reception. When the receive FIFO overflows, the receive frames in the FIFO are discarded. The number of frames discarded at this time is counted. When the value in RMFCR reaches FFFFh, count-up is halted. The counter value is cleared to 0 by a write to RMFCR with any value.

After correction

The RMFCR register indicates the number of frames that could not be stored in the receive FIFO and so were discarded during reception. When the receive FIFO overflows, it stops receiving data, and the rest of frames are discarded. At the same time, the RMFCR register value is incremented. When the RMFCR register value reaches FFFFh, count-up is halted. When any value is written to the RMFCR register, the counter value becomes 0.

For the frame that has not been completely received, after data in the receive FIFO is transferred to the receive buffer, the RACT bit in the receive descriptor 0 (RD0) becomes 0 (descriptor disabled), the RFS9 bit becomes 1 (receive FIFO overflow), and the EESR.RFOF flag becomes 1 (overflow detected).

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Note 2 of the table for the transmit FIFO threshold register (TFTR) is deleted as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	TFT[10:0]	Transmit FIFO Threshold	*omitted*	R/W
b31 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1.When starting transmission before one frame of data write has completed, take care no underflow occurs.
Note 2.Operation cannot be guaranteed when the value set in TFTR is greater than the transmit FIFO size.
Note 3.To prevent a transmit underflow, setting the initial value (store and forward modes) is recommended.

After correction

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	TFT[10:0]	Transmit FIFO Threshold	*omitted*	R/W
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1.When starting transmission before one frame of data write has completed, take care no underflow occurs.
Note 2.To prevent a transmit underflow, using the initial value (store and forward modes) is recommended.

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The following description for the TFT bit[10:0] bits is deleted:

TFT[10:0] Bits (Transmit FIFO Threshold)

The transmit FIFO threshold must be set to a value smaller than the FIFO size specified by the FIFO depth register (FDR).

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Descriptions for the FIFO depth register (FDR) are corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	RFD[4:0]	Receive FIFO Size	00000: 256 bytes 00001: 512 bytes 00010: 768 bytes 00011: 1024 bytes 00100: 1280 bytes 00101: 1536 bytes 00110: 1792 bytes 00111: 2048 bytes Other than the above: Setting prohibited	R/W
b7 to b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b12 to b8	TFD[4:0]	Transmit FIFO Size	00000: 256 bytes 00001: 512 bytes 00010: 768 bytes 00011: 1024 bytes 00100: 1280 bytes 00101: 1536 bytes 00110: 1792 bytes 00111: 2048 bytes Other than the above: Setting prohibited	R/W
b31 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note:•Operation cannot be guaranteed when the value set in FDR is greater than the transmit or receive FIFO size.

After correction

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	RFD[4:0]	Receive FIFO Size	00111: 1968 bytes Other than the above: Setting prohibited	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12 to b8	TFD[4:0]	Transmit FIFO Size	00111: 2048 bytes Other than the above: Setting prohibited	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

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Descriptions for b2 to b0 in the flow control start FIFO threshold setting register (FCFTR) is corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RFDO[2:0]	Receive FIFO Overflow BSY Output Threshold	b2 b0 0 0 0: When 256 – 32 bytes of data is stored in the receive FIFO. 0 0 1: When 512 – 32 bytes of data is stored in the receive FIFO. : 1 1 0: When 1792 – 32 bytes of data is stored in the receive FIFO. 1 1 1: When 2048 – 64 bytes of data is stored in the receive FIFO.	R/W
b15 to b3	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b18 to b16	RFFO[2:0]	Receive Frame Count Overflow BSY Output Threshold	b18 b16 0 0 0: When two receive frames have been stored in the receive FIFO. 0 0 1: When four receive frames have been stored in the receive FIFO. 0 1 0: When six receive frames have been stored in the receive FIFO. : 1 1 0: When 14 receive frames have been stored in the receive FIFO. 1 1 1: When 16 receive frames have been stored in the receive FIFO.	R/W
b31 to b19	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W

After correction

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RFDO[2:0]	Receive FIFO Overflow PAUSE Output Threshold	b2 b0 0 0 0: When 224 (256 – 32) bytes of data is stored in the receive FIFO. 0 0 1: When 480 (512 – 32) bytes of data is stored in the receive FIFO. : 1 1 0: When 1760 (1792 – 32) bytes of data is stored in the receive FIFO. 1 1 1: When 1952 (2048 – 96) bytes of data is stored in the receive FIFO.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	RFFO[2:0]	Receive Frame Count Overflow PAUSE Output Threshold	b18 b16 0 0 0: When 2 receive frames have been stored in the receive FIFO. 0 0 1: When 4 receive frames have been stored in the receive FIFO. 0 1 0: When 6 receive frames have been stored in the receive FIFO. : 1 1 0: When 14 receive frames have been stored in the receive FIFO. 1 1 1: When 16 receive frames have been stored in the receive FIFO.	R/W
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

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Descriptions for the flow control start FIFO threshold setting register (FCFTR) are corrected as follows:

Before correction

FCFTR specifies the flow control of the ETHERC (specifies the threshold of automatic PAUSE output).
The threshold can be set in terms of the data size in the receive FIFO (RFDO[2:0] bits) and the number of receive frames (RFFO[2:0] bits). Flow control is turned on when either of the data size in the receive FIFO or the number of receive frames satisfies the corresponding threshold condition.
If the same receive FIFO size as set by the FIFO depth register (FDR) is set in FCFTR when flow control is to be turned on according to the condition set in the RFDO[2:0] bits, flow control is turned on with (FIFO data size - 64) bytes. For instance, when the FDR.RFD[4:0] bits = 00111b and the FCFTR.RFDO[2:0] bits = 111, flow control is turned on when (2,048 - 64) bytes of data is stored in the receive FIFO. The value set in the RFDO[2:0] bits should be equal to or smaller than the value set in the FDR.RFD[4:0] bits.

After correction

The FCFTR register specifies the flow control of the ETHERC (specifies the threshold of automatic PAUSE output).
The threshold can be set in terms of the data size (RFDO[2:0] bits) or the number of frames (RFFO[2:0] bits) stored in the receive FIFO. Flow control is turned on when either of the data size in the receive FIFO or the number of stored frames satisfies the corresponding threshold condition.

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Descriptions for b27 to b0 in the transmit descriptor 0 (TD0) and the TFE bit explanation are corrected as follows:

Bit	Symbol	Bit Name	Description	R/W
b25 to b0	TFS	Transmit Frame Status	Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: TFS25 to TFS9: Reserved TFS8: Detect Transmit Abort (corresponding to the EESR.TABT flag). TFS7 to TFS4: Reserved TFS3: Detect No Carrier (corresponding to the EESR.CND flag) TFS2: Detect Loss of Carrier (corresponding to the EESR.DLC flag) TFS1: Detect Delayed Collision during Transmission (corresponding to the EESR.CD flag) TFS0: Transmit Retry Over (corresponding to the EESR.TRO flag) When each bit becomes 1, it indicates that the corresponding error has occurred during frame transmission. When any of the TFS bits becomes 1, the TFE bit also becomes 1. When any of bits TFS3 to TFS0 becomes 1, TFS8 also becomes 1.	R/W
b26	TWBI	Write-Back Completion Interrupt Notification	(This bit is valid when TRIMD is set so.) 0: An interrupt request is not generated even when write-back to this descriptor is completed. 1: An interrupt request is generated when write-back to this descriptor is completed (while bits TRIMD.TIM and EESIPR.TWBIP are 1)	R/W
b27	TFE	Transmit Frame Error	0: Frame transmission is successfully completed. 1: An error occurs during frame transmission (transmission aborted).	R/W
			⋮ *omitted*	

TFE Bit (Transmit Frame Error)

When the TFE bit is 1, it indicates that any of the TFS bits is 1. ~~(Through the TRSCER setting, it is possible to prevent this bit from being set by an event indicated by TFS7 to TFS0. It is impossible, however, if an event indicated by TFS7 to TFS0 also causes TFS8 to be set.)~~

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Descriptions for b26 to b0 in the receive descriptor 0 (RD0) and the RFE bit explanation are corrected as follows:

Bit	Symbol	Bit Name	Description	R/W
b26 to b0	RFS	Receive Frame Status	Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: RFS26 to RFS10: Reserved RFS9: Receive FIFO overflow (corresponding to the EESR.RFOF flag) RFS8: Detect Receive Abort (corresponding to the EESR.RABT flag) RFS7: Receive Multicast Address Frame is received (corresponding to the EESR.RMAF flag) RFS6 and RFS5: Reserved RFS4: Receive Residual-Bit Frame is received (corresponding to the EESR.RRF flag) RFS3: Receive Too-Long Frame (corresponding to the EESR.RTLF flag) RFS2: Receive Too-Short Frame (corresponding to the EESR.RTSF flag) RFS1: PHY-LSI Receive Error (corresponding to the EESR.PRE flag) RFS0: CRC Error on Received Frame (corresponding to the EESR.CERF flag) When each bit becomes 1, it indicates that the corresponding error has occurred during frame reception. When any of the RFS bits becomes 1, the RFE bit also becomes 1 (set the TRSCER register to select whether bits RFS7 and RFS4 are reflected in the RFE bit). When any of bits RFS3 to RFS0 becomes 1, RFS8 also becomes 1.	R/W
b27	RFE	Receive Frame Error	0: No error has occurred in the received frame. 1: An error has occurred in the received frame.	R/W
			⋮ *omitted*	

RFE Bit (Receive Frame Error)

When the RFE bit is 1, it indicates that any of the RFS bits is 1 (set the TRSCER register to select whether bits RFS7 and RFS4 are reflected in the RFE bit). ~~It is impossible, however, if an event indicated by RFS7 to RFS0 also causes RFS8 to be set.)~~