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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A129A/E	Rev.	1.00
Title	Disclosure of Specifications for Low Power Timer (LPT) in the RX113 Group		Information Category	Technical Notification		
Applicable Product	RX113 Group	Lot No. All	Reference Document	RX113 Group User's Manual: Hardware Rev.1.02 (R01UH0448EJ0102)		

This document describes the disclosure of specifications for the low-power timer of the applicable product. The related descriptions in the RX113 Group User's Manual: Hardware Rev. 1.02 are changed.

1. Specification of Low Power Timer

1.1 Overview

RX113 Group integrates a low-power timer (LPT) that consists of a single-channel 16-bit timer. The LPT uses a sub-clock oscillator or IWDT-dedicated oscillator as the clock source , and can continue count operation even in software standby mode. A compare match signal can be used to wake up from software standby mode to normal operating mode.

Table 1.1 lists the specifications of the LPT and Figure 1.1 shows a block diagram of the LPT.

Table 1.1 LPT Specifications

Item	Description
Clock source	Sub-clock oscillator or IWDT-dedicated oscillator
Clock division ratio	Divided by 2, 4, 8, 16, or 32
Count operation	• Count up using the 16-bit up-counter • Count operation can be continued even in software standby mode
Compare match	Compare match 0 (a compare match signal is generated only in software standby mode)
Event link function (output)	An event signal is output when compare match 0 occurs (a compare match signal is generated only in software standby mode).

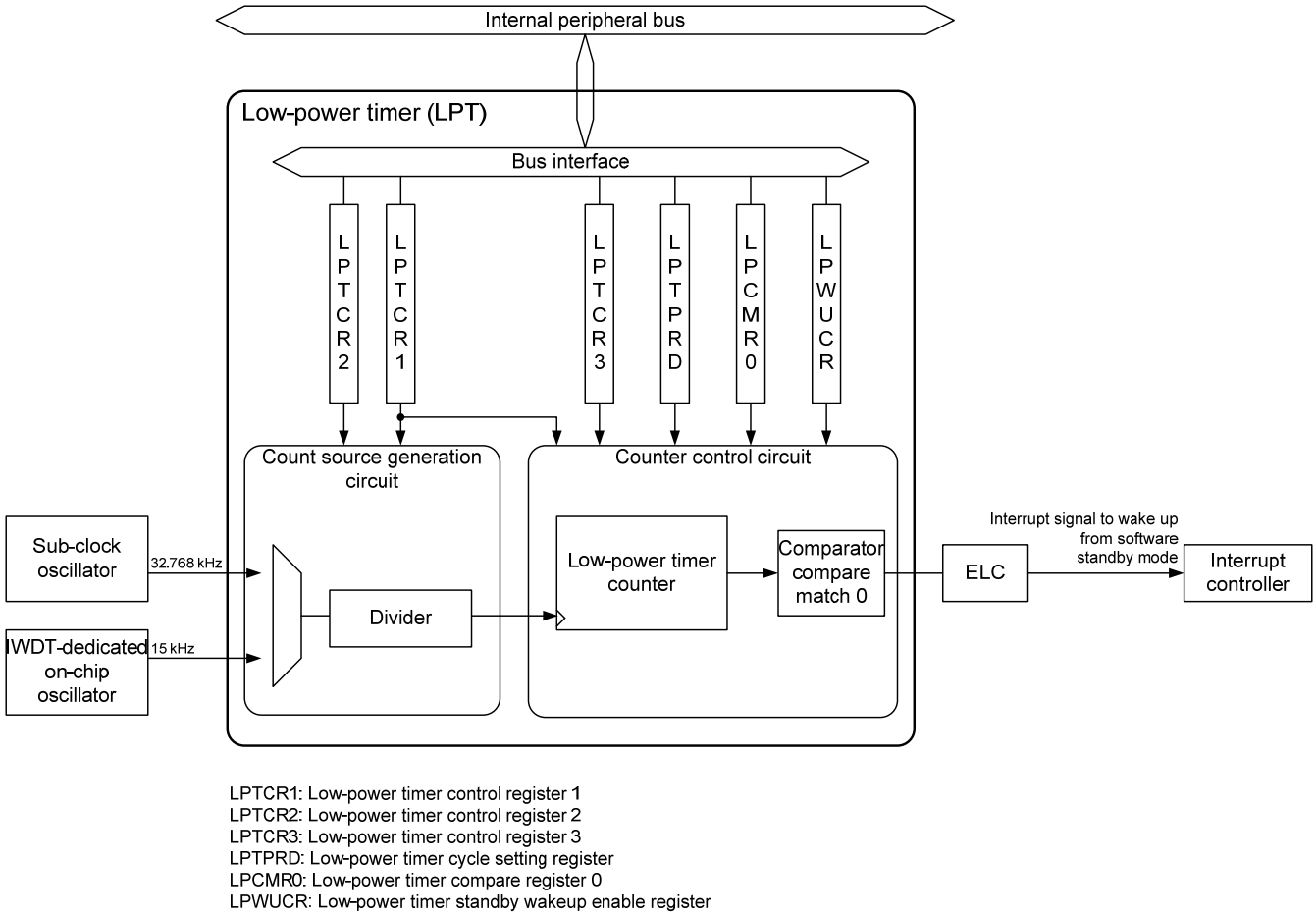


Figure 1.1 LPT Block Diagram

1.2 Register Descriptions

1.2.1 Low-Power Timer Control Register 1 (LPTCR1)

Address(es): 0008 00B0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LPCMRE0	—	LPCNTCKSEL	—	LPCNTPSSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	LPCNTPSSEL[2:0]	Low-Power Timer Clock Division Ratio Select	b2 b0 0 0 1: Source clock divided by 2 0 1 0: Source clock divided by 4 0 1 1: Source clock divided by 8 1 0 0: Source clock divided by 16 1 0 1: Source clock divided by 32 Settings other than above are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	LPCNTCKSEL	Low-Power Timer Clock Source Select *1	0: Sub-clock oscillator is selected 1: IWDT-dedicated on-chip oscillator is selected *2	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	LPCMRE0	Low-Power Timer Compare Match 0 Enable	0: Low-power timer compare match 0 is disabled 1: Low-power timer compare match 0 is enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

Note 1. Satisfy the condition that the frequency of the system clock (ICLK) and peripheral module clock (PCLKB) ≥ 4 × (the frequency of the low-power timer clock source).

Note 2. The IWDT-dedicated on-chip oscillator is supplied to the low-power timer. When modifying this bit, make sure that the IWDT-dedicated on-chip oscillator is oscillating stably.
When the IWDT-dedicated on-chip oscillator is used as the clock source for the low-power timer, set the OFS0.IWDTSLCSTP bit to 0 (counting stop is disabled) in IWDT auto-start mode operation, and set the IWDTCSTPR.SLCSTP bit to 0 (counting stop is disabled) in any other mode. Without this setting, the IWDT-dedicated on-chip oscillator will be stopped in software standby mode.

The LPTCR1 register is used to control the low-power timer.

LPCNTPSSEL[2:0] Bits (Low-Power Timer Clock Division Ratio Select)

These bits are used to select the count clock to be input to the low-power timer from among five divided clocks, which are obtained by dividing the clock source for the low-power timer.

Modify these bits while the low-power timer clock is stopped (LPTCR2.LPCNTSTP = 1).

Do not write to these bits while the low-power timer clock is being supplied (LPTCR2.LPCNTSTP = 0).

LPCNTCKSEL Bit (Low-Power Timer Clock Source Select)

This bit is used to select the sub-clock oscillator or IWDT-dedicated on-chip oscillator as the clock source for the low-power timer.

Modify this bit while the low-power timer clock is stopped (LPTCR2.LPCNTSTP = 1).

Do not write to this bit while the low-power timer clock is being supplied (LPTCR2.LPCNTSTP = 0)

LPCMRE0 Bit (Low-Power Timer Compare Match 0 Enable)

This bit enables or disables low-power timer compare match 0.

Set this bit to 1 and permit the low-power timer waking up from standby mode (LPWUCR.LPWKUPEN = 1) to make the low-power timer operate. If the MCU makes a transition to software standby mode with these settings, the ELC causes the MCU to wake up from software standby mode to normal operating mode when the low-power timer counter value matches the set value of the low-power compare register 0 (LPCMR0).

Modify this bit while the low-power timer counter is stopped (LPTCR3.LPCNTEN = 0).

Do not write to this bit while the low-power timer counter is counting (LPTCR3.LPCNTEN = 1).

Settings for the interrupt and ELC to initiate wakeup from software standby mode are required.

See section 17, Event Link Controller (ELC) for details on the ELC settings, and see section 14, Interrupt Controller (ICUb) for details on the interrupt settings.

An interrupt on low-power timer compare match 0 is generated only in software standby mode.

An interrupt on low-power timer compare match 0 is not generated in normal operating mode, sleep mode, and deep sleep mode.

1.2.2 Low-Power Timer Control Register 2 (LPTCR2)

Address(es): 0008 00B1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LPCNTSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	LPCNTSTP	Low-Power Timer Clock Supply Control	0: Low-power timer clock is supplied 1: Low-power timer clock is stopped	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

The LPTCR2 register is used to control supply of the clock signal to be used for the low-power timer.

LPCNTSTP Bit (Low-Power Timer Clock Supply Control)

This bit is used to supply or stop the clock to be used for the low-power timer. When this bit is set to 0, the clock signal is supplied to the low-power timer counter and divider.

1.2.3 Low-Power Timer Control Register 3 (LPTCR3)

Address(es): 0008 00B2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LPCNTRST	LPCNTEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LPCNTEN	Low-Power Timer Operation Control	0: Low-power timer counter stops 1: Low-power timer counter operates	R/W
b1	LPCNTRST	Low-Power Timer Counter Clear*1	• For writing 0: Writing has no effect 1: Divider and counter are cleared • For reading 0: Clearing is completed 1: Clearing in in progress	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

Note 1. After writing 1 to the LPCNTRST bit and confirming that its value is 0, wait for at least one cycle of the clock selected by the LPTCR1.LPCNTCKSEL bit before writing 1 to the LPCNTRST bit again.

The LPTCR3 register controls operations of the low-power timer counter and clears the division counter.

LPCNTEN Bit (Low-Power Timer Operation Control)

This bit is used to operate or stop the low-power timer counter and divider.

When this bit is set to 1 while the clock to be used for the low-power timer is being supplied (LPTCR2.LPCNTSTP = 0), the low-power timer counter and divider start to operate. Do not write to this bit while the low-power timer clock is stopped (LPTCR2.LPCNTSTP = 1).

Do not write 1 to the LPCNTRST bit while this bit is set to 1.

LPCNTRST Bit (Low-Power Timer Counter Clear)

This bit is used to clear the low-power timer counter and divider.

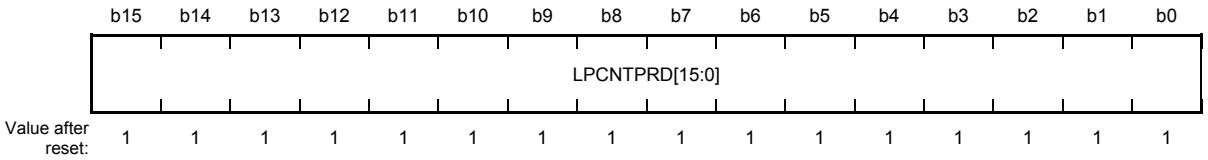
When this bit is set to 1 while the clock to be used for the low-power timer is being supplied (LPTCR2.LPCNTSTP = 0), the low-power timer counter and divider are cleared in synchronization with the clock to be used for the low-power timer. Once clearing is complete, this bit is automatically cleared to 0. Do not write to this bit while the low-power timer clock is stopped (LPTCR2.LPCNTSTP = 1).

When 1 is written to this bit, confirm that its value is 0 before proceeding with further processing.

Write to this bit while the low-power timer counter is stopped (LPCNTEN = 0).

1.2.4 Low-Power Timer Cycle Setting Register (LPTPRD)

Address(es): 0008 00B4h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	LPCNTPRD[15:0]	Low-Power Timer Cycle Setting	Set the low-power timer cycle. 0000h: Setting prohibited	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

The LPTPRD register is used to set the cycle of the low-power timer.

LPCNTPRD[15:0] Bits (Low-Power Timer Cycle Setting)

These bits are used to set the cycle of the low-power timer.

The cycle of the low-power timer is set to (the value in this register + 1) and calculated by the following formula:

Cycle of the low-power timer = Clock source cycle × division ratio × (LPCNTPRD[15:0] + 1)

When the timer counter value matches the set value, the counter is cleared to 0000h and continues counting.

This register cannot be set to 0000h.

Set this register while the low-power timer counter is stopped (LPTCR3.LPCNTEN = 0). Do not write to this register while the low-power timer counter is counting (LPTCR3.LPCNTEN = 1).

Table 1.2 and Table 1.3 list examples of setting the cycles of the low-power timer. These examples show the values closest to the cycles.

Table 1.2 Example of Low-Power Timer Cycle Settings for IWDT-Dedicated LOCO

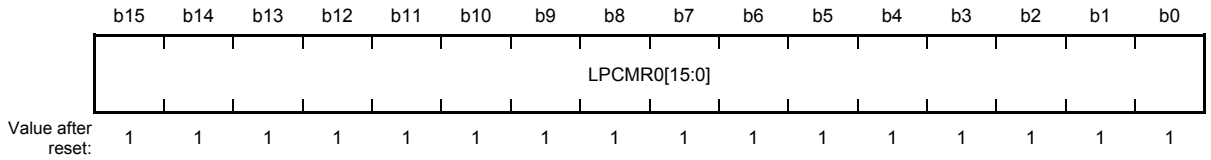
Division Setting / Cycle [ms]	2			4			8			16			32		
	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]
1	0006h	0.93	-6.67	0003h	1.07	6.67	0001h	1.07	6.67	—	—	—	—	—	—
2	000Dh	1.87	-6.67	0006h	1.87	-6.67	0003h	2.13	6.67	0001h	2.13	6.67	—	—	—
5	0024h	4.93	-1.33	0011h	4.80	-4.00	0008h	4.80	-4.00	0004h	5.33	6.67	0001h	4.27	-14.67
10	004Ah	10.00	0.00	0024h	9.87	-1.33	0011h	9.60	-4.00	0008h	9.60	-4.00	0004h	10.67	6.67
20	0095h	20.00	0.00	004Ah	20.00	0.00	0024h	19.73	-1.33	0011h	19.20	-4.00	0008h	19.20	-4.00
50	0176h	50.00	0.00	00BAh	49.87	-0.27	005Ch	49.60	-0.80	002Dh	49.07	-1.87	0016h	49.07	-1.87
100	02EDh	100.00	0.00	0176h	100.00	0.00	00BAh	99.73	-0.27	005Ch	99.20	-0.80	002Dh	98.13	-1.87
200	05DBh	200.00	0.00	02EDh	200.00	0.00	0176h	200.00	0.00	00BAh	199.47	-0.27	005Ch	198.40	-0.80
500	0EA4h	499.87	-0.03	0751h	499.73	-0.05	03A8h	499.73	-0.05	01D3h	499.20	-0.16	00E9h	499.20	-0.16
1000	1D4Ah	999.87	-0.01	0EA4h	999.73	-0.03	0751h	999.47	-0.05	03A8h	999.47	-0.05	01D3h	998.40	-0.16
2000	3A96h	1999.87	-0.01	1D4Ah	1999.73	-0.01	0EA4h	1999.47	-0.03	0751h	1998.93	-0.05	03A8h	1998.93	-0.05
5000	927Bh	5000.00	0.00	493Dh	5000.00	0.00	249Eh	5000.00	0.00	124Eh	4999.47	-0.01	0926h	4998.40	-0.03
10000	—	—	—	—	—	—	493Dh	10000.00	0.00	249Eh	10000.00	0.00	124Eh	9998.93	-0.01
20000	—	—	—	—	—	—	927Bh	20000.00	0.00	493Dh	20000.00	0.00	249Eh	20000.00	0.00
50000	—	—	—	—	—	—	—	—	—	B71Ah	50000.00	0.00	5B8Ch	49998.93	0.00

Table 1.3 Example of Low-Power Timer Cycle Settings for Sub-Clock Oscillator

Division Setting / Cycle [ms]	2			4			8			16			32		
	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]	Set Value	Value [ms]	Error [%]
1	000Fh	0.98	-2.34	0007h	0.98	-2.34	0003h	0.98	-2.34	0001h	0.98	-2.34	—	—	—
2	001Fh	1.95	-2.34	000Fh	1.95	-2.34	0007h	1.95	-2.34	0003h	1.95	-2.34	0001h	1.95	-2.34
5	0050h	4.94	-1.12	0027h	4.88	-2.34	0013h	4.88	-2.34	0009h	4.88	-2.34	0004h	4.88	-2.34
10	00A2h	9.95	-0.51	0050h	9.89	-1.12	0027h	9.77	-2.34	0013h	9.77	-2.34	0009h	9.77	-2.34
20	0146h	19.96	-0.21	00A2h	19.90	-0.51	0050h	19.78	-1.12	0027h	19.53	-2.34	0013h	19.53	-2.34
50	0332h	49.99	-0.02	0198h	49.93	-0.15	00CBh	49.80	-0.39	0065h	49.80	-0.39	0032h	49.80	-0.39
100	0665h	99.98	-0.02	0332h	99.98	-0.02	0198h	99.85	-0.15	00CBh	99.61	-0.39	0065h	99.61	-0.39
200	0CCBh	199.95	-0.02	0665h	199.95	-0.02	0332h	199.95	-0.02	0198h	199.71	-0.15	00CBh	199.22	-0.39
500	1FFFh	500.00	0.00	0FFFh	500.00	0.00	07FFh	500.00	0.00	03FFh	500.00	0.00	01FFh	500.00	0.00
1000	3FFFh	1000.00	0.00	1FFFh	1000.00	0.00	0FFFh	1000.00	0.00	07FFh	1000.00	0.00	03FFh	1000.00	0.00
2000	7FFFh	2000.00	0.00	3FFFh	2000.00	0.00	1FFFh	2000.00	0.00	0FFFh	2000.00	0.00	07FFh	2000.00	0.00
5000	—	—	—	9FFFh	5000.00	0.00	4FFFh	5000.00	0.00	27FFh	5000.00	0.00	13FFh	5000.00	0.00
10000	—	—	—	—	—	—	9FFFh	10000.00	0.00	4FFFh	10000.00	0.00	27FFh	10000.00	0.00
20000	—	—	—	—	—	—	—	—	—	9FFFh	20000.00	0.00	4FFFh	20000.00	0.00
50000	—	—	—	—	—	—	—	—	—	—	—	—	C7FFh	50000.00	0.00

1.2.5 Low-Power Timer Compare Register 0 (LPCMR0)

Address(es): 0008 00B8h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	LPCMR0[15:0]	Low-Power Timer Compare 0	Set the value of compare match 0 for comparison with the low-power timer counter.	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

The LPCMR0 register is used to set the value of compare match 0 for comparison with the low-power timer counter.

LPCMR0[15:0] Bit (Low-Power Timer Compare 0)

These bits are used to set the value of compare match 0 for comparison with the low-power timer counter.

Set the LPCMR0[15:0] bits to a value smaller than the value of the LPTPRD.LPCNTPRD[15:0] bits.

Set this register while the low-power timer counter is stopped (LPTCR3.LPCNTEN = 0). Do not write to this register while the low-power timer counter is counting (LPTCR3.LPCNTEN = 1).

1.2.6 Low-Power Timer Standby Wakeup Enable Register (LPWUCR)

Address(es): 0008 00BCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LPWKUPEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	LPWKUPEN	Low-Power Timer Standby Wakeup Enable	0: Wakeup from software standby mode using low-power timer is disabled 1: Wakeup from software standby mode using low-power timer is enabled	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

The LPWUCR register is used to enable the function that allows wakeup from software standby mode to normal mode when compare match 0 occurs in the low-power timer.

LPWKUPEN Bit (Low-Power Timer Standby Wakeup Enable)

This bit enables or disables the function that allows wakeup from software standby mode to normal mode when compare match 0 occurs in the low-power timer.

Set this bit while the low-power timer counter is stopped (LPTCR3.LPCNTEN = 0). Do not write to this bit while the low-power timer is counting (LPTCR3.LPCNTEN = 1).

1.3 Operation

1.3.1 Periodic Count Operation

The low-power timer is a 16-bit up-counter that operates regardless of the operating state*1.

Set the LPTCR1.LPCNTPSSEL[2:0] bits to select the divided clock and set the LPTCR1.LPCNTCKSEL bit to select the clock source. When the LPTCR2.LPCNTSTP bit is set to 0 and then the LPTCR3.LPCNTEN bit is set to 1, the low-power timer counter starts counting up with the selected clock signal.

When the low-power timer counter value matches the LPTPRD register value, the counter restarts counting up from 0000h.

After the LPTCR1.LPCMRE0 bit is set to 1 and the LPWUCR.LPWKUPEN bit are set to 1, when the low-power timer counter value matches the LPCMR0 register value in software standby mode, the MCU wakes up from software standby mode to normal operating mode via the ELC.

Figure 1.2 shows operation of the low-power timer and Figure 1.3 shows an example of initial settings.

Note 1. When the LPTCR1.LPCNTCKSEL bit is set to 1 (IWDT-dedicated on-chip oscillator selected), the counter stops because the selected clock is stopped in the low-power consumption state under the following settings:
"Counting stop is selected by setting the IWDT sleep mode count stop control bit in option function select register 0 (OFS0.IWDTSLCSTP) in IWDT auto-start mode" or "counting stop is selected by setting sleep mode count stop control bit in the IWDT count stop control register (IWDTCSTPR.SLCSTP) in any mode other than IWDT auto-start mode".

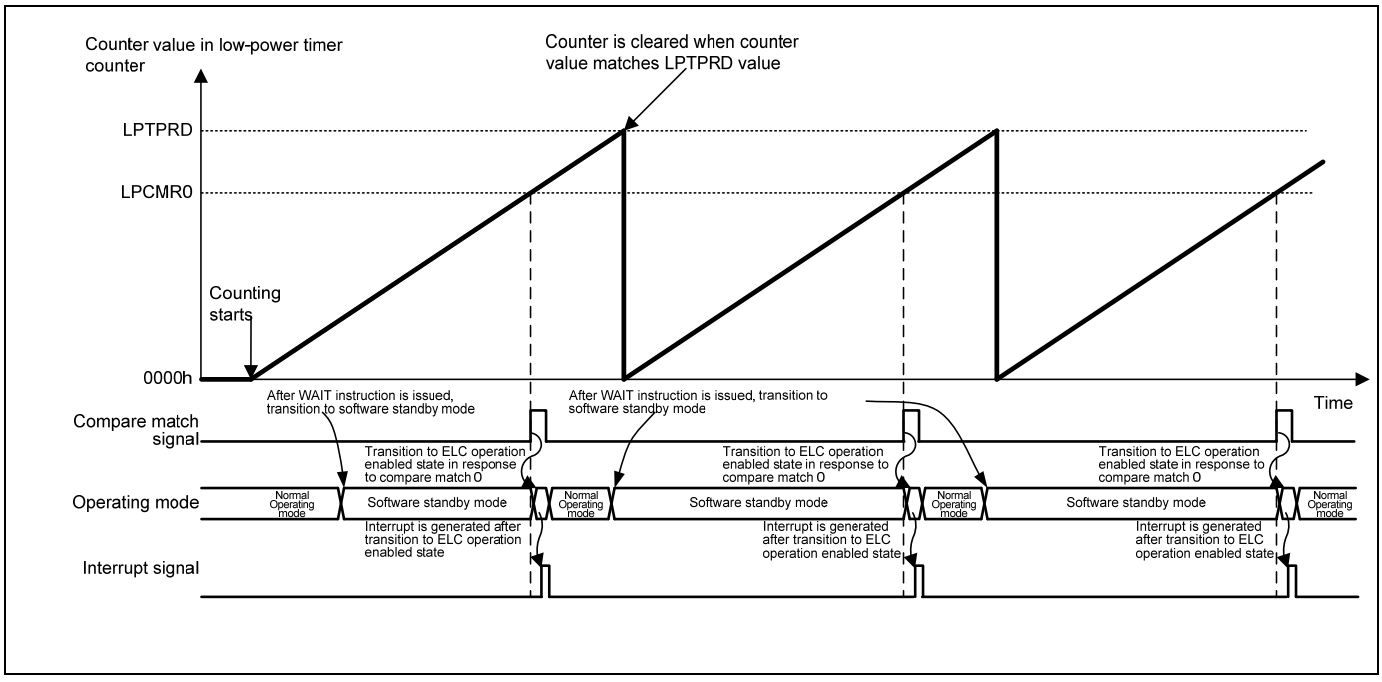


Figure 1.2 Operation of Low-Power Timer

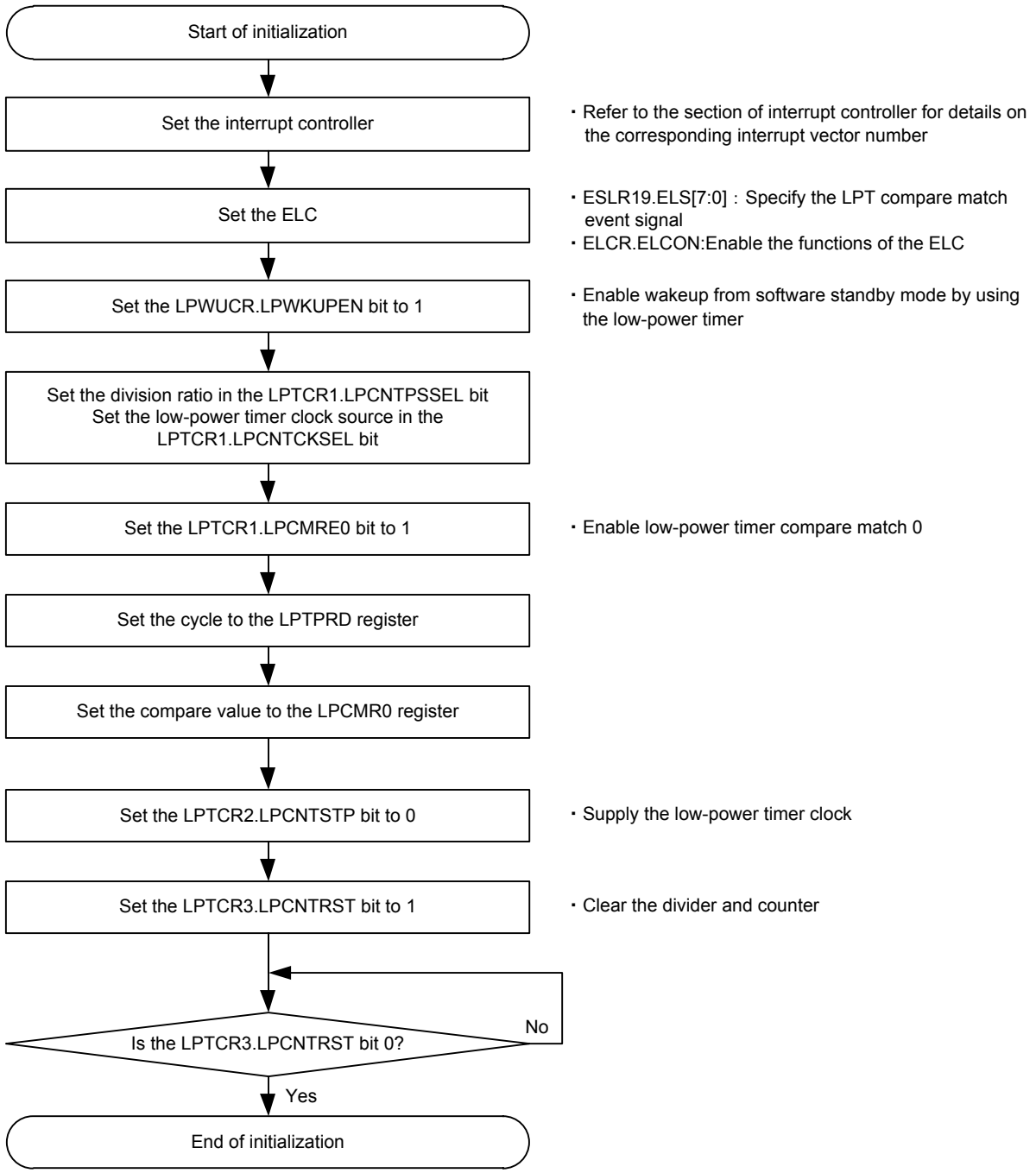


Figure 1.3 Example of Initial Settings

1.3.2 Count Timing of Low-Power Timer Counter

The LPTCR1.LPCNTPSSEL[2:0] bits are used to select the clock to be input to the low-power timer counter from among five divided clocks (1/2, 1/4, 1/8, 1/16, and 1/32), which are obtained by dividing the clock source for the low-power timer counter. Figure 1.4 shows the count timing of the low-power timer counter in this case.

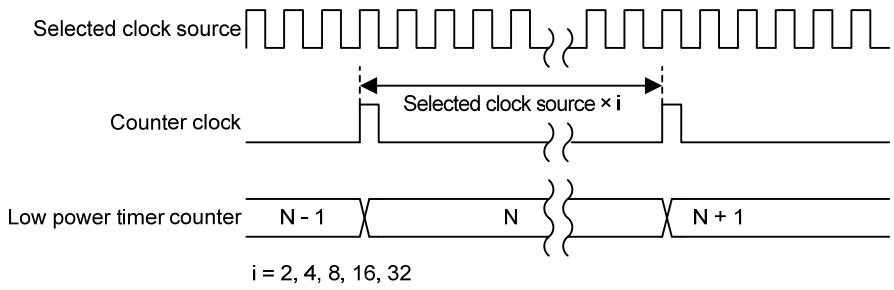


Figure 1.4 Count Timing of Low-Power Timer Counter

1.3.3 Clearing Timing of Low-Power Timer Counter

Writing 1 to the LPTCR3.LPCNTRST bit*1 clears the low-power timer counter.

This bit is automatically set to 0 when the clearing of the counter is completed.

Figure 1.5 shows the clearing timing of the low-power timer counter in this case.

Note 1. Write to the LPTCR3.LPCNTRST bit while the counter is stopped (LPTCR3.LPCNTEN = 0).

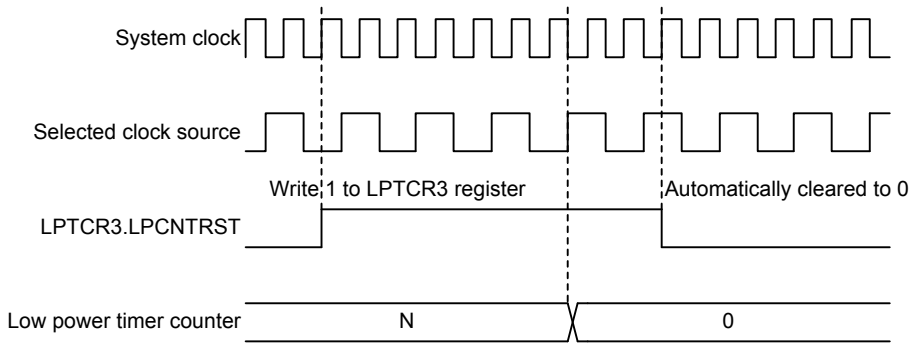


Figure 1.5 Reset Timing of Low-Power Timer Counter

1.4 Release from Software Standby Mode by an Interrupt Signal through the Event Link Controller (ELC)

The low-power timer can be set up to use the event link controller (ELC) to output an event signal upon LPT compare match 0 (only in software standby mode).

This is done by setting LPT compare match with the ELSR19 register of the event link controller (ELC), leading to LPT compare-match interrupts acting as event signals that return the MCU to normal operating mode from software standby mode.

1.5 Usage Notes

1.5.1 Notes on Transition to Software Standby Mode

When the MCU has returned to normal operating mode from software standby mode, and is then to be returned to software standby mode, wait for at least 1 cycle of the clock selected by the LPTCR1.LPCNTCKSEL bit before executing the WAIT instruction.

2. Changes in RX113 Group User's Manual: Hardware Rev1.02

Tables 11.2, 12.1, 14.3, 17.2, and 17.3 are changed as follows.

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Table 11.2 Operating Conditions of Each Power Consumption Mode

	Sleep Mode	Deep Sleep Mode	Software Standby Mode
		omitted	
Low-power timer (LPT)	Operating possible	Operating possible	Operating possible
		omitted	

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Table 12.1 Association between PRCR Bits and Registers to be Protected

PRCR Bit	Register to be Protected
	omitted
PRC2	・Registers related to the low-power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
	omitted

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Table 14.3 Interrupt Vector Table (3/7)

Source of Interrupt Request Generation	Name	Vector No.	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
-				*omitted*					-	-
ELC	ELSR19I	80	0140h	Edge	○	×	○	IER0A.IEN0	IPR080	-
-				*omitted*						

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Table 17.2 Correspondence between the ELSRn Register and the Peripheral Functions

Register Name	Peripheral Function (Module)
	omitted
ELSR19	ICU (LPT-specific interrupt)*2
	Omitted

Note 2. Specify 0101 1101b (5Dh) as an event number.

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Table 17.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] bits and Signal Numbers

ELS[7:0] Bit Value	Peripheral Modules	Event Signal Set in ELSRn
		omitted
5Dh	LPT	LPT compare match
		omitted