Date: Jan. 28, 2015

RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A238A/E	Rev.	1.00
Title	Deletion of Specifications and Errata for R32C/116A Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	R32C/116A Group	Lot No.	Reference Document	R32C/116A Group User's Manual: Hardware Rev. 1.10 (R01UH0213EJ0110)		

This document describes deletion of specifications and errata for the R32C/116A Group User's Manual: Hardware, Rev. 1.10.

1. Deletion of Specifications

Development of products on the planning phase in Table 1.5 is discontinued. Accordingly, specifications for the N version are deleted from the Operating Temperature in Tables 1.2, 1.4, and 29.2, and the Temperature Code in Figure 1.1.

2. Errata

The corrections are indicated in red in the list below.

- Page 1 of 541, expression "I^2C" in line 9 of 1.1 is modified as follows:
  "I^2C-bus interface"

- Page 157 of 541, description in lines 9 and 10 of chapter 12 is modified as follows:
  "One divides the on-chip oscillator clock by 1, 2, 4 or 8; the other divides the peripheral bus clock by 16 or 128."

- Page 184 of 541, descriptions in Figure 14.5 is modified as follows:
  "The figure below applies under the following conditions:
  memory-to-memory transfer; incrementing source address; non-incrementing destination address; single transfer mode; transfer complete interrupt generated after 2 transfers (transfer counter = 2); no chain transfer"

- Page 191 of 541, description of the third bullet point of 16.1 is corrected as follows:
  "One-shot timer mode: The timer outputs a pulse after a trigger input until the counter reaches 0000h"

- Page 196 of 541, typos "b2 b3", "b4 b5", and "b6 b7" in Figure 16.9 are corrected as follows:
  "b3 b2", "b5 b4", and "b7 b6"

- Page 203 of 541, typo "$\overline{INT}$" in Note 1 of Figures 16.13 and 16.14 is corrected as follows:
  "$\overline{INT2}$"

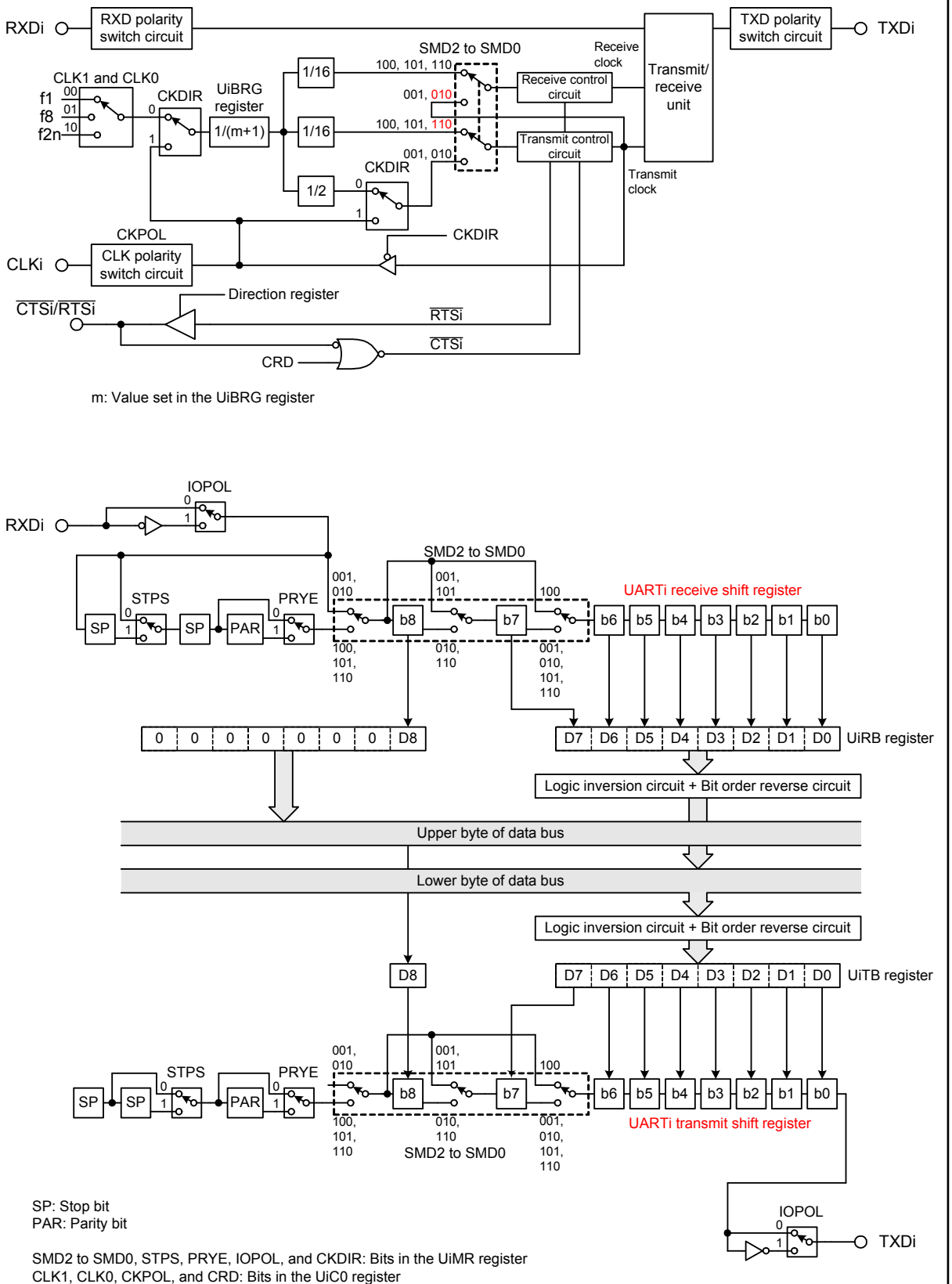
•Page 207 of 541, bit symbol “TAiS” in the Function column for the MR2 bit in Figure 16.16 is corrected as follows:

“TAiOS”

•Pages 240 to 291 of 541, terms in chapter 18 are corrected as follows:

Before Correction	After Correction	Figure/Table/Section Number
receive register	receive shift register	Figures 18.1, 18.2, 18.22, 18.28 Tables 18.2, 18.5, 18.11, 18.14 Section 18.3.8
transmit register	transmit shift register	Figures 18.1, 18.2, 18.21, 18.22, 18.26, 18.27 Tables 18.2 (2 corrections), 18.3, 18.4, 18.5 (2 corrections), 18.6, 18.7, 18.10, 18.14 (2 corrections), 18.15 Section 18.3.8 (3 corrections)
SS function	slave select function	Figure 18.13 (3 corrections) Table 18.14 Sections 18.4.1, 18.4.1.1, 18.4.1.2
BRG	UiBRG	Table 18.8 (3 corrections)
restart condition	repeated START condition	Figure 18.14 Table 18.10 Sections 18.3.2 (2 corrections), 18.5.3

•Page 241 of 541, positions of “010” for bits SMD2 to SMD0 in Figure 18.1 are corrected as follows:



•Page 251 of 541, expression “baud rate generator count source” in the function of bits DL0 to DL2 in Figure 18.13 is corrected as follows:

“count source for the UiBRG register”

•Pages 258, 259, 266, 267, 276, 286 of 541, descriptions in Function of the UiBRG register in Tables 18.3, 18.4, 18.6, 18.7, 18.10, and 18.15 are modified as follows:

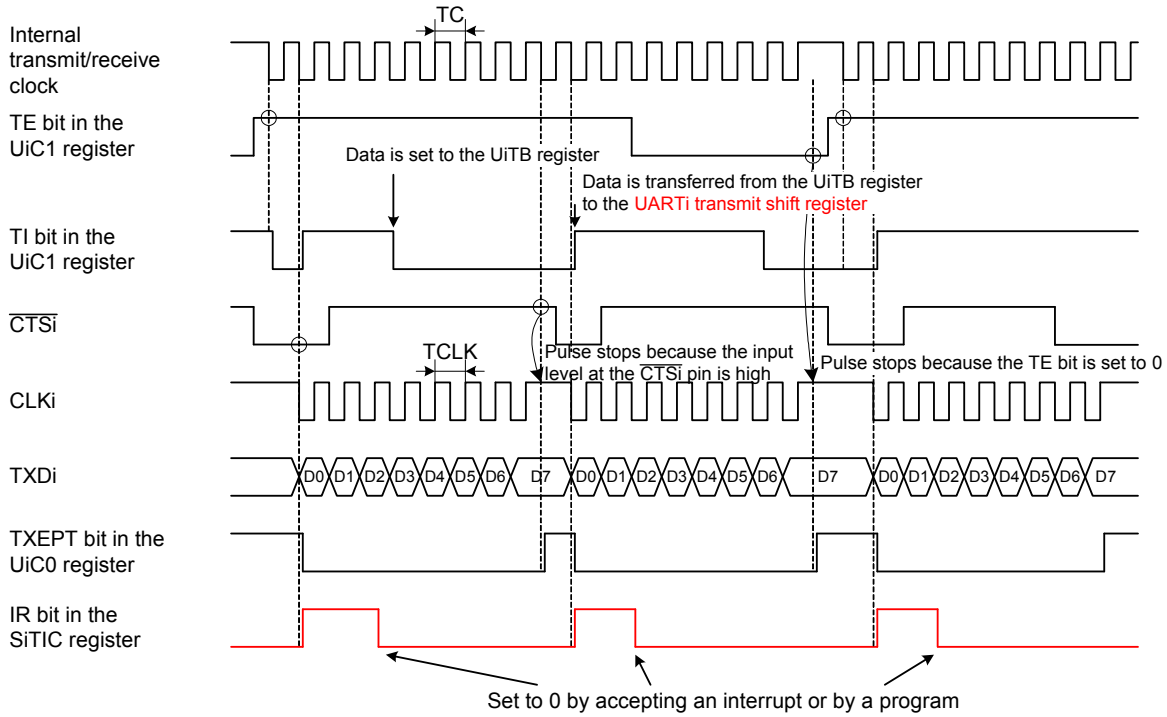
“Set the divide ratio according to the bit rate”

•Pages 259, 267 of 541, description for (b7 to b4) to registers UiC1 and U78CON in Tables 18.4 and 18.7 is added as follows:

“(b7 to b4) Set the bits to 0000b”

•Page 260 of 541, waveform of the IR bit in Figure 18.21 is corrected as follows:

Transmit timing (when selecting an internal clock)



This figure applies under the following conditions:

- The CKDIR bit in the UiMR register is 0 (internal clock).
- The CRD bit in the UiC0 register is 0 (CTS function enabled).
- The CKPOL bit in the UiC0 register is 0 (output transmit data on the falling edge of the transmit/receive clock).
- The UiIRS bit in registers UiC1, U78CON, and U910CON is 0 (an interrupt request is generated when the transmit buffer is empty).

TC = TCLK = 2(m + 1)/fx

fx: UiBRG count source frequency (f1, f8, or f2n)

m: Value setting in the UiBRG register

•Page 262 of 541, descriptions in 18.1.1 are modified as follows:
"When a transmit/receive error occurs in synchronous serial interface mode, follow the procedures below to perform a reset:

(1) Set the TE bit to 0 (transmission disabled) and the RE bit to 0 (reception disabled) in the UiC1 register (i = 0 to 10).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set again bits SMD2 to SMD0 to either of 001b, 101b, or 110b.
(4) Set the TE bit to 1 (transmission enabled) and the RE bit to 1 (reception enabled) in the UiC1 register."

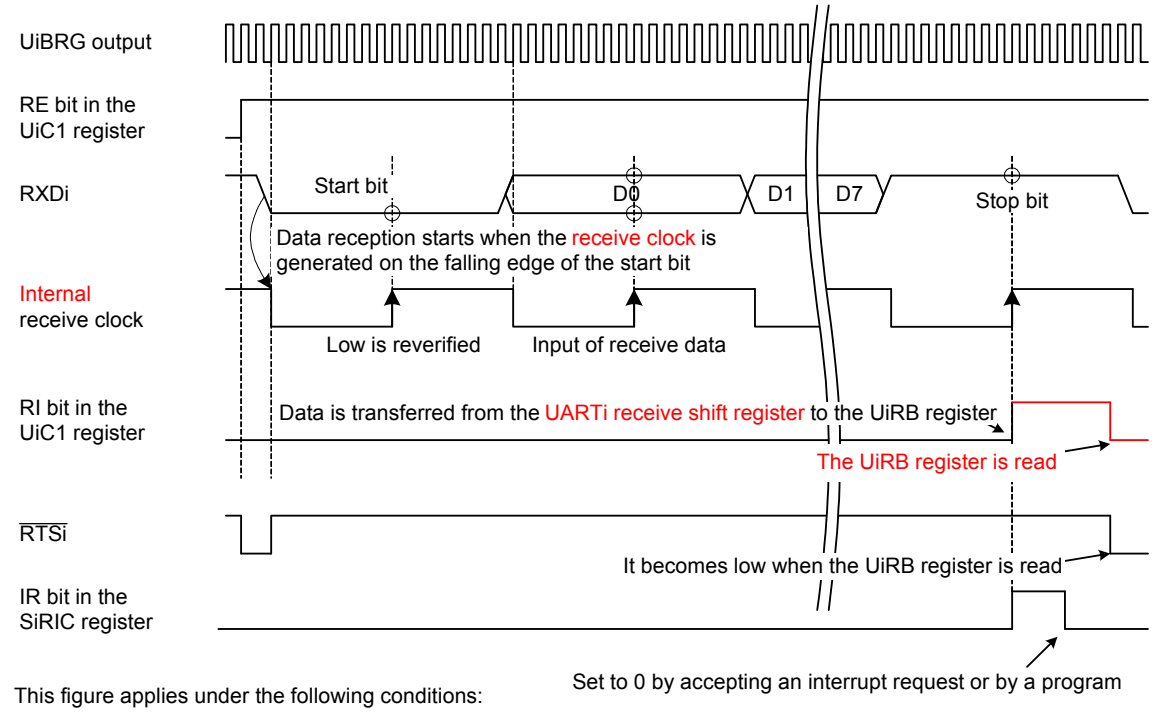
•Page 264 of 541, the following description is added to line 3 of 18.1.6:
"after the last bit is transmitted"

•Page 267 of 541, description for (b7) to the UiMR register in Table 18.7 is added as follows:
"(b7) Set the bit to 0"

•Pages 268, 269 of 541, description "Internal transmit/receive clock" in Figures 18.26 and 18.27 is corrected as follows:
"Internal transmit clock"

•Page 270 of 541, Figure 18.28 is corrected as follows:

Example of data receive timing when the character length is 8-bit (parity disabled, 1 stop bit)



This figure applies under the following conditions:
- The PRYE bit in the UiMR register is 0 (parity disabled).
- The STPS bit in the UiMR register is 0 (1 stop bit).

•Page 271 of 541, descriptions in 18.2.2 are modified as follows:
"When a transmit/receive error occurs in UART mode, follow the procedure below to perform a reset:

(1) Set the TE bit to 0 (transmission disabled) and the RE bit to 0 (reception disabled) in the UiC1 register (i = 0 to 10).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set again bits SMD2 to SMD0 to either of 001b, 101b, or 110b.
(4) Set the TE bit to 1 (transmission enabled) and the RE bit to 1 (reception enabled) in the UiC1 register.

•Page 274 of 541, descriptions for the Interrupt request generating timing in Table 18.9 are modified as follows:

Interrupt request generating timing	• START condition is detected • STOP condition is detected • ACK (acknowledge) is detected, or reception is completed • NACK (not-acknowledge) is detected, or transmission is completed

•Page 276 of 541, description for (b6 to b4) to the UiMR register in Table 18.10 is added as follows:
"(b6 to b4) Set the bits to 000b"

•Page 291 of 541, description for suspending and resuming communication is added to 18.5.4 as follows:

"**18.5.4 Reset Procedure** or Suspend/Resume Procedure
Operations which result in communication errors such as rewriting function select registers during transmission/reception should not be performed. Follow the procedure below to reset the internal circuit once the communication error occurs in the following cases: when the operation above is performed by a receiver or transmitter or when a bit slip is caused by noise.
Also follow the procedure below when suspending and resuming communication in an emergency."

•Page 404 of 541, descriptions in lines 5 and 6 of 26. I/O Pins are modified as follows:
"The pull-up resistors are enabled for every group of four pins. However, when a pin functions as an output pin, a pull-up resistor is disabled regardless of the register settings."

•Page 404 of 541, description in the last paragraph of 26. I/O Pins is corrected as follows:
"The input-only port P8_5 shares a pin with $\overline{\text{NMI}}$ and has neither function select register nor the corresponding direction bit. Port P14_1 also functions as an input-only port. The function select register and bit 1 in the PD14 register are reserved. Port P9 is protected from unexpected write accesses by the PRC2 bit in the PRCR register (refer to 10. "Protection")."

•Pages 437, 438 of 541, description in Note 2 of Tables 26.2 and 26.3 are modified as follows:
"When configuring as an output port to release the pin open, it remains as an input port until it is set as an output port after a reset is released. Therefore, while it remains as an input port, the power supply current may increase due to the undefined voltage level of the pin. In addition, the direction register value may change due to noise or program runaway caused by the noise. To avoid these situations, reconfigure the direction register regularly by software, which may achieve higher program reliability."

•Pages 437, 438 of 541, description "addresses: 03E2h, 03E3h, 03E6h and 03E7h" in Note 4 of Tables 26.2 and 26.3 is modified as follows:
"registers PD16 and PD17, PD18, and PD19"

•Page 497, 500, 510, 513, 530 of 541, expression "restart condition" in Tables 28.34, 28.39, 28.40, 28.60, 28.65, 28.66, and line 1 of 29.9.3 is modified as follows:
"repeated START condition"

• Page 531 of 541, description for suspending and resuming communication is added to 29.9.4 as follows:

"**29.9.4 Reset Procedure** or Suspend/Resume Procedure

Operations which result in communication errors such as rewriting function select registers during transmission/reception should not be performed. Follow the procedure below to reset the internal circuit once the communication error occurs in the following cases: when the operation above is performed by a receiver or transmitter or when a bit slip is caused by noise.

Also follow the procedure below when suspending and resuming communication in an emergency."