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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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# RENESAS TECHNICAL UPD

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Product Category	MPU&MCU, MCMs	Document No.	TN-SH7-519A/EA	Rev.	1.0
Title	Data corruption in OC RAM mode in cache enhanced mode	Information Category	Usage Limitation		
Applicable Product	SH7750R SH7751R SH7760 SH-4 core use product	Lot No.	Reference Document	SH7751 series hardware manual ADE-602-201 SH7750 series hardware manual ADE-602-124 SH7760 series hardware manual ADE-602-291 Other SH-4 documents	
		All			

## 1. Summary

Internal RAM data may be updated incorrectly when OC RAM mode is specified in the cache enhanced mode. The condition and the workaround are described below.

## 2. Contents

When the following conditions 1 – 4 are satisfied at the same time, the internal RAM data may be corrupted.

- Cache enhanced mode is specified (CCR.EMODE=1).
- OC RAM mode is specified, where OC is used as half-size cache and half-size internal RAM (CCR.ORA=1).
- An exception or an interruption occurs. Note that this condition includes breaks by a debugger generated by swapping an original instruction into TRAPA instruction or illegal instruction code H'FFFD.
- There exists a store instruction (MOV, FMOV, AND.B, OR.B, XOR.B, MOVCA.L, STC.L, STS.L) to the internal RAM area (address between H'7C000000 and H'7FFFFFFF), within 4 instructions after the exception or the interruption described in the condition no.3. This condition includes a case where a store instruction to the internal RAM area generates an exception.

What happened by the problem is

wrong 8-byte-data are written into the internal RAM area that is mapped by an 8-byte-boundary address different by H'2000 from the address accessed by the store instruction described in the condition no.3. For example, a long word store instruction to address H'7C000204 may corrupt 8 bytes in the internal RAM mapped by H'7C002200 – H'7C002207.

## 3. Examples

Example 1: A store instruction to the internal RAM area within 4 instructions after an instruction causing a TLB miss exception

MOV.L #H'0C400000, R0	R0 is an address causing a TLB miss
MOV.L #H'7C000204, R1	R1 is mapped onto internal RAM
MOV.L @R0,R2	TLB miss exception occurs
NOP	1st word
NOP	2nd word
NOP	3rd word
MOV.L R3, @R1	Store instruction to the internal RAM

Example 2: A store instruction to the internal RAM area within 4 instructions after an interruption is accepted

MOV.L #H'7C002000, R1	R1 is mapped onto internal RAM
MOV.L #H'12345678, R0	An interruption is accepted after this instruction
NOP	1st word
NOP	2nd word
NOP	3rd word
MOV.L R0, @R1	Store instruction to the internal RAM

Example 3: TRAPA or H'FFFD swaps an instruction and generates a break by a debugger

Original Instructions	After swapped	Notes
MOV.L #H'7C000000, R0	MOV.L #H'7C000000, R0	
ADD R0,R0	TRAPA #H'01	R0 is not mapped onto internal RAM in original instructions
MOV.L R1, @R0	MOV.L R1, @R0	ADD is swapped by TRAPA and R0 is mapped onto internal RAM. This store is cancelled but 2LW from H'7C002000 is corrupted.

4. Workaround

It is possible to avoid this problem by either of the following workaround when OC RAM mode is specified in the cache enhanced mode.

1. Only 8k bytes out of 16k bytes internal RAM area can be used. In this case, it is forbidden to use two RAM areas that have the same address [12:0] and the different address [13]. For example, use 8k byte RAM area between H'7C000000 – H'7C001FFF or between H'7C001000 – H'7C002FFF.

[Note] When instructions are swapped to generate a break by a debugger, the following memory access instructions may specify a forbidden address by this workaround that is mapped onto the other half 8kB internal RAM area. The problem still happens in this case, but this phenomenon only occurs at a debugging phase using a break by swapping instructions. A hardware break where instructions are not swapped can be used for this purpose without any problem.

2. It should be guaranteed that no exception and interruption is occurred within four instructions before a store instruction to the internal RAM area. This can be adopted, for example, when the internal RAM is used as a data table that is accessed only by load instructions and store instructions to the internal RAM area exist only for the table generation. In this case, SR.BL should be set to 1 in order to mask all the interruptions. Exceptions such as TLB misses should also be avoided during the table generation.

[Note] The problem still happens when instructions are swapped to generate a break by a debugger, but this phenomenon only occurs at a debugging phase. A hardware break where instructions are not swapped can be used for this purpose without any problem