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RENESAS TECHNICAL UPDATE

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Product category	MPU & MCU	Document No.	TN-RX*-A092A/E	Rev.	1.00
Title	Corrections to Descriptions for the Boundary Scan Register in the RX630 Group User's Manual: Hardware		Information category	Technical information	
Applicable products	RX630 Group	Lot no. All	Reference document	RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040JJ0150)	

This document describes corrections to descriptions in the "1.Overview" and "44.Boundary Scan" of the RX630 Group User's Manual: Hardware.

1. Note 2 of the Table 1.3 List of Products is corrected as follows (additions are underlined):

Note 2.The sub-clock oscillator and real-time clock and boundary scan have different specifications. For details, see section 11.2.8, Sub-Clock Oscillator Wait Control Register (SOSCWTCR), section 28.2.19, RTC Control Register 3 (RCR3), and section 44.2.4. Boundary Scan Register (JTBSR).

2. Table 44.6 Boundary Scan Register 177-pin TFLGA/176-pin LFBGA (3/10) is corrected as follows (changes are underlined):

(Before)

Pin No	Pin Name	Input/Output	Bit Name
⋮	⋮	⋮	⋮
N8	PL2	Output	311
		Output enable	310
		Input	309
M6	P55	Output	308
		Output enable	307
		Input	306

(After)

Pin No	Pin Name	Input/Output	Bit Name
⋮	⋮	⋮	⋮
N8	PL2	Output	311
		Output enable	310
			309
N7	P55	Output	308
		Output enable	307
		Input	306

3. Table 44.7 Boundary Scan Register 145-pin TFLGA is corrected as follows (changes are underlined):

145-pin TFLGA (1/8)

From TDI				
Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
B3	P05	Output	417	339
		Output enable	416	338
		Input	415	337
D3	P03	Output	414	336
		Output enable	413	335
		Input	412	334
C2	P02	Output	411	333
		Output enable	410	332
		Input	409	331
D4	P01	Output	408	330
		Output enable	407	329
		Input	406	328
D1	P00	Output	405	327
		Output enable	404	326
		Input	403	325
D2	PF5	Output	402	324
		Output enable	401	323
		Input	400	322
E3	PJ5	Output	399	321
		Output enable	398	320
		Input	397	319
F3	PJ3	Output	396	318
		Output enable	395	317
		Input	394	316
H4	P35	Input	393	315
J2	P33	Output	392	314
		Output enable	391	313
		Input	390	312
J3	P32	Output	389	311
		Output enable	388	310
		Input	387	309
L1	P25	Output	386	308
		Output enable	385	307
		Input	384	306
L4	P24	Output	380	305
		Output enable	379	304
		Input	378	303
L2	P23	Output	374	302
		Output enable	373	301
		Input	372	300
M1	P22	Output	371	299
		Output enable	370	298
		Input	369	297

145-pin TFLGA (2/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
N1	P21	Output	368	296
		Output enable	367	295
		Input	366	294
N2	P20	Output	359	287
		Output enable	358	286
		Input	357	285
M2	P17	Output	356	284
		Output enable	355	283
		Input	354	282
N3	P87	Output	353	281
		Output enable	352	280
		Input	351	279
L3	P16	Output	350	278
		Output enable	349	277
		Input	348	276
M3	P86	Output	347	275
		Output enable	346	274
		Input	345	273
K4	P15	Output	344	272
		Output enable	343	271
		Input	342	270
N4	P14	Output	341	269
		Output enable	340	268
		Input	339	267
L5	P13	Output	335	266
		Output enable	334	265
		Input	333	264
M4	P12	Output	332	263
		Output enable	331	262
		Input	330	261
L6	P56	Output	320	260
		Output enable	319	259
		Input	318	258
N7	P55	Output	308	257
		Output enable	307	256
		Input	306	255
K5	P54	Output	305	254
		Output enable	304	253
		Input	303	252
K6	P53	Output	302	251
		Output enable	301	250
		Input	300	249

145-pin TFLGA (3/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
L7	P52	Output	296	248
		Output enable	295	247
		Input	294	246
K7	P51	Output	293	245
		Output enable	292	244
		Input	291	243
M7	P50	Output	290	242
		Output enable	289	241
		Input	288	240
L8	P83	Output	287	239
		Output enable	286	238
		Input	285	237
N9	PC7	Output	284	236
		Output enable	283	235
		Input	282	234
M8	PC6	Output	281	233
		Output enable	280	232
		Input	279	231
L9	PC5	Output	278	230
		Output enable	277	229
		Input	276	228
N10	P82	Output	275	227
		Output enable	274	226
		Input	273	225
M9	P81	Output	272	224
		Output enable	271	223
		Input	270	222
K9	P80	Output	269	221
		Output enable	268	220
		Input	267	219
L10	PC4	Output	266	218
		Output enable	265	217
		Input	264	216
N11	PC3	Output	263	215
		Output enable	262	214
		Input	261	213
M10	P77	Output	260	212
		Output enable	259	211
		Input	258	210
K10	P76	Output	257	209
		Output enable	256	208
		Input	255	207
L11	PC2	Output	254	206
		Output enable	253	205
		Input	252	204

145-pin TFLGA (4/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
N12	P75	Output	251	203
		Output enable	250	202
		Input	249	201
N13	P74	Output	248	200
		Output enable	247	199
		Input	246	198
M12	PC1	Output	245	197
		Output enable	244	196
		Input	243	195
M13	PL1	Output	242	194
		Output enable	241	193
		Input	240	192
M11	PC0	Output	239	191
		Output enable	238	190
		Input	237	189
L13	PL0	Output	236	188
		Output enable	235	187
		Input	234	186
L12	P73	Output	233	185
		Output enable	232	184
		Input	231	183
K11	PB7	Output	230	182
		Output enable	229	181
		Input	228	180
K12	PB6	Output	227	179
		Output enable	226	178
		Input	225	177
K13	PB5	Output	224	176
		Output enable	223	175
		Input	222	174
J11	PB4	Output	221	173
		Output enable	220	172
		Input	219	171
J10	PB3	Output	218	170
		Output enable	217	169
		Input	216	168
J12	PB2	Output	215	167
		Output enable	214	166
		Input	213	165
J13	PB1	Output	212	164
		Output enable	211	163
		Input	210	162
H10	P72	Output	209	161
		Output enable	208	160
		Input	207	159

145-pin TFLGA (5/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
H11	P71	Output	206	158
		Output enable	205	157
		Input	204	156
H12	PB0	Output	200	155
		Output enable	199	154
		Input	198	153
H13	PA7	Output	194	152
		Output enable	193	151
		Input	192	150
G11	PA6	Output	191	149
		Output enable	190	148
		Input	189	147
G10	PA5	Output	188	146
		Output enable	187	145
		Input	186	144
G13	PA4	Output	185	143
		Output enable	184	142
		Input	183	141
F10	PA3	Output	182	140
		Output enable	181	139
		Input	180	138
F13	PA2	Output	176	137
		Output enable	175	136
		Input	174	135
F12	PA1	Output	170	134
		Output enable	169	133
		Input	168	132
E10	PA0	Output	164	131
		Output enable	163	130
		Input	162	129
E13	P67	Output	158	128
		Output enable	157	127
		Input	156	126
E11	P66	Output	152	125
		Output enable	151	124
		Input	150	123
E12	P65	Output	146	122
		Output enable	145	121
		Input	144	120
D10	PE7	Output	143	119
		Output enable	142	118
		Input	141	117
D13	PE6	Output	140	116
		Output enable	139	115
		Input	138	114

145-pin TFLGA (6/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
D11	PK5	Output	137	113
		Output enable	136	112
		Input	135	111
C12	P70	Output	134	110
		Output enable	133	109
		Input	132	108
C13	PK4	Output	131	107
		Output enable	130	106
		Input	129	105
D12	PE5	Output	128	104
		Output enable	127	103
		Input	126	102
B13	PE4	Output	125	101
		Output enable	124	100
		Input	123	99
A13	PE3	Output	122	98
		Output enable	121	97
		Input	120	96
B12	PE2	Output	119	95
		Output enable	118	94
		Input	117	93
A12	PE1	Output	116	92
		Output enable	115	91
		Input	114	90
C11	PE0	Output	113	89
		Output enable	112	88
		Input	111	87
D9	P64	Output	110	86
		Output enable	109	85
		Input	108	84
C10	P63	Output	107	83
		Output enable	106	82
		Input	105	81
A11	P62	Output	104	80
		Output enable	103	79
		Input	102	78
B11	P61	Output	101	77
		Output enable	100	76
		Input	99	75
A10	PK3	Output	98	74
		Output enable	97	73
		Input	96	72
D8	P60	Output	95	71
		Output enable	94	70
		Input	93	69

145-pin TFLGA (7/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
B10	PK2	Output	92	68
		Output enable	91	67
		Input	90	66
C9	PD7	Output	89	65
		Output enable	88	64
		Input	87	63
A9	PD6	Output	83	62
		Output enable	82	61
		Input	81	60
D7	PD5	Output	77	59
		Output enable	76	58
		Input	75	57
B9	PD4	Output	74	56
		Output enable	73	55
		Input	72	54
C8	PD3	Output	68	53
		Output enable	67	52
		Input	66	51
A8	PD2	Output	56	50
		Output enable	55	49
		Input	54	48
C7	PD1	Output	50	47
		Output enable	49	46
		Input	48	45
B8	PD0	Output	44	44
		Output enable	43	43
		Input	42	42
D6	P93	Output	41	41
		Output enable	40	40
		Input	39	39
A7	P92	Output	38	38
		Output enable	37	37
		Input	36	36
B7	P91	Output	35	35
		Output enable	34	34
		Input	33	33
A6	P90	Output	32	32
		Output enable	31	31
		Input	30	30
B6	P47	Output	29	29
		Output enable	28	28
		Input	27	27
C5	P46	Output	26	26
		Output enable	25	25
		Input	24	24

145-pin TFLGA (8/8)

Pin No	Pin Name	Input/Output	Bit Name (Note1)	Bit Name (Note2)
A5	P45	Output	23	23
		Output enable	22	22
		Input	21	21
E5	P44	Output	20	20
		Output enable	19	19
		Input	18	18
B5	P43	Output	17	17
		Output enable	16	16
		Input	15	15
A4	P42	Output	14	14
		Output enable	13	13
		Input	12	12
C4	P41	Output	11	11
		Output enable	10	10
		Input	9	9
A3	P40	Output	8	8
		Output enable	7	7
		Input	6	6
A2	P07	Output	5	5
		Output enable	4	4
		Input	3	3
To TDO				

Note1. Products to which Note2 is not given in “Table 1.3 List of Products”.
Note2. Products to which Note2 is given in “Table 1.3 List of Products”.