

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RL*-A0098A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L13 Descriptions in the User's Manual: Hardware Rev. 2.10 Changed		Information Category	Technical Notification	
Applicable Product	RL78/L13 Group	Lot No.	Reference Document	RL78/L13 User's Manual: Hardware Rev. 2.10 R01UH0382EJ0210 (Aug 12,2016)	
		All lots			

This document describes misstatements found in the RL78/L13 User's Manual: Hardware Rev. 2.10 (R01UH0382EJ0210).

## Corrections

Applicable Item	Applicable Page	Contents
5.4.4 Low-speed on-chip oscillator	Page 169	Incorrect descriptions revised
7.9.2 Cautions when using the counter restart trigger	Page 386	Incorrect descriptions revised
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22.2 States of Operation During Reset Periods	Page 891	Incorrect descriptions revised
27.2 Format of User Option Byte	Page 939	Incorrect descriptions revised

## Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0409EJ0210	
1	5.4.4 Low-speed on-chip oscillator		Page 169	Page 3
2	7.9.2 Cautions when using the counter restart trigger		Page 386	Page 4
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~~Incorrect: Bold with underline~~; Correct: Gray hatched

**Revision History**

RL78/L1C Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0098A/E	Feb. 3, 2021	First edition issued Corrections No.1 to No.8 revised (this document)

### 1. 5.4.4 Low-speed on-chip oscillator (p.169)

Incorrect:

A low-speed on-chip oscillator is incorporated in the RL78/L13.  
The low-speed on-chip oscillator clock is used only as the clock for the watchdog timer, real-time clock 2, 12-bit interval timer, and the LCD controller/driver. The low-speed on-chip oscillator clock cannot be used as the CPU clock.

~~This clock operates when either bit 4 (WDTON) of the option byte (000C0H) or bit 4 (WUTMMCK0) of the subsystem clock supply mode control register (OSMC), or both, are set to 1.~~

~~As long as the watchdog timer is not operating and WUTMMCK0 is not zero, the low-speed on-chip oscillator continues oscillating. Note that only when the watchdog timer is operating and the WUTMMCK0 bit is 0, oscillation of the low-speed on-chip oscillator will stop while the WDSTBYON bit is 0 and operation is in the HALT, STOP, or SNOOZE mode. The low-speed on-chip oscillator clock does not stop even if a program loop that stops the system occurs while the watchdog timer is operating.~~

Correct:

A low-speed on-chip oscillator is incorporated in the RL78/L13.  
The low-speed on-chip oscillator clock is used only as the clock for the watchdog timer, real-time clock 2, 12-bit interval timer, and the LCD controller/driver. The low-speed on-chip oscillator clock cannot be used as the CPU clock.

The low-speed on-chip oscillator runs while the watchdog timer is operating or when the setting of bit 4 (WUTMMCK0) in the subsystem clock supply mode control register (OSMC) is 1.

The low-speed on-chip oscillator is stopped when the watchdog timer is stopped and WUTMMCK0 is set to 0.

2. 7.9.2 Cautions when using the counter restart trigger (p.386)

Incorrect:

(1) Using external interrupts (INTP0 to INTP7)

INTP0 to INTP7, which are used as counter restart trigger sources, are not affected by the settings of the external interrupt rising edge enable register (EGP0) or external interrupt falling edge enable register (EGN0). Only the rising edge is valid.

Correct:

(1) Using external interrupts (INTP0 to INTP7)

INTP0 to INTP7, which are used as counter restart trigger sources, are not affected by the settings of the external interrupt rising edge enable register (EGP0) or external interrupt falling edge enable register (EGN0). Only the rising edge is valid.

However, when using the PWM output function for IH control, the active edge can be selected by 16-bit timer KB2 output control register 01 (TKBIOC01).

3. 11.1 Functions of Watchdog Timer (p.433)

Incorrect:

(omitted)

~~When 75% + 1/2FIL of the overflow time~~ is reached, an interval interrupt can be generated.

Correct:

(omitted)

When 75% of the overflow time + 1/2 FIL is reached, an interval interrupt can be generated.

4. 11.4.4 Setting watchdog timer interval interrupt (p.439)

Incorrect:

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% + 1/2FIL of the overflow time is reached.

Table 11-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is used.
1	Interval interrupt is generated <u>when 75% + 1/2FIL of overflow time</u> is reached.

5. 14.3.14 Serial standby control register m (SSCm) (p.526)

Incorrect:

(omitted)

Caution The maximum transfer rate in the SNOOZE mode is as follows.

- When using CSI00: 1 Mbps
- When using UART0, UART2: 9600 bps

Correct:

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% of the overflow time + 1/2 FIL is reached.

Table 11-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is used.
1	Interval interrupt is generated <u>when 75% of the overflow time + 1/2 FIL</u> is reached.

Correct:

(omitted)

Caution The maximum transfer rate in the SNOOZE mode is as follows.

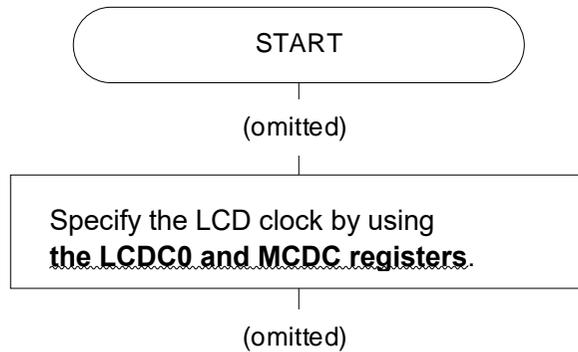
- When using CSI00: 1 Mbps
- When using UART0, UART2: 4800 bps

6. 16.6 Setting the LCD Controller/Driver (p.770)

Incorrect:

(1) External resistance division method

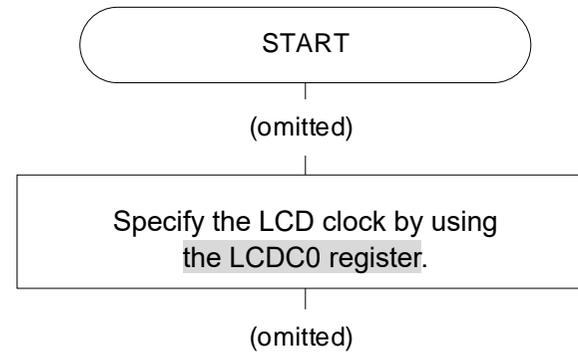
Figure 16-17. External Resistance Division Method Setting Procedure



Correct:

(1) External resistance division method

Figure 16-17. External Resistance Division Method Setting Procedure



7. 22.2 States of Operation During Reset Periods (p.891)

Incorrect:

Table 22-1. Operation Statuses During Reset Period

Item		During Reset Period
System clock		(omitted)
Subsystem clock	fXT	<b>Operation possible (the XT1 and XT2 pins are input port mode)</b>
(omitted)		

Correct:

Table 22-1. Operation Statuses During Reset Period

Item		During Reset Period
System clock		(omitted)
Subsystem clock	fXT	<b>Operation possible</b>
(omitted)		

8. 27.2 Format of User Option Byte (p.939)

Incorrect:

Figure 27-1. Format of User Option Byte (000C0H/010C0H)  
(omitted)

WDTINT	Use of interval interrupt of watchdog timer
0	Interval interrupt is used.
1	Interval interrupt is generated <u>when 75% + 1/2fil. of overflow time</u> is reached.

Corrected:

Figure 27-1. Format of User Option Byte (000C0H/010C0H)  
(omitted)

WDTINT	Use of interval interrupt of watchdog timer
0	Interval interrupt is used.
1	Interval interrupt is generated when 75% of the overflow time + 1/2 fil is reached.