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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A056A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1D Descriptions in the Hardware User's Manual Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1D R5F117xxx	Lot No. All lots	Reference Document	RL78/I1D User's Manual: Hardware Rev.2.00 R01UH0474EJ0200 (Jan. 2015)		

This document describes misstatements found in the RL78/I1D User's Manual: Hardware Rev.2.00 (R01UH0474EJ0200).

Corrections

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1.6 Outline of Functions Number of event input of event link controller in outline of function table	Page 15	Incorrect descriptions revised
3.1 Memory Space. Last address of the Data flash memory Figure 3 - 1 Memory Map (R5F117xA (x = 6, 7, A, B, G))	Page 45	Incorrect descriptions revised
3.2.5 Extended special function registers. Manipulable bit range in subsysytem clock supply mode control register Table 3 - 9 Extended Special Function Register (2nd SFR) List (2/5)	Page 67	Incorrect descriptions revised
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15.3.4 Comparator filter control register (COMPFIR) Figure 15 - 5 Format of Comparator filter control register (COMPFIR)	Pages 433 and 434	Incorrect descriptions revised
15.3.5 Comparator output control register (COMPOCR) Figure 15 - 6 Format of Comparator output control register (COMPOCR)	Page 435	Incorrect descriptions revised
19.3.3 Vector Table Text and Figure 19 - 4 in 19.3.3. Vector Table	Page 650	Incorrect descriptions revised
19.4.2 Normal Mode Text and Figure 19 - 16 in 19.4.2. Normal Mode	Page 662	Incorrect descriptions revised
30.8.3 Procedure for accessing data flash memory Setup time for each main clock mode	Page 826	Incorrect descriptions revised
34.1 Absolute Maximum Ratings Ratings of analog input voltage	Page 856	Incorrect descriptions revised
34.3.2 Supply current characteristics Note of LS (low-speed main) mode (MCSEL = 1)	Page 864	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items Document No. English R01UH0474EJ0200		Pages in this document for corrections
1	1.6 Outline of Functions Number of event input of event link controller in outline of function table	Page 15	Page 3
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9	19.3.3 Vector Table Text and Figure 19 - 4 in 19.3.3. Vector Table	Page 650	Page 11
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11	30.8.3 Procedure for accessing data flash memory Setup time for each main clock mode	Page 826	Page 13
12	34.1 Absolute Maximum Ratings Ratings of analog input voltage	Page 856	Page 14
13	34.3.2 Supply current characteristics Note of LS (low-speed main) mode (MCSEL = 1)	Page 864	Page 15

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1D User's Manual: Hardware Rev.2.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A056A/E	Oct. 29, 2015	First edition issued No.1 to 13 in corrections (This notice)

1. 1.6 Outline of Functions

Number of event input of event link controller in outline of function table (Page 15)

Incorrect:

(omitted)

Data transfer controller (DTC)		16 sources	20 sources	19 sources	20 sources	23 sources
Event link controller (ELC)		Event input: **13**, Event trigger output: 5	Event input: 17 Event trigger output: 5	Event input: **16**, Event trigger output: 7	Event input: 17 Event trigger output: 7	Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	22	22	24	24	24
	External	3	5	5	5	8
Key interrupt		—	3	—	3	4

(omitted)

Correct:

(omitted)

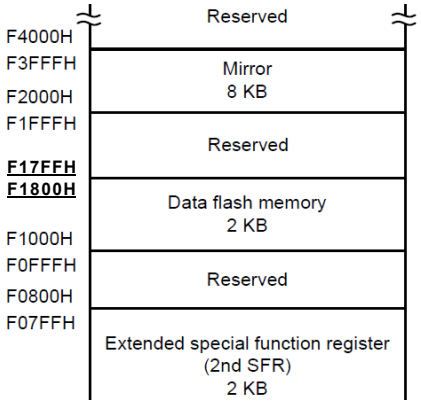
Data transfer controller (DTC)		16 sources	20 sources	19 sources	20 sources	23 sources
Event link controller (ELC)		Event input: 15, Event trigger output: 5	Event input: 17 Event trigger output: 5	Event input: 17, Event trigger output: 7	Event input: 17 Event trigger output: 7	Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	22	22	24	24	24
	External	3	5	5	5	8
Key interrupt		—	3	—	3	4

(omitted)

2. 3.1 Memory Space. Last address of the Data flash memory
Figure 3 - 2 Memory Map (R5F117xA (x = 6, 7, A, B, G)) (Page 45)

Incorrect:

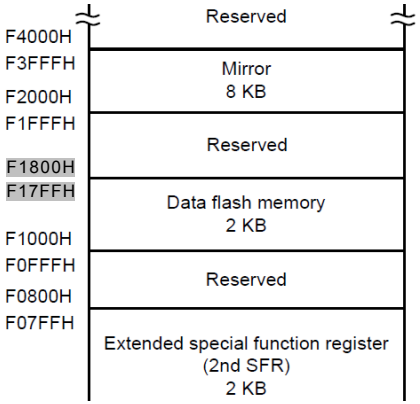
(omitted)



(omitted)

Correct:

(omitted)



(omitted)

3. 3.2.5 Extended special function registers. Manipulable bit range in subsysytem clock supply mode control register

Table 3 - 9 Extended Special Function Register (2nd SFR) List (2/5) (Page 67)

Incorrect:

Table 3 - 9 Extended Special Function Register (2nd SFR) List (2/5)

Address	Extended Special Function Register (2nd SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F00F1H	Peripheral reset control register 0	PRR0	R/W	√	√	—	00H
F00F2H	Middle-speed on-chip oscillator frequency select register	MOCODIV	R/W	—	√	—	00H
F00F3H	Subsystem clock supply mode control register	OSMC	R/W	—	√	—	00H
F00F5H	RAM parity error control register	RPECTL	R/W	√	√	—	00H
F00F8H	Regulator mode control register	PMMC	R/W	√	√	—	00H

(omitted)

Correct:

Table 3 - 9 Extended Special Function Register (2nd SFR) List (2/5)

Address	Extended Special Function Register (2nd SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F00F1H	Peripheral reset control register 0	PRR0	R/W	√	√	—	00H
F00F2H	Middle-speed on-chip oscillator frequency select register	MOCODIV	R/W	—	√	—	00H
F00F3H	Subsystem clock supply mode control register	OSMC	R/W	√	√	—	00H
F00F5H	RAM parity error control register	RPECTL	R/W	√	√	—	00H
F00F8H	Regulator mode control register	PMMC	R/W	√	√	—	00H

(omitted)

4. 6.3.2 System clock control register (CKC)
Figure 6 - 3 Format of System clock control register (CKC) (Page 136)

Incorrect:

Figure 6 - 3 Format of System clock control register (CKC)

(omitted)

MCM1	Main on-chip oscillator clock (f_{OCO}) operation control
0	High-speed on-chip oscillator clock
1	Middle-speed on-chip oscillator clock

(omitted)

Note 1. Bits 7, 5, and 1 are read-only.
Note 2. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

Correct:

Figure 6 - 3 Format of System clock control register (CKC)

(omitted)

MCM1 Note2	Main on-chip oscillator clock (f_{OCO}) operation control
0	High-speed on-chip oscillator clock
1	Middle-speed on-chip oscillator clock

(omitted)

Note 1. Bits 7, 5, and 1 are read-only.
Note 2. Changing the value of the MCM0 bit and MCM1 bit are prohibited while the CSS bit is set to 1.

5. 6.7 Resonator and Oscillator Constants. Delete the resonators for which the operation is verified and their oscillator constants

6.7 Resonator and Oscillator Constants (Pages 178 to 180)

Incorrect:

The resonators for which the operation is verified and their oscillator constants are shown below.

Caution 1. The constants for these oscillator circuits are reference values based on specific environments set up for evaluation by the manufacturers. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board. Furthermore, if you are switching from a different product to this microcontroller, and whenever you change the board, again request evaluation by the manufacturer of the oscillator circuit mounted on the new board.

Caution 2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78 microcontroller so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Figure 6 - 22 Example of External Circuit

(omitted)

Correct:

For the resonators for which the operation is verified and their oscillator constants, refer to the target product page of the Renesas Electronics website.

Caution 1. The constants for these oscillator circuits are reference values based on specific environments set up for evaluation by the manufacturers. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board. Furthermore, if you are switching from a different product to this microcontroller, and whenever you change the board, again request evaluation by the manufacturer of the oscillator circuit mounted on the new board.

Caution 2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78 microcontroller so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Figure 6 - 22 Example of External Circuit

(Delete the resonators for which the operation is verified and their oscillator constants on pages 179 and 180.)

6. 8.3.5 Real-time clock control register 1 (RTCC1). Added notes

Figure 8 - 8 Format of Real-time clock control register 1 (RTCC1) (3/3) (Page 298)

Incorrect:

Figure 8 - 8 Format of Real-time clock control register 1 (RTCC1) (3/3)

(omitted)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.
Be sure to write 1 to it to read or write the counter value.
As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.
After RWAIT is set to 1, it takes up to one f_{RTC} clock cycle before reading/writing the count value is enabled (RWST = 1).
When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

Correct:

Figure 8 - 8 Format of Real-time clock control register 1 (RTCC1) (3/3)

(omitted)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.
Be sure to write 1 to it to read or write the counter value.
As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.
After RWAIT is set to 1, it takes up to one f_{RTC} clock cycle before reading/writing the count value is enabled (RWST = 1).
When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

Note 1. When the RWAIT bit is set to 1 within one cycle of f_{RTC} clock after setting the RTCE bit to 1, the RWST bit being set to 1 may take up to two cycles of the operating clock (f_{RTC}).
Note 2. When the RWAIT bit is set to 1 within one cycle of f_{RTC} clock after release from the standby mode (HALT mode, STOP mode, or SNOOZE mode), the RWST bit being set to 1 may take up to two cycles of the operating clock (f_{RTC}).

7. 15.3.4 Comparator filter control register (COMPFIR) Figure 15 - 5 Format of Comparator filter control register (COMPFIR) (Pages 433 and 434)

Incorrect:

Figure 15 - 5 Format of Comparator filter control register (COMPFIR)

(omitted)

Note 1. If bits C1FCK1 to C1FCK0, C1EPO, and C1EDG are changed, a comparator 1 interrupt and an event signal to the ELC may be generated. Change these bits only after setting the ELSELR19 register for the ELC to 0 (not linked to comparator 1 output). In addition, clear bit 5 (**CPMIF1**) in interrupt request flag register 1H (IF1H) to 0.
If bits C1FCK1 to C1FCK0 are changed from 00B (no comparator 1 filter) to a value other than 00B (comparator 1 filter enabled), allow the time for sampling four times to elapse until the filter output is updated, and then use the comparator 1 interrupt request or the event signal to the ELC.

Note 2. If bits C0FCK1 to C0FCK0, C0EPO, and C0EDG are changed, a comparator 0 interrupt and an event signal to the ELC may be generated. Change these bits only after setting the ELSELR18 register for the ELC to 0(not linked to comparator 0 output). In addition, clear bit 4 (**CPMIF0**) in interrupt request flag register 1H (IF1H) to 0.
If bits C0FCK1 to C0FCK0 are changed from 00B (no comparator 0 filter) to a value other than 00B (comparator 0 filter enabled), allow the time for sampling four times to elapse until the filter output is updated, and then use the comparator 0 interrupt request or the event signal to the ELC.

Correct:

Figure 15 - 5 Format of Comparator filter control register (COMPFIR)

(omitted)

Note 1. If bits C1FCK1 to C1FCK0, C1EPO, and C1EDG are changed, a comparator 1 interrupt and an event signal to the ELC may be generated. Change these bits only after setting the ELSELR19 register for the ELC to 0 (not linked to comparator 1 output). In addition, clear bit 5 (CMPIF1) in interrupt request flag register 1H (IF1H) to 0.
If bits C1FCK1 to C1FCK0 are changed from 00B (no comparator 1 filter) to a value other than 00B (comparator 1 filter enabled), allow the time for sampling four times to elapse until the filter output is updated, and then use the comparator 1 interrupt request or the event signal to the ELC.

Note 2. If bits C0FCK1 to C0FCK0, C0EPO, and C0EDG are changed, a comparator 0 interrupt and an event signal to the ELC may be generated. Change these bits only after setting the ELSELR18 register for the ELC to 0(not linked to comparator 0 output). In addition, clear bit 4 (CMPIF0) in interrupt request flag register 1H (IF1H) to 0.
If bits C0FCK1 to C0FCK0 are changed from 00B (no comparator 0 filter) to a value other than 00B (comparator 0 filter enabled), allow the time for sampling four times to elapse until the filter output is updated, and then use the comparator 0 interrupt request or the event signal to the ELC.

8. 15.3.5 Comparator output control register (COMPOCR) Figure 15 - 6 Format of Comparator output control register (COMPOCR) (Page 435)

Incorrect:

Figure 15 - 6 Format of Comparator output control register (COMPOCR)

(omitted)

Note 2. If C1IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 5 (**CPMIF1**) in interrupt request flag register 1H (IF1H) may set to 1 (interrupt requested), clear **bit 0** (**CPMIF1**) in interrupt request flag register **2H**(**IF2H**) to 0 before using an interrupt.

Note 3. If C0IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since **bit 5** (**CPMIF0**) in interrupt request flag register 1H (IF1H) may set to 1 (interrupt requested), clear bit 4 (**CPMIF0**) in interrupt request flag register 1H(IF1H) to 0 before using an interrupt.

Correct:

Figure 15 - 6 Format of Comparator output control register (COMPOCR)

(omitted)

Note 2. If C1IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 5 (CMPIF1) in interrupt request flag register 1H (IF1H) may set to 1 (interrupt requested), clear bit 5 (CMPIF1) in interrupt request flag register 1H(IF1H) to 0 before using an interrupt.

Note 3. If C0IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 4 (CMPIF0) in interrupt request flag register 1H (IF1H) may set to 1 (interrupt requested), clear bit 4 (CMPIF0) in interrupt request flag register 1H(IF1H) to 0 before using an interrupt.

9. 19.3.3 Vector Table
Text and Figure 19 - 4 in 19.3.3. Vector Table (Page 650)

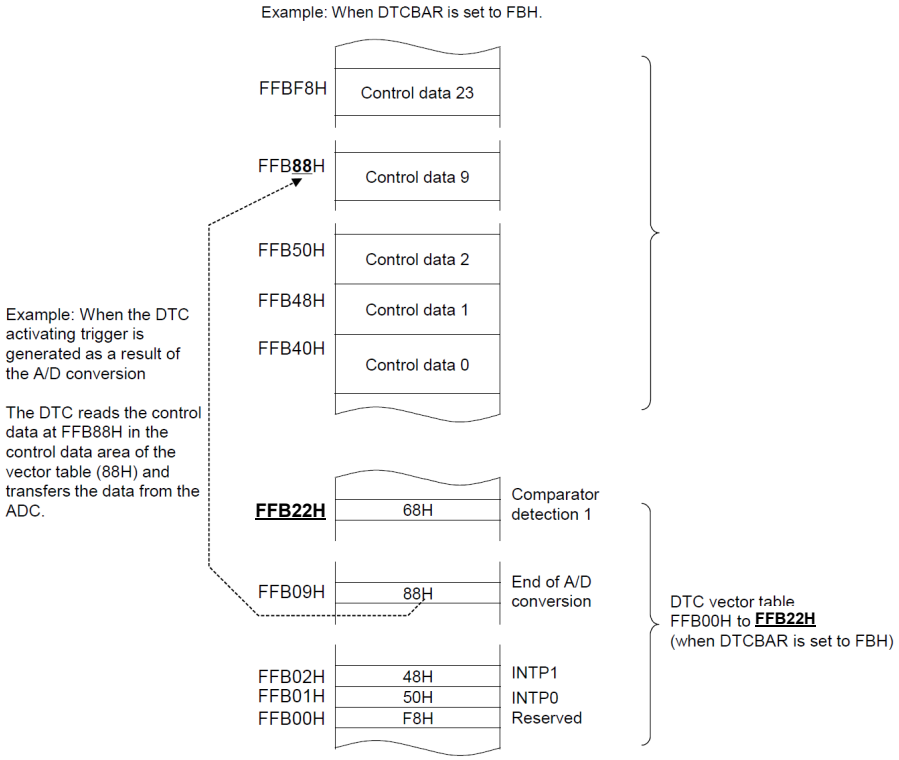
Incorrect:

19.3.3 Vector Table

When the DTC is activated, one set of control data from among the 24 control data sets is selected according to the **4 lower-order bits** of values read from the location in the vector table which is assigned to the corresponding activation source, and the selected control data are read from the DTC control data area.

(omitted)

Figure 19 - 4 Start Address of Control Data and Vector Table



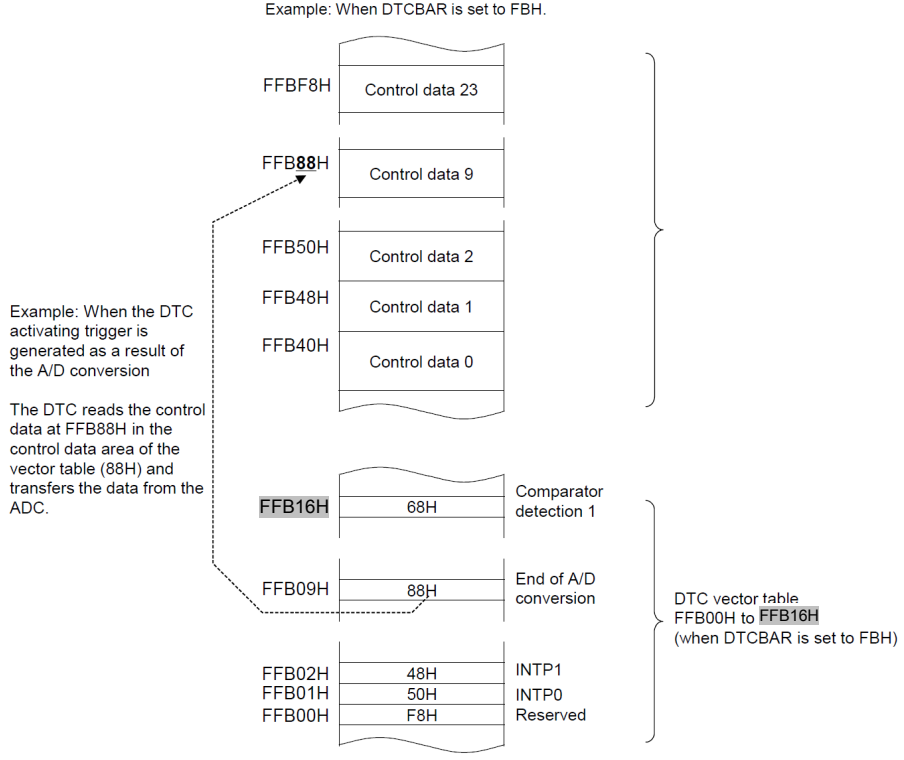
Correct:

19.3.3 Vector Table

When the DTC is activated, one set of control data from among the 24 control data sets is selected according to the 8 lower-order bits of values read from the location in the vector table which is assigned to the corresponding activation source, and the selected control data are read from the DTC control data area.

(omitted)

Figure 19 - 4 Start Address of Control Data and Vector Table



10. 19.4.2 Normal Mode
Text and Figure 19 - 16 in 19.4.2. Normal Mode (Page 662)

Incorrect:

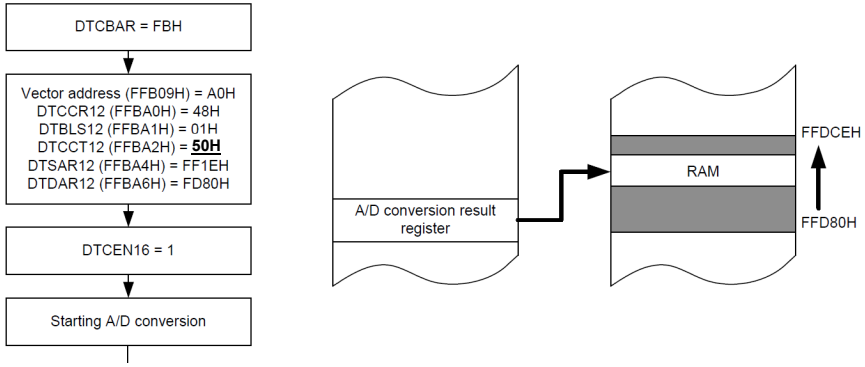
(1) Example 1 of using normal mode: Consecutively capturing A/D conversion results

The DTC is activated by an A/D conversion end interrupt and the value of the A/D conversion result register is transferred to RAM.

- The vector address is FFB09H and control data is allocated at FFBA0H to FFBA7H
- Transfers 2-byte data of the A/D conversion result register (FFF1EH, FFF1FH) to 80 bytes of FFD80H to FFDCEH of RAM

(omitted)

Figure 19 - 16 Example 1 of using normal mode: Consecutively capturing A/D conversion results



(omitted)

Correct:

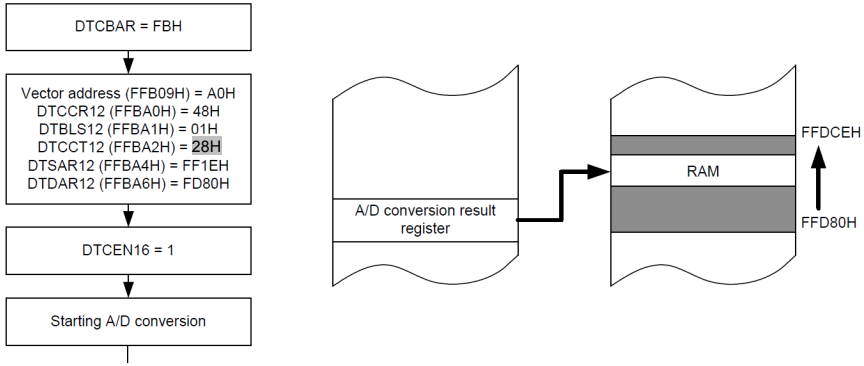
(1) Example 1 of using normal mode: Consecutively capturing A/D conversion results

The DTC is activated by an A/D conversion end interrupt and the value of the A/D conversion result register is transferred to RAM.

- The vector address is FFB09H and control data is allocated at FFBA0H to FFBA7H
- Transfers 2-byte data of the A/D conversion result register (FFF1EH, FFF1FH) to 80 bytes of FFD80H to FFDCEH of RAM 40 times

(omitted)

Figure 19 - 16 Example 1 of using normal mode: Consecutively capturing A/D conversion results



(omitted)

11. 30.8.3 Procedure for accessing data flash memory Setup time for each main clock mode (Page 826)

Incorrect:

30.8.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).
<2> Wait for the setup to finish for software timer, etc.
The time setup takes differs for each main clock mode.
<Setup time for each main clock mode>
- HS (high-speed main) mode: **5 ms**
- LS (low-speed main) mode: 720 ns
- LP (low-power main) mode: 720 ns
- LV (low-voltage main) mode: **10 ms**

<3> After the wait, the data flash memory can be accessed.

(omitted)

Correct:

30.8.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).
<2> Wait for the setup to finish for software timer, etc.
The time setup takes differs for each main clock mode.
<Setup time for each main clock mode>
- HS (high-speed main) mode: 5 µs
- LS (low-speed main) mode: 720 ns
- LP (low-power main) mode: 720 ns
- LV (low-voltage main) mode: 10 µs

<3> After the wait, the data flash memory can be accessed.

(omitted)

12. 34.1 Absolute Maximum Ratings
Ratings of analog input voltage (Page 856)

Incorrect:

Absolute Maximum Ratings

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD}=AV_{DD}	-0.3 to +4.6	V

(omitted)

Analog input voltage	V_{AI1}	ANI16 to ANI18	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Note 2	V
	V_{AI2}	ANI0 to ANI13	-0.3 to AV_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Note 2	V
	V_{AI3}	Operational amplifier input pin	-0.3 to AV_{DD} + 0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
Note 2. Must be 4.6 V or lower.
Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

(omitted)

Correct:

Absolute Maximum Ratings

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD}=AV_{DD}	-0.3 to +4.6	V

(omitted)

Analog input voltage	V_{AI1}	ANI16 to ANI18	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Note 2, 3	V
	V_{AI2}	ANI0 to ANI13	-0.3 to AV_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Note 2, 3	V
	V_{AI3}	Operational amplifier input pin	-0.3 to AV_{DD} + 0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
Note 2. Must be 4.6 V or lower.
Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

(omitted)

13. 34.3.2 Supply current characteristics
Note of LS (low-speed main) mode (MCSEL = 1) (Page 864)

Incorrect:

(T_A = -40 to + 85 ˚C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to +105 ˚C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operation mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105 ˚C	Basic operation	V_{DD} = 3.0V			1.4		mA
(omitted)											
			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 3, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.6	1.1	mA
							Resonator connection		0.6	1.2	
				f_{MX} = 4 MHz Note 3, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.6	1.1	
							Resonator connection		0.6	1.2	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 1 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 3.0 V	Square wave input		100	190	µA
							Resonator connection		136	250	
				f_{MX} = 1 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 2.0 V	Square wave input		100	190	
							Resonator connection		136	250	

(omitted)

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

(omitted)

Correct:

(T_A = -40 to + 85 ˚C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to +105 ˚C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operation mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105 ˚C	Basic operation	V_{DD} = 3.0V			1.4		mA
(omitted)											
			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.6	1.1	mA
							Resonator connection		0.6	1.2	
				f_{MX} = 4 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.6	1.1	
							Resonator connection		0.6	1.2	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 1 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 3.0 V	Square wave input		100	190	µA
							Resonator connection		136	250	
				f_{MX} = 1 MHz Note 2, T_A = -40 to +85 ˚C	Normal operation	V_{DD} = 2.0 V	Square wave input		100	190	
							Resonator connection		136	250	

(omitted)

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

(omitted)