Date: Sep.24, 2013

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A018A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1A Descriptions in the Hardware User's Manual Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1A R5F10E	Lot No. All lots	Reference Document	RL78/G1A User's Manual: Hardware Rev.1.10 R01UH0305EJ0110 (Mar. 2013)		

This document describes misstatements found in the RL78/G1A User's Manual: Hardware Rev.1.10 (R01UH0305EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
11.2 Configuration of A/D Converter	Pages 363	Incorrect descriptions revised
11.3.2 A/D converter mode register 0 (ADM0)	Pages 371 to 375	Incorrect descriptions revised
12.6 Operation of UART (UART0 to UART2) Communication	Pages 528	Incorrect descriptions revised
12.6.1 UART transmission	Pages 539	Incorrect descriptions revised
13.5.16 Communication operations	Page 637	Incorrect descriptions revised
17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)	Pages 746	Incorrect descriptions revised
18.3.3 SNOOZE mode	Page 767	Incorrect descriptions revised
22.3.1.1 Flash memory CRC control register (CRC0CTL)	Pages 808	Incorrect descriptions revised
25.4.3 Procedure for accessing data flash memory	Page 842	Changed specification
29.3.1 Pin characteristics	Page 889 , 890	Incorrect descriptions revised
29.4 AC Characteristics	Page 900	Incorrect descriptions revised
29.5.1 Serial array unit	Page 905 to 917	Incorrect descriptions revised
29.6.1 A/D converter characteristics	Page 929	Extended specification
30.3.1 Pin characteristics	Page 944 , 945	Incorrect descriptions revised
30.4 AC Characteristics	Page 954	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No. English	R01UH0305EJ0110	
1	11.2 Configuration of A/D Converter		Page 363	Page 3
2	11.3.2 A/D converter mode register 0 (ADM0)		Pages 371 to 375	Pages 4 to 7
3	12.6 Operation of UART (UART0 to UART2) Communication		Page 528	Page 8
4	12.6.1 UART transmission		Page 539	Pages 9 , 10
5	13.5.16 Communication operations		Page 637	Page 11
6	17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)		Page 746	Pages 12 , 13
7	18.3.3 SNOOZE mode		Page 767	Page 14
8	22.3.1.1 Flash memory CRC control register (CRC0CTL)		Page 808	Page 14
9	25.4.3 Procedure for accessing data flash memory		Page 842	Pages 15 , 16
10	29.3.1 Pin characteristics		Pages 889 , 890	Page 17
11	29.4 AC Characteristics		Page 900	Page 18
12	29.5.1 Serial array unit		Page 905 to 917	Pages 19 to 24
13	29.6.1 A/D converter characteristics		Page 929	Page 25
14	30.3.1 Pin characteristics		Page 944 , 945	Page 26
15	30.4 AC Characteristics		Page 954	Page 27

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G1A User's Manual: Hardware Rev.1.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A018A/E	Sep. 9, 2013	First edition issued No.1 to 15 in corrections (This notice)

Incorrect:

1. 11.2 Configuration of A/D Converter

(9) AVREFP pin
This pin inputs an external reference voltage (AVREFP).
If using AVREFP as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 1.
The analog signals input to ANI2 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AVREFP and the -side reference voltage (AVREFM/AVSS).
In addition to AVREFP, it is possible to select AVDD, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

Correct:

(9) AVREFP pin
This pin inputs an external reference voltage (AVREFP).
If using AVREFP as the + side reference voltage of the A/D converter, set the A/D converter mode register 2 (ADM2), ADREFP1 bits to 1 and ADREFP0 bits to 0.
The analog signals input to ANI2 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AVREFP and the -side reference voltage (AVREFM/AVSS).
In addition to AVREFP, it is possible to select AVDD, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

Incorrect:

2. 11.3.2 A/D converter mode register 0 (ADM0)

Table 11-3. A/D Conversion Time Selection (2/4)

(2) 12 bit A/D Converter When there is stabilization wait time (hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode Note 1))

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time +Conversion Time	Stabilization Wait Time + Conversion Time Selection				
										AVDD = 1.6 to 3.6 V	AVDD = 1.6 to 3.6 V	AVDD = 1.8 to 3.6 V	AVDD = 2.4 to 3.6 V	AVDD = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	1	0	Normal 1	f_{CLK}/32	4 f_{CLK}	54 f_{AD} (number of sampling clock: 11 f_{AD})	1732/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.125 μs
0	0	1				f_{CLK}/16			868/f_{CLK}				54.25 μs	27.125 μs
0	1	0				f_{CLK}/8			436/f_{CLK}			54.5 μs	27.25 μs	13.625 μs
0	1	1				f_{CLK}/6			328/f_{CLK}			41 μs	20.5 μs	10.25 μs
1	0	0				f_{CLK}/5			274/f_{CLK}			34.25 μs	17.125 μs	8.5625 μs
1	0	1				f_{CLK}/4			220/f_{CLK}		55 μs	27.5 μs	13.75 μs	6.875 μs
1	1	0				f_{CLK}/2			112/f_{CLK}		28 μs	14 μs	7 μs	3.5 μs
1	1	1				f_{CLK}/1	2 f_{CLK}		56/f_{CLK}	56 μs	14 μs	7 μs	3.5 μs	Setting prohibited
0	0	0	1	1	Normal 2	f_{CLK}/32	58 f_{CLK}	66 f_{AD} (number of sampling clock: 23 f_{AD})	2170/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	67.8125 μs
0	0	1				f_{CLK}/16			1114/f_{CLK}				69.625 μs	34.8125 μs
0	1	0				f_{CLK}/8			586/f_{CLK}			73.25 μs Note 2	36.625 μs	18.3125 μs
0	1	1				f_{CLK}/6			454/f_{CLK}			56.75 μs Note 2	28.375 μs	14.1875 μs
1	0	0				f_{CLK}/5			388/f_{CLK}			48.5 μs Note 2	24.25 μs	12.125 μs
1	0	1				f_{CLK}/4			322/f_{CLK}		80.5 μs Note 2	40.25 μs Note 2	20.125 μs	10.0625 μs
1	1	0				f_{CLK}/2			190/f_{CLK}		47.5 μs Note 2	23.75 μs Note 2	11.875 μs	5.9375 μs
1	1	1				f_{CLK}/1	29 f_{CLK}		95/f_{CLK}	95 μs Note 2	23.75 μs Note 2	11.875 μs Note 2	5.9375 μs	Setting prohibited
0	0	0	1	0	Low-voltage 1	f_{CLK}/32	15 f_{CLK}	76 f_{AD} (number of sampling clock: 33 f_{AD})	2447/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76.46875 μs Note 2
0	0	1				f_{CLK}/16			1231/f_{CLK}				76.9375 μs Note 2	38.46875 μs Note 2
0	1	0				f_{CLK}/8			623/f_{CLK}			77.875 μs	38.9375 μs Note 2	19.46875 μs Note 2
0	1	1				f_{CLK}/6			471/f_{CLK}			58.875 μs	29.4375 μs Note 2	14.71875 μs Note 2
1	0	0				f_{CLK}/5			395/f_{CLK}			49.375 μs	24.6875 μs Note 2	12.34375 μs Note 2
1	0	1				f_{CLK}/4			319/f_{CLK}		79.75 μs Note 2	39.875 μs	19.9375 μs Note 2	9.96875 μs Note 2
1	1	0				f_{CLK}/2			167/f_{CLK}		41.75 μs Note 2	20.875 μs	10.4375 μs Note 2	5.21875 μs Note 2
1	1	1				f_{CLK}/1			91/f_{CLK}	91 μs Note 2	22.75 μs Note 2	11.375 μs	5.6875 μs Note	Setting prohibited
0	0	0	1	1	Low-voltage 2	f_{CLK}/32	8 f_{CLK}	230 f_{AD} (number of sampling clock: 187 f_{AD})	7368/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	230.25 μs Note 2
0	0	1				f_{CLK}/16			3688/f_{CLK}				230.5 μs Note 2	115.25 μs Note 2
0	1	0				f_{CLK}/8			1848/f_{CLK}			231 μs Note 2	115.5 μs Note 2	57.75 μs Note 2
0	1	1				f_{CLK}/6			1388/f_{CLK}			173.5 μs Note 2	86.75 μs Note 2	43.375 μs Note 2
1	0	0				f_{CLK}/5			1158/f_{CLK}			144.75 μs Note 2	72.375 μs Note 2	36.1875 μs Note 2
1	0	1				f_{CLK}/4			928/f_{CLK}		232 μs	116 μs Note 2	58 μs Note 2	29 μs Note 2
1	1	0				f_{CLK}/2			468/f_{CLK}		117 μs	58.5 μs Note 2	29.25 μs Note 2	14.625 μs Note 2
1	1	1				f_{CLK}/1			238/f_{CLK}	238 μs	59.5 μs	29.75 μs Note 2	14.875 μs Note 2	Setting prohibited

Correct:

Table 11-3. A/D Conversion Time Selection (2/4)

(2) 12 bit A/D Converter When there is stabilization wait time (hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode Note 1))

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time +Conversion Time	Stabilization Wait Time + Conversion Time Selection				
										AVDD = 1.6 to 3.6 V	AVDD = 1.6 to 3.6 V	AVDD = 1.8 to 3.6 V	AVDD = 2.4 to 3.6 V	AVDD = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0						fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	0	Normal 1	$f_{CLK}/32$	4 f_{CLK}	54 f_{AD} (number of sampling clock: 11 f_{AD})	1732/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.125 μs
0	0	1				$f_{CLK}/16$			868/f_{CLK}				54.25 μs	27.125 μs
0	1	0				$f_{CLK}/8$			436/f_{CLK}			54.5 μs	27.25 μs	13.625 μs
0	1	1				$f_{CLK}/6$			328/f_{CLK}			41 μs	20.5 μs	10.25 μs
1	0	0				$f_{CLK}/5$			274/f_{CLK}			34.25 μs	17.125 μs	8.5625 μs
1	0	1				$f_{CLK}/4$			220/f_{CLK}		55 μs	27.5 μs	13.75 μs	6.875 μs
1	1	0				$f_{CLK}/2$			112/f_{CLK}		28 μs	14 μs	7 μs	3.5 μs
1	1	1				$f_{CLK}/1$	2 f_{CLK}		56/f_{CLK}	56 μs	14 μs	7 μs	3.5 μs	Setting prohibited
0	0	0	0	1	Normal 2	$f_{CLK}/32$	58 f_{CLK}	66 f_{AD} (number of sampling clock: 23 f_{AD})	2170/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	67.8125 μs
0	0	1				$f_{CLK}/16$			1114/f_{CLK}				69.625 μs	34.8125 μs
0	1	0				$f_{CLK}/8$			586/f_{CLK}			73.25 μs Note 2	36.625 μs	18.3125 μs
0	1	1				$f_{CLK}/6$			454/f_{CLK}			56.75 μs Note 2	28.375 μs	14.1875 μs
1	0	0				$f_{CLK}/5$			388/f_{CLK}			48.5 μs Note 2	24.25 μs	12.125 μs
1	0	1				$f_{CLK}/4$			322/f_{CLK}		80.5 μs Note 2	40.25 μs Note 2	20.125 μs	10.0625 μs
1	1	0				$f_{CLK}/2$			190/f_{CLK}		47.5 μs Note 2	23.75 μs Note 2	11.875 μs	5.9375 μs
1	1	1				$f_{CLK}/1$	29 f_{CLK}		95/f_{CLK}	95 μs Note 2	23.75 μs Note 2	11.875 μs Note 2	5.9375 μs	Setting prohibited
0	0	0	1	0	Low-voltage 1	$f_{CLK}/32$	15 f_{CLK}	76 f_{AD} (number of sampling clock: 33 f_{AD})	2447/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76.46875 μs Note 2
0	0	1				$f_{CLK}/16$			1231/f_{CLK}				76.9375 μs Note 2	38.46875 μs Note 2
0	1	0				$f_{CLK}/8$			623/f_{CLK}			77.875 μs	38.9375 μs Note 2	19.46875 μs Note 2
0	1	1				$f_{CLK}/6$			471/f_{CLK}			58.875 μs	29.4375 μs Note 2	14.71875 μs Note 2
1	0	0				$f_{CLK}/5$			395/f_{CLK}			49.375 μs	24.6875 μs Note 2	12.34375 μs Note 2
1	0	1				$f_{CLK}/4$			319/f_{CLK}		79.75 μs Note 2	39.875 μs	19.9375 μs Note 2	9.96875 μs Note 2
1	1	0				$f_{CLK}/2$			167/f_{CLK}		41.75 μs Note 2	20.875 μs	10.4375 μs Note 2	5.21875 μs Note 2
1	1	1				$f_{CLK}/1$			91/f_{CLK}	91 μs Note 2	22.75 μs Note 2	11.375 μs	5.6875 μs Note	Setting prohibited
0	0	0	1	1	Low-voltage 2	$f_{CLK}/32$	8 f_{CLK}	230 f_{AD} (number of sampling clock: 187 f_{AD})	7368/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	230.25 μs Note 2
0	0	1				$f_{CLK}/16$			3688/f_{CLK}				230.5 μs Note 2	115.25 μs Note 2
0	1	0				$f_{CLK}/8$			1848/f_{CLK}			231 μs Note 2	115.5 μs Note 2	57.75 μs Note 2
0	1	1				$f_{CLK}/6$			1388/f_{CLK}			173.5 μs Note 2	86.75 μs Note 2	43.375 μs Note 2
1	0	0				$f_{CLK}/5$			1158/f_{CLK}			144.75 μs Note 2	72.375 μs Note 2	36.1875 μs Note 2
1	0	1				$f_{CLK}/4$			928/f_{CLK}		232 μs	116 μs Note 2	58 μs Note 2	29 μs Note 2
1	1	0				$f_{CLK}/2$			468/f_{CLK}		117 μs	58.5 μs Note 2	29.25 μs Note 2	14.625 μs Note 2
1	1	1				$f_{CLK}/1$			238/f_{CLK}	238 μs	59.5 μs	29.75 μs Note 2	14.875 μs Note 2	Setting prohibited

Incorrect:

Table 11-3. A/D Conversion Time Selection (4/4)

(4) 8 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode [Note 1]))

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time +Conversion Time	Stabilization Wait Time + Conversion Time Selection				
										AV_{DD} = 1.6 to 3.6 V	AV_{DD} = 1.6 to 3.6 V	AV_{DD} = 1.8 to 3.6 V	AV_{DD} = 2.4 to 3.6 V	AV_{DD} = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	1	0	Normal 1	f_{CLK}/32	4 f_{CLK}	41 f_{AD} (number of sampling clock: 11 f_{AD})	1316/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	41.125 μs
0	0	1				f_{CLK}/16			660/f_{CLK}				41.25 μs	20.625 μs
0	1	0				f_{CLK}/8			332/f_{CLK}			41.5 μs	20.75 μs	10.375 μs
0	1	1				f_{CLK}/6			250/f_{CLK}			31.25 μs	15.625 μs	7.8125 μs
1	0	0				f_{CLK}/5			209/f_{CLK}			25.125 μs	13.0625 μs	6.53125 μs
1	0	1				f_{CLK}/4			168/f_{CLK}		42 μs	21 μs	10.5 μs	5.25 μs
1	1	0				f_{CLK}/2			86/f_{CLK}		21.5 μs	10.75 μs	5.375 μs	2.6875 μs
1	1	1				f_{CLK}/1	2 f_{CLK}		43/f_{CLK}	43 μs	10.75 μs	5.375 μs	2.6875 μs	Setting prohibited
0	0	0	1	1	Normal 2	f_{CLK}/32	58 f_{CLK}	53 f_{AD} (number of sampling clock: 23 f_{AD})	1754/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.8125 μs
0	0	1				f_{CLK}/16			906/f_{CLK}				56.625 μs	28.3125 μs
0	1	0				f_{CLK}/8			482/f_{CLK}			60.25 μs [Note 2]	30.125 μs	15.0625 μs
0	1	1				f_{CLK}/6			376/f_{CLK}			47 μs [Note 2]	23.5 μs	11.75 μs
1	0	0				f_{CLK}/5			323/f_{CLK}			40.375 μs [Note 2]	20.1875 μs	10.09375 μs
1	0	1				f_{CLK}/4			270/f_{CLK}		67.5 μs [Note 2]	33.75 μs [Note 2]	16.875 μs	8.4375 μs
1	1	0				f_{CLK}/2			164/f_{CLK}		41 μs [Note 2]	20.5 μs [Note 2]	10.25 μs	5.125 μs
1	1	1				f_{CLK}/1	29 f_{CLK}		82/f_{CLK}	82 μs [Note 2]	20.5 μs [Note 2]	10.25 μs [Note 2]	5.125 μs	Setting prohibited
0	0	0	1	0	Low-voltage 1	f_{CLK}/32	15 f_{CLK}	63 f_{AD} (number of sampling clock: 33 f_{AD})	2031/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	63.46875 μs [Note 2]
0	0	1				f_{CLK}/16			1023/f_{CLK}				63.9375 μs [Note 2]	31.96875 μs [Note 2]
0	1	0				f_{CLK}/8			519/f_{CLK}			64.875 μs	32.4375 μs [Note 2]	16.21875 μs [Note 2]
0	1	1				f_{CLK}/6			393/f_{CLK}			49.125 μs	24.5625 μs [Note 2]	12.28125 μs [Note 2]
1	0	0				f_{CLK}/5			330/f_{CLK}			41.25 μs	20.625 μs [Note 2]	10.3125 μs [Note 2]
1	0	1				f_{CLK}/4			267/f_{CLK}		66.75 μs [Note 2]	33.375 μs	16.6875 μs [Note 2]	8.34375 μs [Note 2]
1	1	0				f_{CLK}/2			141/f_{CLK}		35.25 μs [Note 2]	17.625 μs	8.8125 μs [Note 2]	4.40625 μs [Note 2]
1	1	1				f_{CLK}/1			78/f_{CLK}	78 μs [Note 2]	19.5 μs [Note 2]	9.75 μs	4.875 μs [Note 2]	Setting prohibited
0	0	0	1	1	Low-voltage 2	f_{CLK}/32	8 f_{CLK}	217 f_{AD} (number of sampling clock: 187 f_{AD})	6952/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	217.25 μs [Note 2]
0	0	1				f_{CLK}/16			3480/f_{CLK}				217.5 μs [Note 2]	108.75 μs [Note 2]
0	1	0				f_{CLK}/8			1744/f_{CLK}			218 μs	109 μs [Note 2]	54.5 μs [Note 2]
0	1	1				f_{CLK}/6			1310/f_{CLK}			163.75 μs [Note 2]	81.875 μs [Note 2]	40.9375 μs [Note 2]
1	0	0				f_{CLK}/5			1093/f_{CLK}			136.625 μs [Note 2]	68.3125 μs [Note 2]	34.15625 μs [Note 2]
1	0	1				f_{CLK}/4			876/f_{CLK}		219 μs	109.5 μs [Note 2]	54.75 μs [Note 2]	27.375 μs [Note 2]
1	1	0				f_{CLK}/2			442/f_{CLK}		110.5 μs	55.25 μs [Note 2]	27.625 μs [Note 2]	13.8125 μs [Note 2]
1	1	1				f_{CLK}/1			225/f_{CLK}	225 μs	56.25 μs	28.125 μs [Note 2]	14.0625 μs [Note 2]	Setting prohibited

Correct:

Table 11-3. A/D Conversion Time Selection (4/4)

(4) 8 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode [Note 1]))

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time +Conversion Time	Stabilization Wait Time + Conversion Time Selection				
										AV_{DD} = 1.6 to 3.6 V	AV_{DD} = 1.6 to 3.6 V	AV_{DD} = 1.8 to 3.6 V	AV_{DD} = 2.4 to 3.6 V	AV_{DD} = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{CLK}	41 f_{AD} (number of sampling clock: 11 f_{AD})	1316/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	41.125 μs
0	0	1				f_{CLK}/16			660/f_{CLK}				41.25 μs	20.625 μs
0	1	0				f_{CLK}/8			332/f_{CLK}			41.5 μs	20.75 μs	10.375 μs
0	1	1				f_{CLK}/6			250/f_{CLK}			31.25 μs	15.625 μs	7.8125 μs
1	0	0				f_{CLK}/5			209/f_{CLK}			25.125 μs	13.0625 μs	6.53125 μs
1	0	1				f_{CLK}/4			168/f_{CLK}		42 μs	21 μs	10.5 μs	5.25 μs
1	1	0				f_{CLK}/2			86/f_{CLK}		21.5 μs	10.75 μs	5.375 μs	2.6875 μs
1	1	1				f_{CLK}/1	2 f_{CLK}		43/f_{CLK}	43 μs	10.75 μs	5.375 μs	2.6875 μs	Setting prohibited
0	0	0	0	1	Normal 2	f_{CLK}/32	58 f_{CLK}	53 f_{AD} (number of sampling clock: 23 f_{AD})	1754/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.8125 μs
0	0	1				f_{CLK}/16			906/f_{CLK}				56.625 μs	28.3125 μs
0	1	0				f_{CLK}/8			482/f_{CLK}			60.25 μs [Note 2]	30.125 μs	15.0625 μs
0	1	1				f_{CLK}/6			376/f_{CLK}			47 μs [Note 2]	23.5 μs	11.75 μs
1	0	0				f_{CLK}/5			323/f_{CLK}			40.375 μs [Note 2]	20.1875 μs	10.09375 μs
1	0	1				f_{CLK}/4			270/f_{CLK}		67.5 μs [Note 2]	33.75 μs [Note 2]	16.875 μs	8.4375 μs
1	1	0				f_{CLK}/2			164/f_{CLK}		41 μs [Note 2]	20.5 μs [Note 2]	10.25 μs	5.125 μs
1	1	1				f_{CLK}/1	29 f_{CLK}		82/f_{CLK}	82 μs [Note 2]	20.5 μs [Note 2]	10.25 μs [Note 2]	5.125 μs	Setting prohibited
0	0	0	1	0	Low-voltage 1	f_{CLK}/32	15 f_{CLK}	63 f_{AD} (number of sampling clock: 33 f_{AD})	2031/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	63.46875 μs [Note 2]
0	0	1				f_{CLK}/16			1023/f_{CLK}				63.9375 μs [Note 2]	31.96875 μs [Note 2]
0	1	0				f_{CLK}/8			519/f_{CLK}			64.875 μs	32.4375 μs [Note 2]	16.21875 μs [Note 2]
0	1	1				f_{CLK}/6			393/f_{CLK}			49.125 μs	24.5625 μs [Note 2]	12.28125 μs [Note 2]
1	0	0				f_{CLK}/5			330/f_{CLK}			41.25 μs	20.625 μs [Note 2]	10.3125 μs [Note 2]
1	0	1				f_{CLK}/4			267/f_{CLK}		66.75 μs [Note 2]	33.375 μs	16.6875 μs [Note 2]	8.34375 μs [Note 2]
1	1	0				f_{CLK}/2			141/f_{CLK}		35.25 μs [Note 2]	17.625 μs	8.8125 μs [Note 2]	4.40625 μs [Note 2]
1	1	1				f_{CLK}/1			78/f_{CLK}	78 μs [Note 2]	19.5 μs [Note 2]	9.75 μs	4.875 μs [Note 2]	Setting prohibited
0	0	0	1	1	Low-voltage 2	f_{CLK}/32	8 f_{CLK}	217 f_{AD} (number of sampling clock: 187 f_{AD})	6952/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	217.25 μs [Note 2]
0	0	1				f_{CLK}/16			3480/f_{CLK}				217.5 μs [Note 2]	108.75 μs [Note 2]
0	1	0				f_{CLK}/8			1744/f_{CLK}			218 μs	109 μs [Note 2]	54.5 μs [Note 2]
0	1	1				f_{CLK}/6			1310/f_{CLK}			163.75 μs [Note 2]	81.875 μs [Note 2]	40.9375 μs [Note 2]
1	0	0				f_{CLK}/5			1093/f_{CLK}			136.625 μs [Note 2]	68.3125 μs [Note 2]	34.15625 μs [Note 2]
1	0	1				f_{CLK}/4			876/f_{CLK}		219 μs	109.5 μs [Note 2]	54.75 μs [Note 2]	27.375 μs [Note 2]
1	1	0				f_{CLK}/2			442/f_{CLK}		110.5 μs	55.25 μs [Note 2]	27.625 μs [Note 2]	13.8125 μs [Note 2]
1	1	1				f_{CLK}/1			225/f_{CLK}	225 μs	56.25 μs	28.125 μs [Note 2]	14.0625 μs [Note 2]	Setting prohibited

Incorrect:

3. 12.6 Operation of UART (UART0 to UART2) Communication

- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	**CSI21**		**IIC21**

Correct:

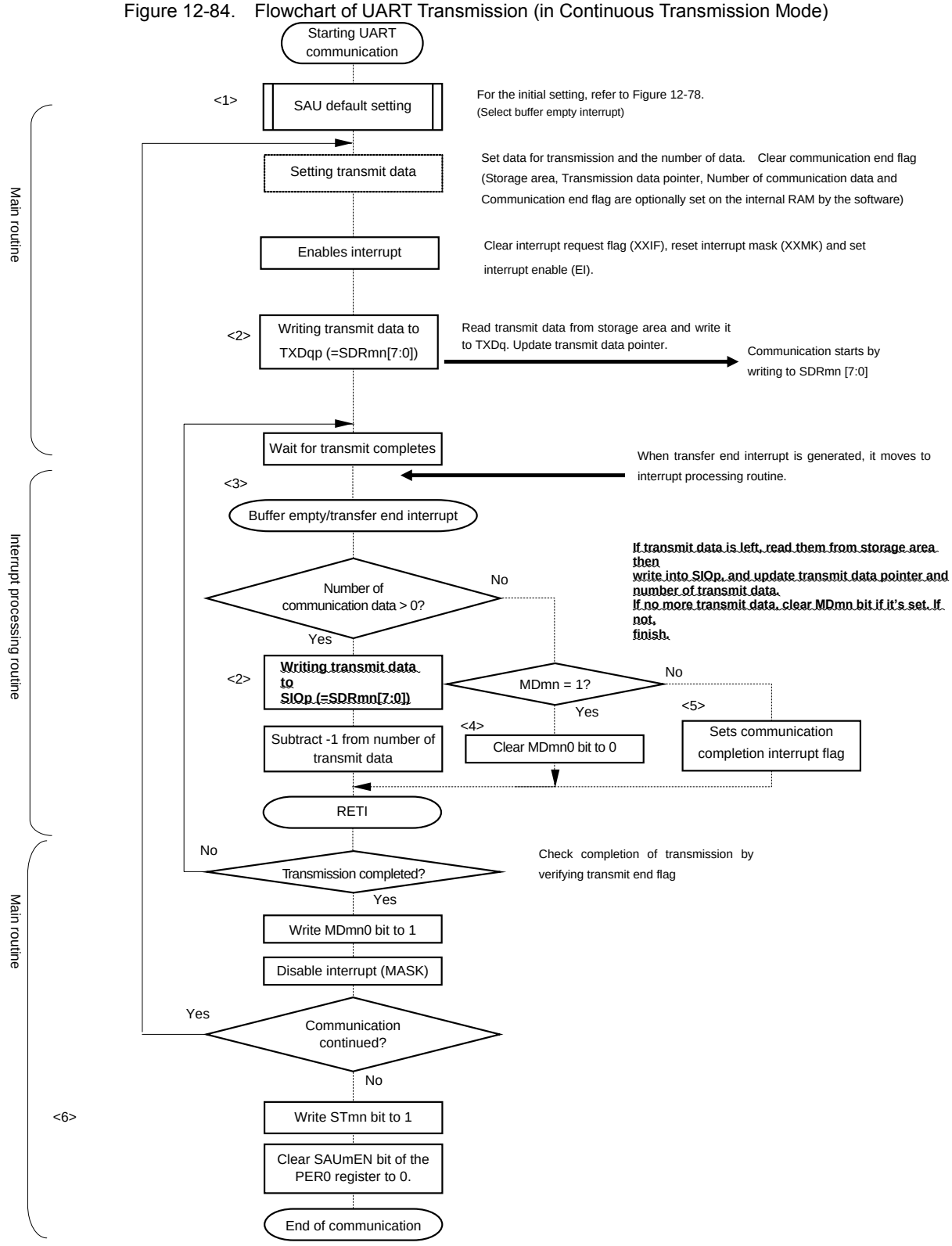
- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	–		–

Incorrect:

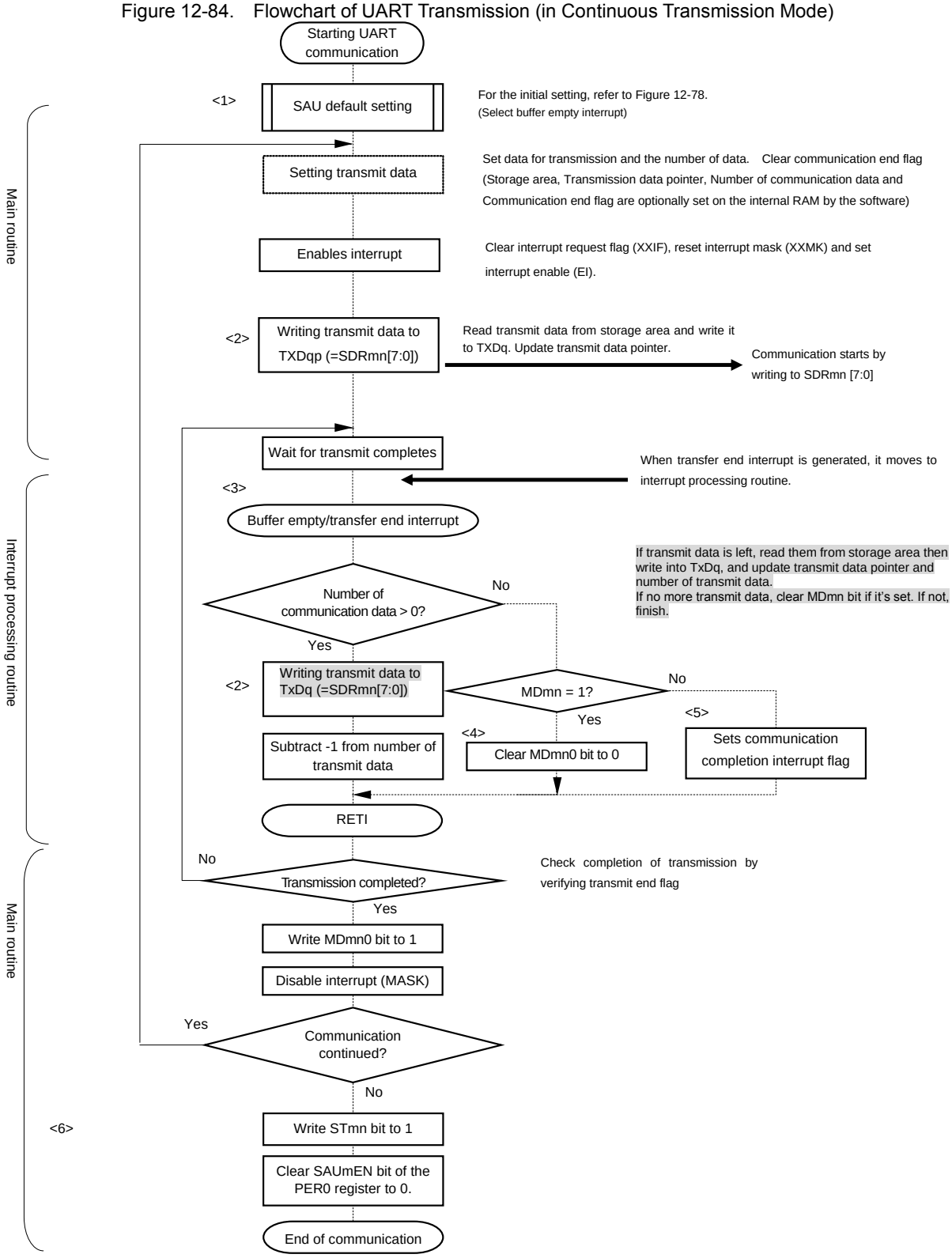
4. 12.6.1 UART transmission

Figure 12-84. Flowchart of UART Transmission (in Continuous Transmission Mode)



Correct:

Figure 12-84. Flowchart of UART Transmission (in Continuous Transmission Mode)



Incorrect:

5. 13.5.16 Communication operations

Note The wait time is calculated as follows.
(IICWL0 setting value + IICWH0 setting value + 4) × f_{CLK} + t_F × 2 [clocks]

Correct:

Note The wait time is calculated as follows.
(IICWL0 setting value + IICWH0 setting value + 4[clocks]) / f_{CLK} + t_F × 2

Incorrect:

6. 17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)

Figure 17-5. Format of Port Mode Register (PM0 to PM2, PM7, PM12, PM15)

Address: FFF20H After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF22H After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF27H After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70

Address: FFF2CH After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

Address: FFF2FH After reset: **00H** R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150

PM0n	I/O mode selection for Pmn/KRm pin (n = 0 to 9, m = 0 to 2, 7, 12, 15)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Correct:

Figure 17-5. Format of Port Mode Register (PM0 to PM2, PM7, PM12, PM15)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70

Address: FFF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

Address: FFF2FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150

PMmn	I/O mode selection for Pmn/KRk pin (n = 0 to 7, m = 0 to 2, 7, 12, 15 , k= 0 to 9)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Incorrect:

7. 18.3.3 SNOOZE mode

Transition time from SNOOZE mode to normal operation:
• When vectored interrupt servicing is carried out:
HS (High-speed main) mode : **4.99 to 9.44 µs + 7 clocks**
LS (Low-speed main) mode : **1.10 to 5.08µs + 7 clocks**
LV (Low-voltage main) mode : **16.58 to 25.40 µs + 7 clocks**
• When vectored interrupt servicing is not carried out:
HS (High-speed main) mode : **4.99 to 9.44 µs + 7 clocks**
LS (Low-speed main) mode : **1.10 to 5.08µ s + 7 clocks**
LV (Low-voltage main) mode : **16.58 to 25.40µs + 7 clocks**

8. 22.3.1.1 Flash memory CRC control register (CRC0CTL)

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	0	0	0	**0 to 3FFBH (16 K to 4 bytes)**
0	0	0	0	0	1	**0 to 7FFBH (32 K to 4 bytes)**
0	0	0	0	1	0	**0 to BFFBH (48 K to 4 bytes)**
0	0	0	0	1	1	**0 to FFFBH (64 K to 4 bytes)**
Other than above						Setting prohibited

Correct:

Transition time from SNOOZE mode to normal operation: •
• When vectored interrupt servicing is carried out:
HS (High-speed main) mode : 4.99 to 9.44 µs + 1 clocks
LS (Low-speed main) mode : 1.10 to 5.08µs + 1 clocks
LV (Low-voltage main) mode : 16.58 to 25.40 µs + 1 clocks ••
• When vectored interrupt servicing is not carried out:
HS (High-speed main) mode : 4.99 to 9.44 µs + 1 clocks
LS (Low-speed main) mode : 1.10 to 5.08µ s + 1 clocks
LV (Low-voltage main) mode : 16.58 to 25.40µs + 1 clocks

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	0	0	0	0 to 3FFBH (16 K - 4 bytes)
0	0	0	0	0	1	0 to 7FFBH (32 K - 4 bytes)
0	0	0	0	1	0	0 to BFFBH (48 K - 4 bytes)
0	0	0	0	1	1	0 to FFFBH (64 K - 4 bytes)
Other than above						Setting prohibited

Incorrect:

9. 25.4.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).
<2> Wait for the setup to finish for software timer.etc.
The time setup takes differs for each main clock mode.
<Setup time for each main clock mode>
• HS (High-speed main): 5 µs
• LS (Low-speed main): 720 ns
• LV (Low-voltage main): 10 µs
<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.
2. Before executing a STOP instruction during the setup time, temporarily clear DFLEN to 0.

Correct:

The data flash memory is stopped after a reset ends. To access the data flash, make initial settings according to the following procedure.

<1> Set bit 0 (DFLEN) of the data flash control register (DFLCTL) to 1.
<2> Wait for the setup to finish for software timer, etc.
The time setup takes differs for each flash operation mode for the main clock.
<Setup time for each flash operation mode>
• HS (High speed main): 5 µs
• LS (Low speed main): 720 ns
• LV (Low voltage main): 10 µs
<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.
2. Transition to the STOP mode is not possible during the setup time. To enter the STOP mode during the setup time, clear DFLEN to 0 and then execute the STOP instruction.
3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, operate the high-speed on-chip oscillator clock (HIOSTOP = 0) and execute the data flash library after 30 µs have elapsed.

After initialized, the data flash memory can be read by using a CPU instruction or can be read/written by using a data flash library.
If the DMA controller operates when the data flash memory is accessed, however, follow one of these procedures:

(A) Suspending/forcibly terminating DMA transfer
Before reading the data flash memory, suspend DMA transfer of all the channels used. After setting the DWAITn bit to 1, however, wait at least for the duration of three clocks (f_{CLK}) before reading the data flash memory. After reading the data flash memory, lift the suspension of transfer by clearing the DWAITn bit to 0.
Or, forcibly terminate DMA transfer in accordance with the procedure in 15.5.5 Forced termination by software before reading the data flash memory. Resume DMA transfer after the data flash memory has been read.
(B) Access the data flash memory by using the newest data flash library.
(C) Insertion of NOP
Insert an NOP instruction immediately before the instruction that reads the data flash memory.
<Example>
MOVW HL,!addr16 ; Reads RAM.
NOP ; Insert NOP instruction before reading data flash memory.
MOV A,[DE] ; Read data flash memory.

If a high-level language such as C is used, however, the compiler may generate two instructions for one code. In this case, the NOP instruction is not inserted immediately before the data flash memory read instruction.
Therefore, read the data flash memory by (A) or (B) above.

Remarks 1. n: DMA channel number (n = 0, 1)
2. f_{CLK}: CPU/peripheral hardware clock frequency

Incorrect:

10. 29.3 DC Characteristics

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (1/5)

Note 3. Specification under output current where the duty ≤ 70%.

The output current value that has changed the duty ratio lower than 70% can be calculated with the following expression (when changing the duty ratio to n%).

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Note 3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio lower than 70% can can be calculated with the following expression (when changing the duty ratio to n%).

Correct:

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

Incorrect:

11. 29.4 AC Characteristics

(T_A = −40 to +85°C, **1.6 V ≤ AV_{DD} ≤ 3.6 V**, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

	Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
	Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{main}) mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
					2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
				LV (Low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
				LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
			In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
					2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
				LV (Low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
				LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
	External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
<R>			2.4 V ≤ V_{DD} < 2.7 V			1.0		**1.0**	MHz
			1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
			1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
		f_{EXS}				32		35	kHz
	External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
<R>			2.4 V ≤ V_{DD} < 2.7 V			30			ns
			1.8 V ≤ V_{DD} < 2.4 V			60			ns
			1.6 V ≤ V_{DD} < 1.8 V			120			ns
		t_{EXHS}, t_{EXLS}				13.7			μs
	TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns[Note]
	TO00, TO01, TO03 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
					1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LV (Low-voltage main) mode		1.6 V ≤ EV_{DD0} ≤ 3.6 V			2	MHz
			LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
	PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
					1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LV (Low-voltage main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
	Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 3.6 V	1			μs
			INTP1 to INTP11		1.6 V ≤ EV_{DD0} ≤ 3.6 V	1			μs
	Key interrupt input high-level width, low-level width	t_{KR}	KR0 to KR9		1.8 V ≤ EV_{DD0} ≤ 3.6 V, 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
					1.6 V ≤ EV_{DD0} < 1.8 V, 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
	$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Correct:

(T_A = −40 to +85°C, $AV_{DD} \le V_{DD} \le 3.6$ V, 1.6 V ≤ $EV_{DD0} \le V_{DD} \le 3.6$ V, $V_{SS} = EV_{SS0}$ = 0 V)

	Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
	Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{main}) mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
					2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
				LV (Low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
				LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
			In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
					2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
				LV (Low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
				LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
<R>	External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
<R>			2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
			1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
			1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
		f_{EXS}				32		35	kHz
<R>	External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
<R>			2.4 V ≤ V_{DD} < 2.7 V			30			ns
			1.8 V ≤ V_{DD} < 2.4 V			60			ns
			1.6 V ≤ V_{DD} < 1.8 V			120			ns
		t_{EXHS}, t_{EXLS}				13.7			μs
	TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns[Note]
	TO00, TO01, TO03 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
					1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LV (Low-voltage main) mode		1.6 V ≤ EV_{DD0} ≤ 3.6 V			2	MHz
			LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
	PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
					1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LV (Low-voltage main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
			LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
					1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
	Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 3.6 V	1			μs
			INTP1 to INTP11		1.6 V ≤ EV_{DD0} ≤ 3.6 V	1			μs
	Key interrupt input high-level width, low-level width	t_{KR}	KR0 to KR9		1.8 V ≤ EV_{DD0} ≤ 3.6 V, 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
					1.6 V ≤ EV_{DD0} < 1.8 V, 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
	$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

12. 29.5.1 Serial array unit

Incorrect:

(2)During communication at same potential (CSI mode) (master mode, SCKp... internal clock output corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 3.6 V, ~~$t_{KCY1} \geq 4/f_{CLK}$~~	83.3 Note 4		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	t_{KCY1}/2 –10		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
SIp setup time (to SCKp↑) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	33		110		110		ns
SIp hold time (from SCKp↑) Note 6	t_{KSI1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 7	t_{KSO1}	C = 30 pF Note 8		10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.
2. LS is condition of LS (low-speed main) mode.
3. LV is condition of LV (low-voltage main) mode.
4. The value must also be 2/fCLK or more.
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
8. C is the load capacitance of the SCKp and SOp output lines.

Correct:

(2)During communication at same potential (CSI mode) (master mode, SCKp... internal clock output corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 3.6 V, $t_{KCY1} \geq 2/f_{CLK}$	83.3 Note 4		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	t_{KCY1}/2 –10		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
SIp setup time (to SCKp↑) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	33		110		110		ns
SIp hold time (from SCKp↑) Note 6	t_{KSI1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 7	t_{KSO1}	C = 20 pF Note 8		10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.
2. LS is condition of LS (low-speed main) mode.
3. LV is condition of LV (low-voltage main) mode.
4. The fMCL must also be 24MHz or less.
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
8. C is the load capacitance of the SCKp and SOp output lines.

Incorrect:

Notes 1. HS is condition of HS (high-speed main) mode.
2. LS is condition of LS (low-speed main) mode.
3. LV is condition of LV (low-voltage main) mode.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
7. C is the load capacitance of the SOp output lines.
8. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Correct:

Notes 1. HS is condition of HS (high-speed main) mode.
2. LS is condition of LS (low-speed main) mode.
3. LV is condition of LV (low-voltage main) mode.
4. Transfer rate in the SNOOZE mode : MAX. 1 Mbps
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1, The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
8. C is the load capacitance of the SOp output lines.

Incorrect:

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = −40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

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Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	$t_{KCY1} \geq 2/f_{CLK}$	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 − 120		t_{KCY1}/2 − 120		t_{KCY1}/2 − 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 − 10		t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		3		110		110		ns
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10		10	ns

Correct:

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = −40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

<R>

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	$t_{KCY1} \geq 2/f_{CLK}$	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 − 120		t_{KCY1}/2 − 120		t_{KCY1}/2 − 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 − 10		t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		110		ns
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10		10	ns

Incorrect:

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

(T_A = −40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to $\overline{SCKp}$↑) Note 4	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	**81**		479		479		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	**177**		479		479		ns
SIp hold time (from $\overline{SCKp}$↑) Note 4	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		**100**		**100**		**100**	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ		**195**		**195**		**195**	ns
SIp setup time (to $\overline{SCKp}$↓) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	**44**		110		110		ns
SIp hold time (from $\overline{SCKp}$↓) Note 5	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 5	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Correct:

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)
(T_A = −40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to $\overline{SCKp}$↑) Note 4	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from $\overline{SCKp}$↑) Note 4	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns
SIp setup time (to $\overline{SCKp}$↓) Note 5	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from $\overline{SCKp}$↓) Note 5	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 5	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 6, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

13. 29.6.1 A/D converter characteristics

Addition:

When $AV_{REF(+)}$= AV_{REFP}/ANI0(ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$= AV_{REFM}/ANI1(ADREFM = 1), target pin:ANI2-ANI12

(T_A = - 40 to +85°C, 2.7 ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD}≤ 3.6V, V_{SS} = 0V, AV_{SS} = 0V, Reference voltage(+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error Note1,2,3	AINL	12bit resolution		±1.7	±3.3	LSB
Conversion time	T_{CONV}	ADTYP=0, 12bit resolution	3.375			µs
Zero-scale error Note1,2,3	E_{ZS}	12bit resolution		±1.3	±3.2	LSB
Full-scale error Note1,2,3	E_{FS}	12bit resolution		±0.7	±2.9	LSB
Integral linearity error Note1,2,3	ILE	12bit resolution		±1.0	±1.4	LSB
Differential linearity error Note1,2,3	DLE	12bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1: TYP. Value is the average value AV_{DD} = AV_{REFP} = 3V, T_A = 25 °C.
MAX. Values are mean ± 3σ in normal distribution.
2: This value based on the characterization results, is not subject to production testing.
3: Excludes quantization error (±1/2 LSB).

Caution 1. Attention must be paid to noise input to each power supply and ground lines.
The reference voltage line of AV_{REFP} is separated from the other power supply lines for noise countermeasures.
Caution 2. Please make sure that pulses whose voltage suddenly change, such as digital pulses, are not input or output to a pin adjacent to the pin whose value is being A/D converted and P20 to P27, P150 to P154.

Incorrect:

14. 30.3.1 Pin characteristics

(T_A = −40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Note 3. Specification under output current where the duty ≤ 70%.

The output current value that has changed the duty ratio lower than 70% can be calculated with the following expression (when changing the duty ratio to n%).

(T_A = −40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Note 3. Specification under output current where the duty ≤ 70%.

The output current value that has changed the duty ratio lower than 70% can can be calculated with the following expression (when changing the duty ratio to n%).

15. 30.4 AC Characteristics

(T_A = −40 to +105°C, **2.4 V ≤ AV_{DD} ≤ 3.6 V,** 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Correct:

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

(T_A = −40 to +105°C, AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)