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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A060A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G14 Descriptions in the Hardware User's Manual Rev. 3.20 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G14 R5F104xxx	Lot No. All lots	Reference Document	RL78/G14 User's Manual: Hardware Rev.3.20 R01UH0186EJ0320 (Jan. 2015)		

This document describes misstatements found in the RL78/G14 User's Manual: Hardware Rev.3.20 (R01UH0186EJ0320).

Corrections

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Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

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Incorrect,OLD: Bold with underline; Correct,NEW: Gray hatched

Revision History

RL78/G14 User's Manual: Hardware Rev.3.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A060A/E	Apr. 21, 2016	First edition issued No.1 to 39 in corrections (This notice)

1. 2.1.1 30-pin (Code Flash Memory 16 KB to 64 KB)(Page 57)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
(Omitted)					

2. 2.1.2 32-pin (Code Flash Memory 16 KB to 64 KB) (Page 59)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

3. 2.1.3 36-pin (Code Flash Memory 16 KB to 64 KB) (Page 61)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

4. 2.1.4 40-pin (Code Flash Memory 16 KB to 64 KB) (Page 63)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

5. 2.1.5 44-pin (Code Flash Memory 16 KB to 64 KB) (Page 65)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

6. 2.1.6 48-pin (Code Flash Memory 16 KB to 64 KB) (Page 67)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

7. 2.1.7 52-pin (Code Flash Memory 16 KB to 64 KB) (Page 69)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

8. 2.1.8 64-pin (Code Flash Memory 16 KB to 64 KB) (Page 71)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

9. 2.1.9 30-pin (Code Flash Memory 96 KB to 256 KB)(Page 73)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
(Omitted)					

10. 2.1.10 32-pin (Code Flash Memory 96 KB to 256 KB) (Page 75)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{SSI00}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{SSI00}$	
(Omitted)					

11. 2.1.11 36-pin (Code Flash Memory 96 KB to 64 KB) (Page 77)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

12. 2.1.12 40-pin (Code Flash Memory 96 KB to 256 KB) (Page 79)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P62 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
(Omitted)					

13. 2.1.13 44-pin (Code Flash Memory 96 KB to 256 KB) (Page 81)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

14. 2.1.14 48-pin (Code Flash Memory 96 KB to 256 KB) (Page 83)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

15. 2.1.15 52-pin (Code Flash Memory 96 KB to 256 KB) (Page 85)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

16. 2.1.16 64-pin (Code Flash Memory 96 KB to 256 KB) (Page 87)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance).
P61				SDAA0	
P62				$\overline{\text{SSI00}}$	
P63				—	
(Omitted)					

17. 2.1.17 80-pin (Page 89)

Pin Type revised

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance). For P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting at the input port.
P61				SDAA0	
P62				$\overline{\text{SSI00}}$/SCLA1	
P63				SDAA1	
P64	7-1-3			TI10/TO10	
P65				TI11/TO11	
P66				TI12/TO12	
P67				TI13/TO13	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance). For P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting at the input port.
P61				SDAA0	
P62				$\overline{\text{SSI00}}$/SCLA1	
P63				SDAA1	
P64	7-1-3			TI10/TO10	
P65				TI11/TO11	
P66				TI12/TO12	
P67				TI13/TO13	
(Omitted)					

18. 2.1.17 100-pin (Page 92)

Pin Type revised

Incorrect:

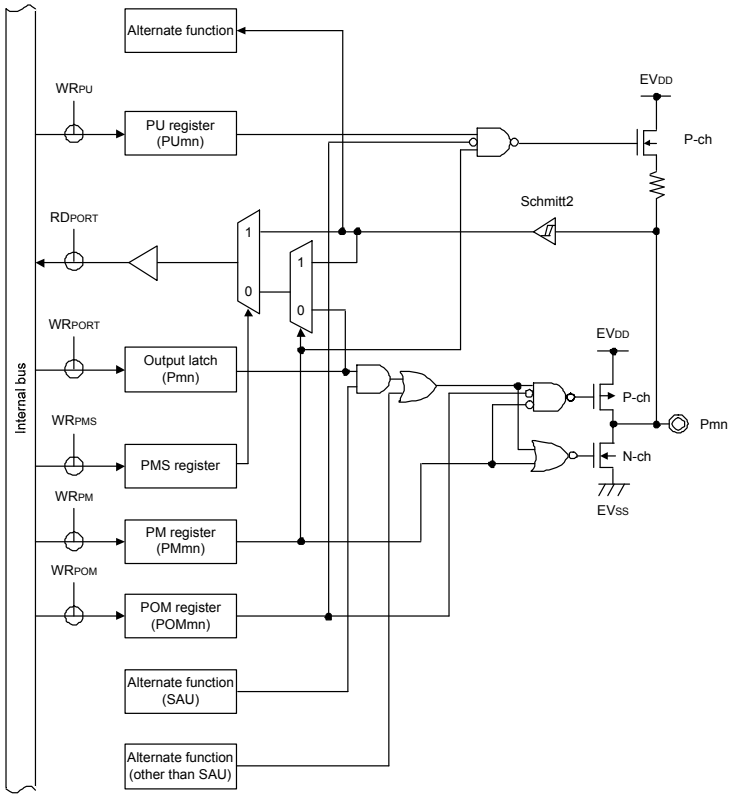
Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	~~12-1-2~~	I/O	Input port	SCLA0	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance). For P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting at the input port.
P61				SDAA0	
P62				$\overline{\text{SSI00}}$/SCLA1	
P63				SDAA1	
P64	7-1-3			TI10/TO10	
P65				TI11/TO11	
P66				TI12/TO12	
P67				TI13/TO13	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P60	12-1-5	I/O	Input port	SCLA0	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6V tolerance). For P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting at the input port.
P61				SDAA0	
P62				$\overline{\text{SSI00}}$/SCLA1	
P63				SDAA1	
P64	7-1-3			TI10/TO10	
P65				TI11/TO11	
P66				TI12/TO12	
P67				TI13/TO13	
(Omitted)					

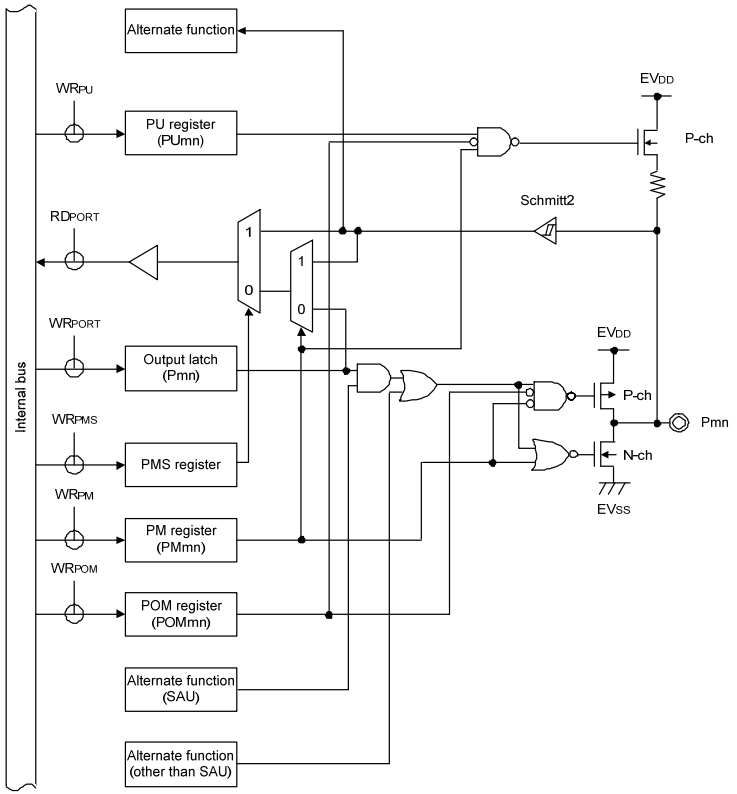
19. 2.4 Pin Block Diagrams
Figure 2-8 Pin Block Diagram of Pin Type7-1-4(Page 107)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

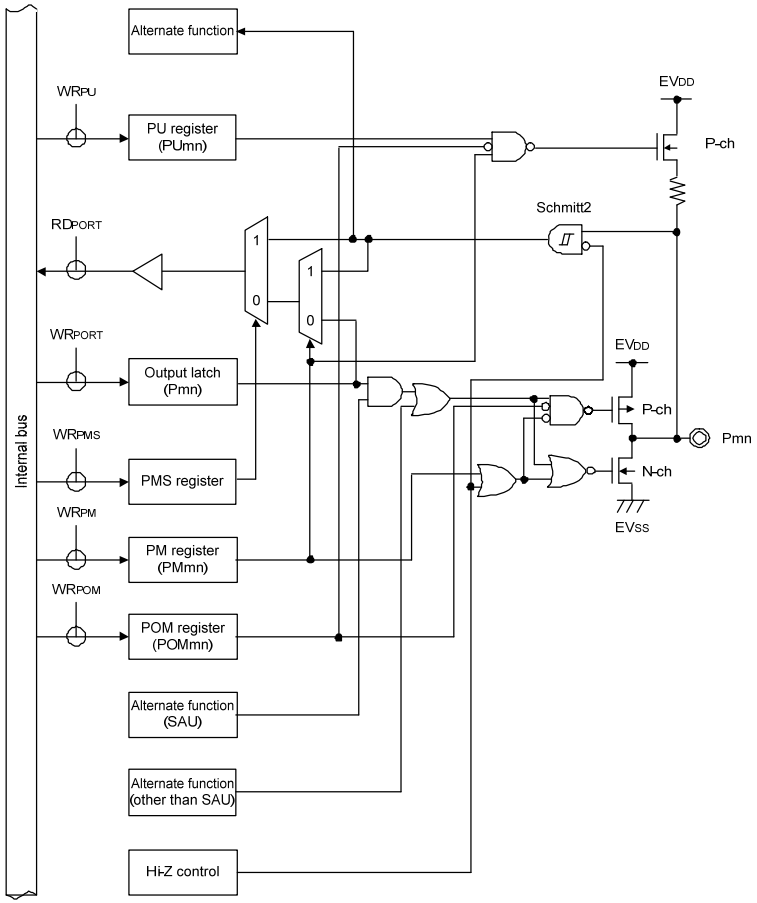


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

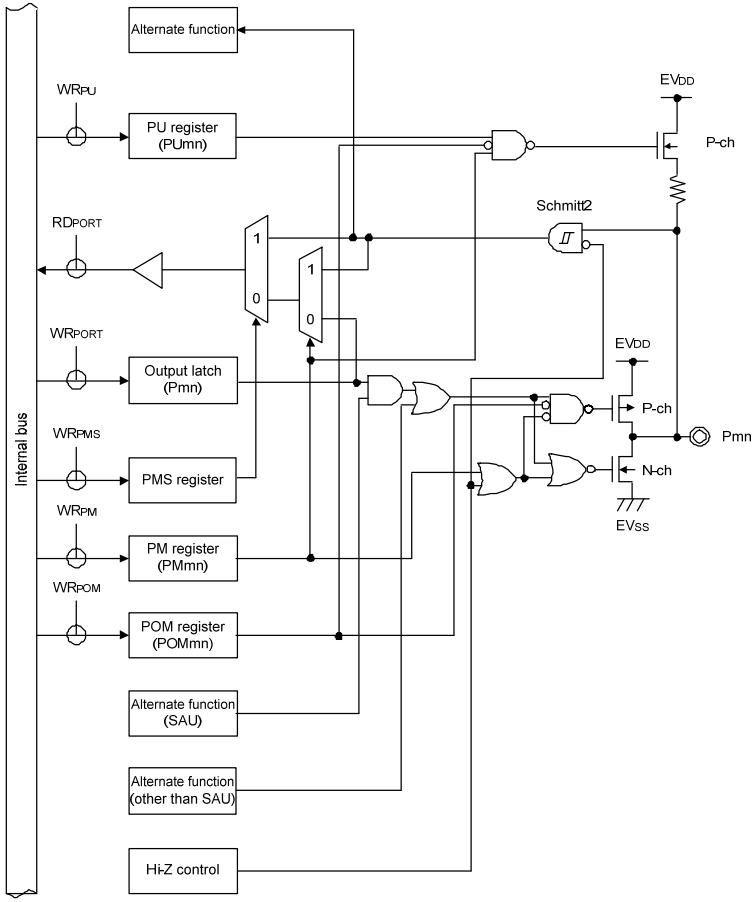
20. 2.4 Pin Block Diagrams
Figure 2-10 Pin Block Diagram of Pin Type7-1-8(Page 109)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

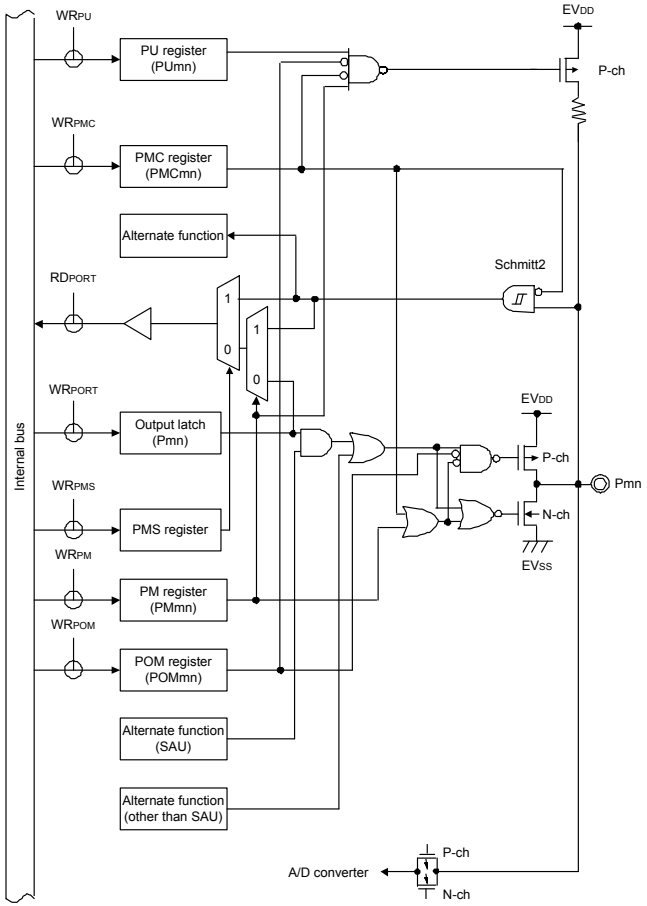


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

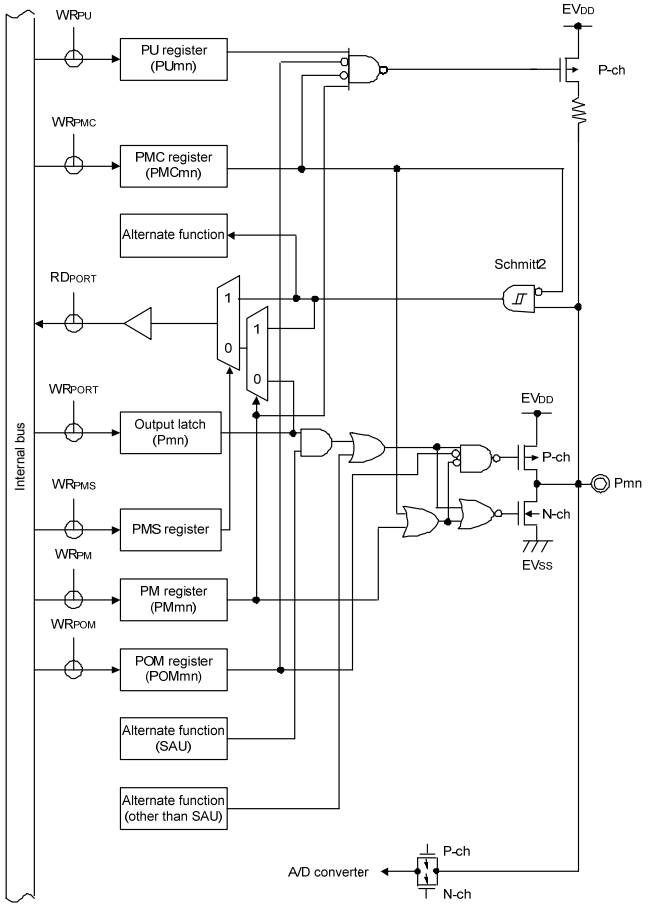
21. 2.4 Pin Block Diagrams
Figure 2-12 Pin Block Diagram of Pin Type7-3-4(Page 111)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

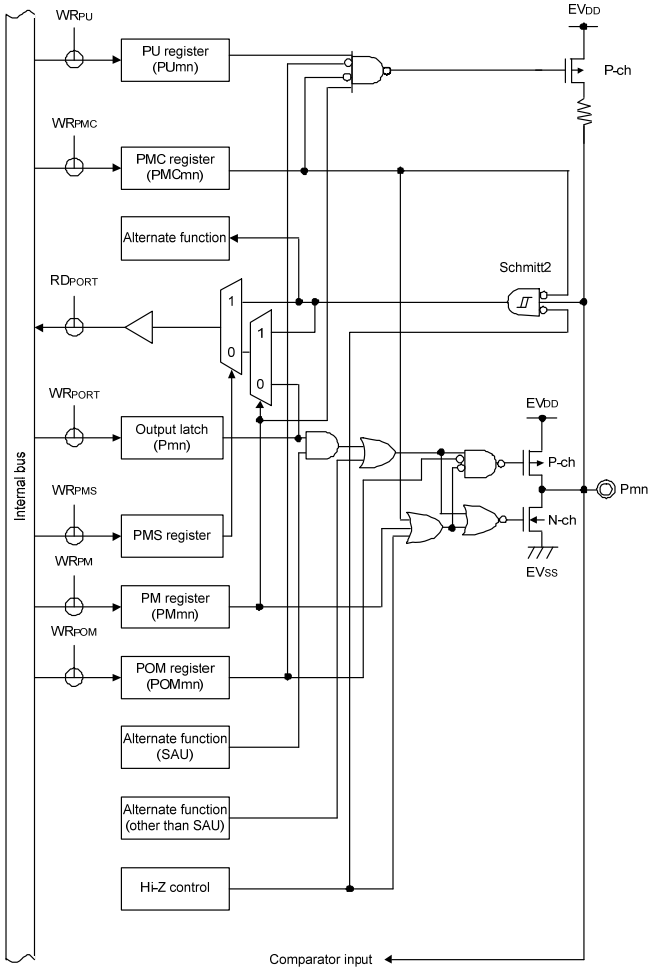


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

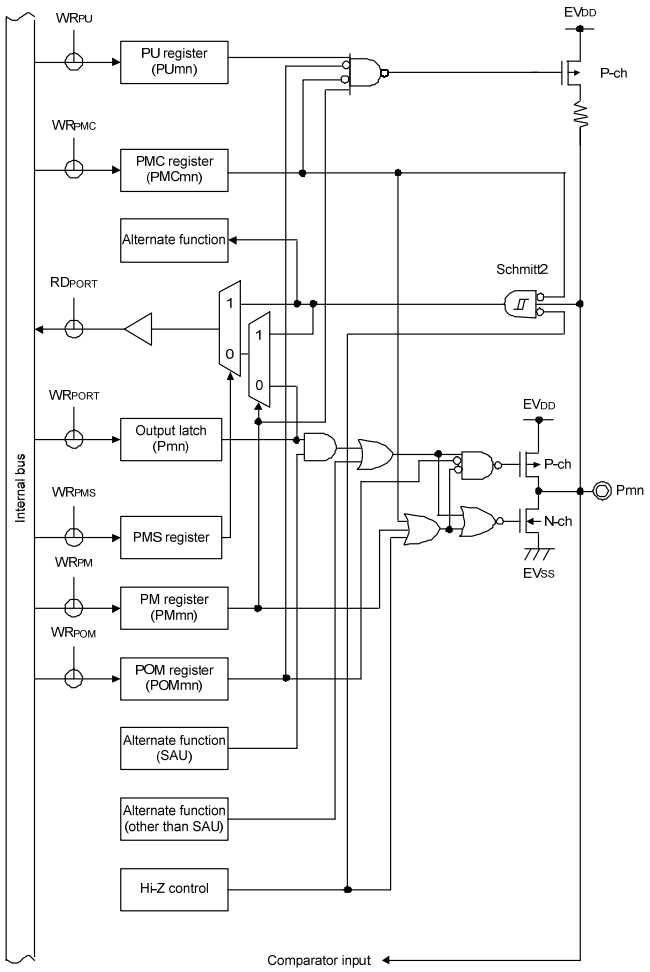
22. 2.4 Pin Block Diagrams
Figure 2-14 Pin Block Diagram of Pin Type7-3-4(Page 113)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

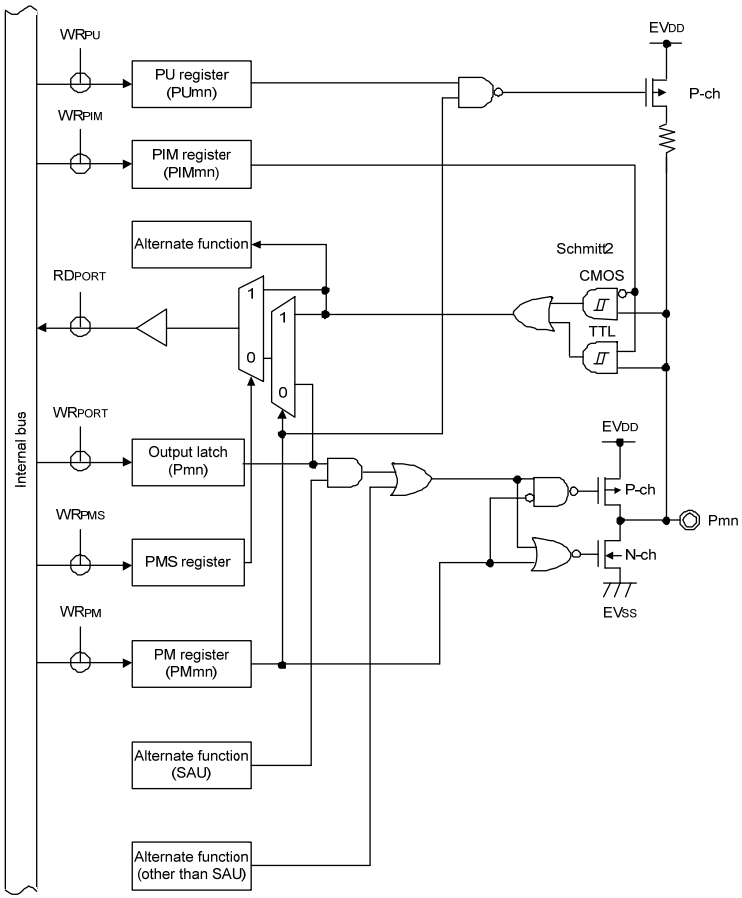


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

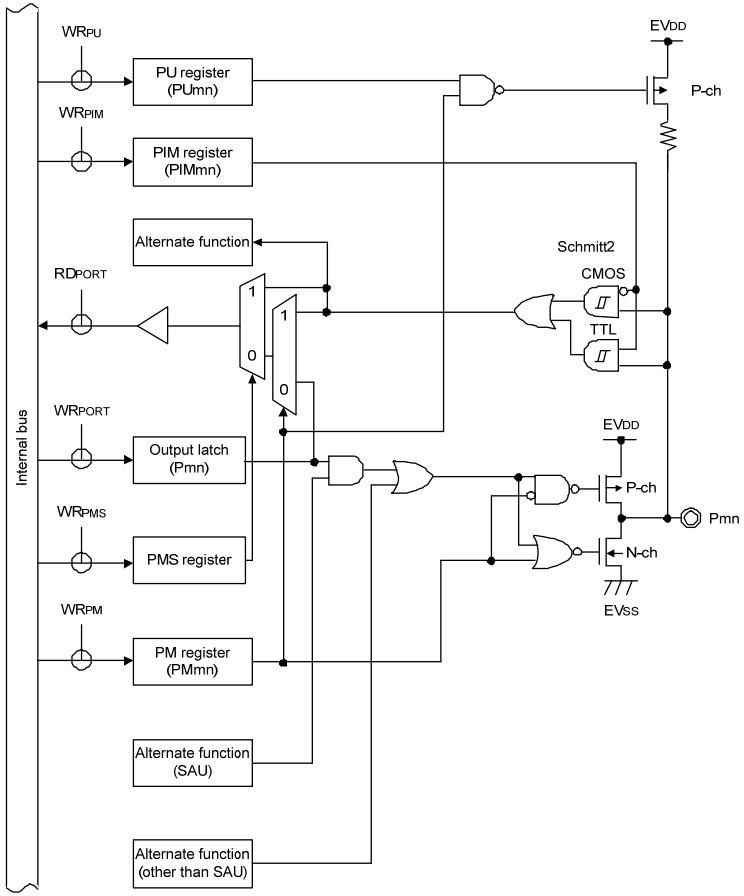
23. 2.4 Pin Block Diagrams
Figure 2-15 Pin Block Diagram of Pin Type8-1-3(Page 114)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

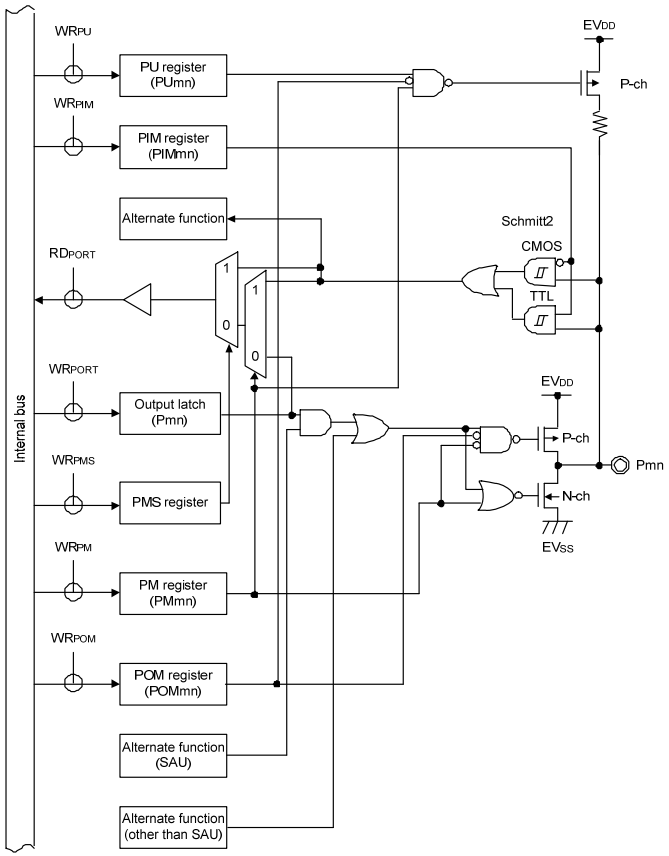


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

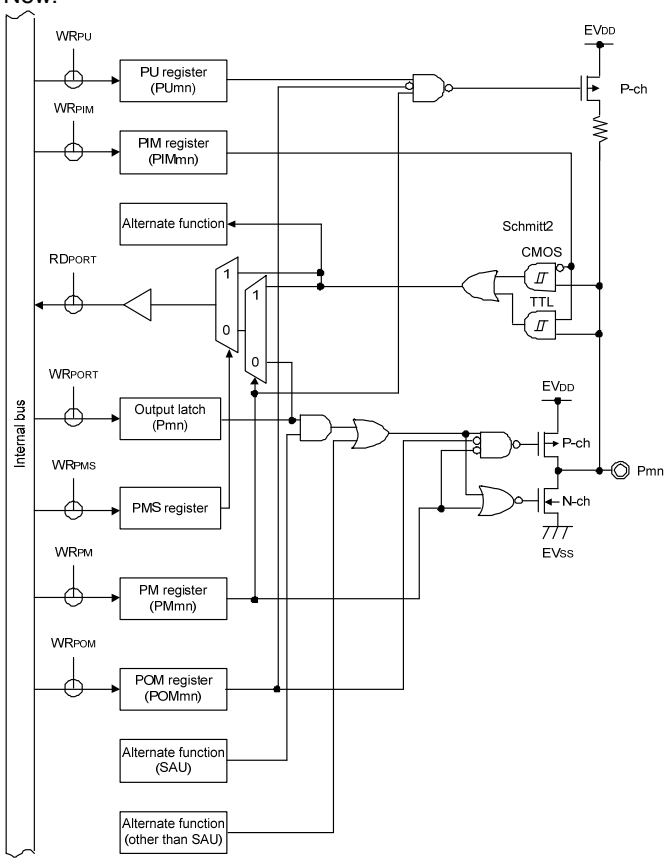
24. 2.4 Pin Block Diagrams
Figure 2-16 Pin Block Diagram of Pin Type8-1-4(Page 115)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:



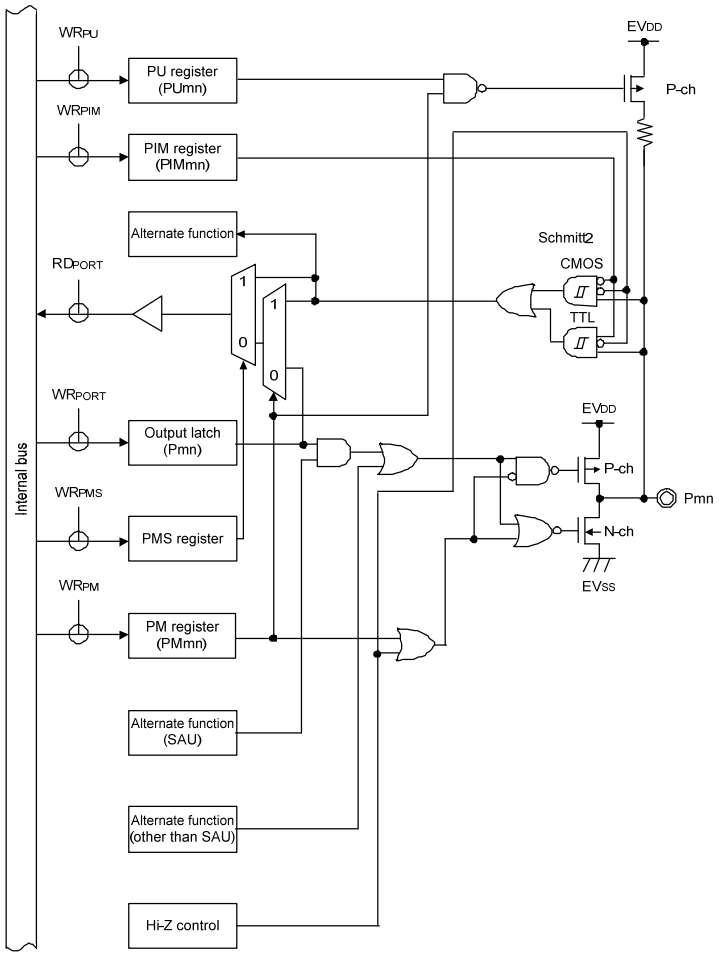
Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

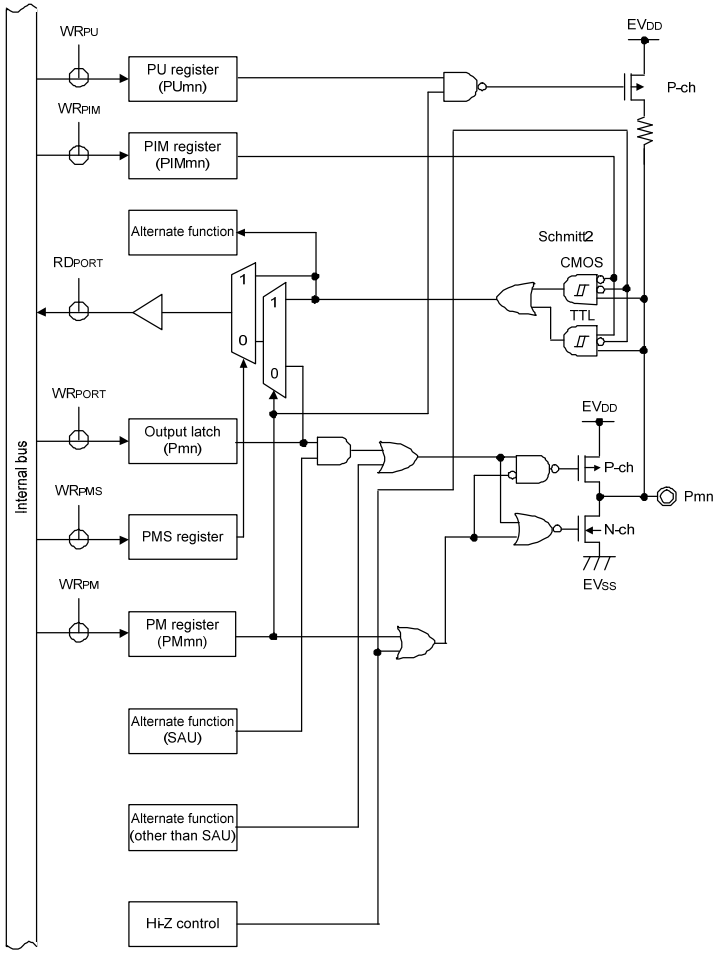
25. 2.4 Pin Block Diagrams
Figure 2-17 Pin Block Diagram of Pin Type8-1-7(Page 116)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

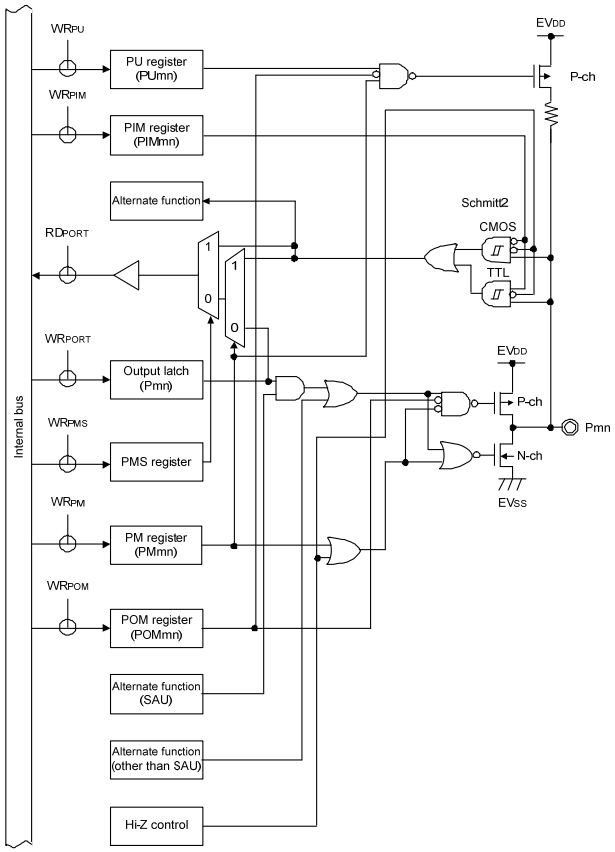


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

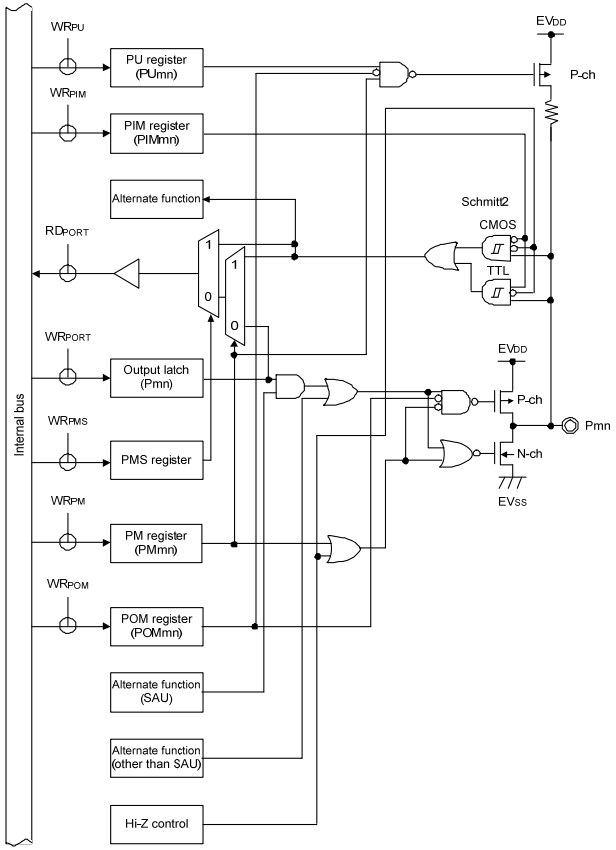
26. 2.4 Pin Block Diagrams
Figure 2-18 Pin Block Diagram of Pin Type8-1-8(Page 117)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:



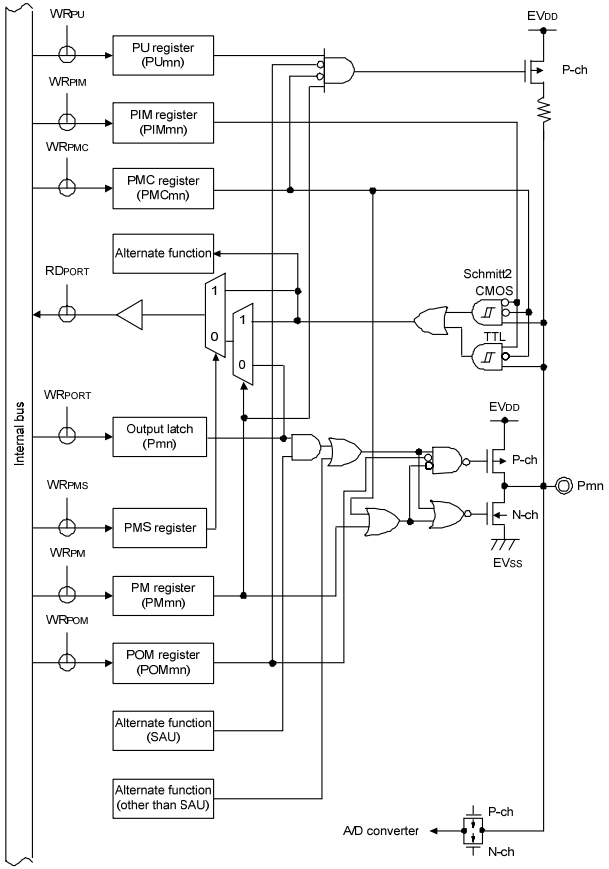
Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

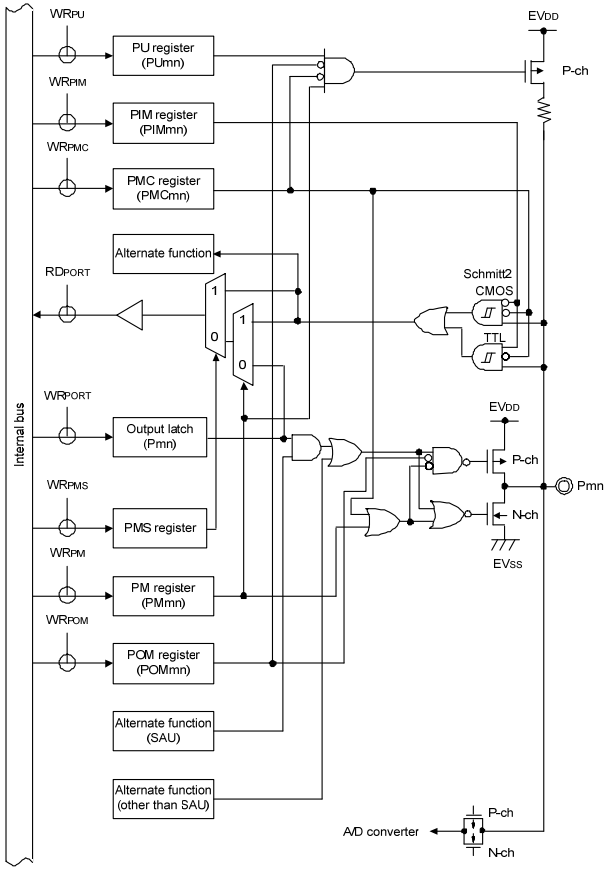
27. 2.4 Pin Block Diagrams
Figure 2-19 Pin Block Diagram of Pin Type8-3-4(Page 118)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:



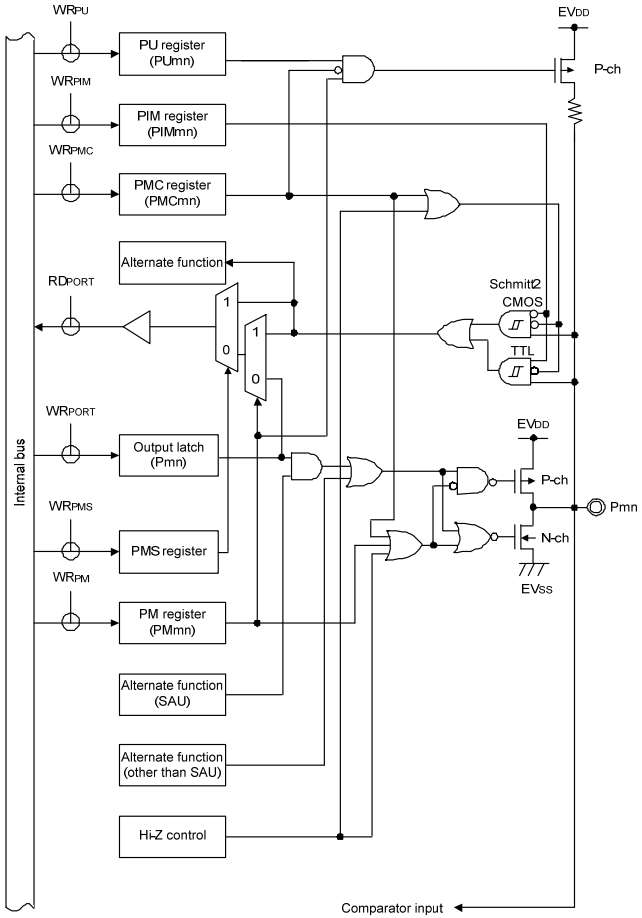
Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

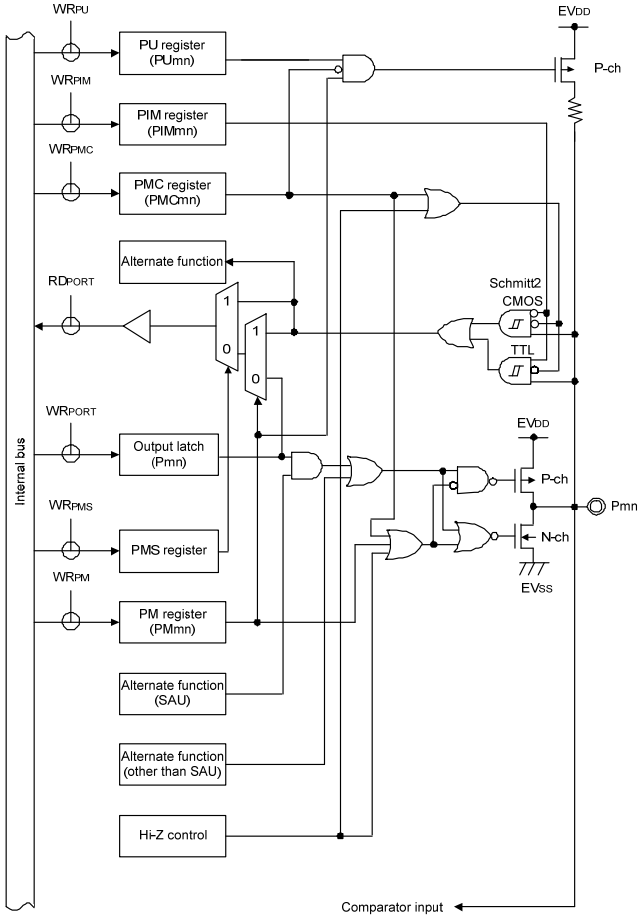
28. 2.4 Pin Block Diagrams
Figure 2-20 Pin Block Diagram of Pin Type8-6-6(Page 119)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:

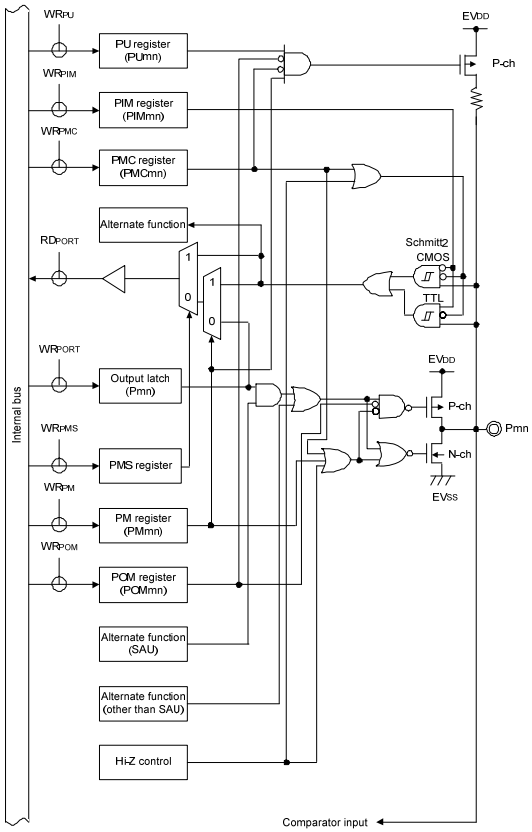


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

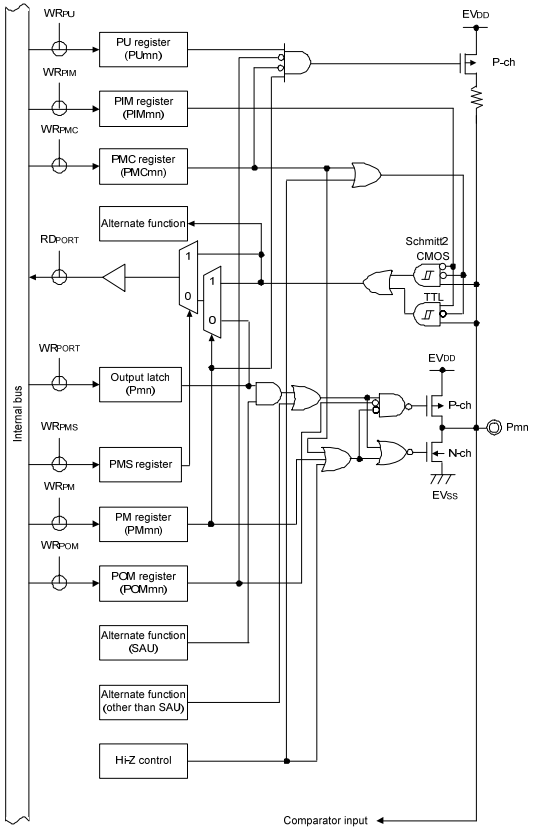
29. 2.4 Pin Block Diagrams
Figure 2-21 Pin Block Diagram of Pin Type8-6-8(Page 120)

Old:



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

New:



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

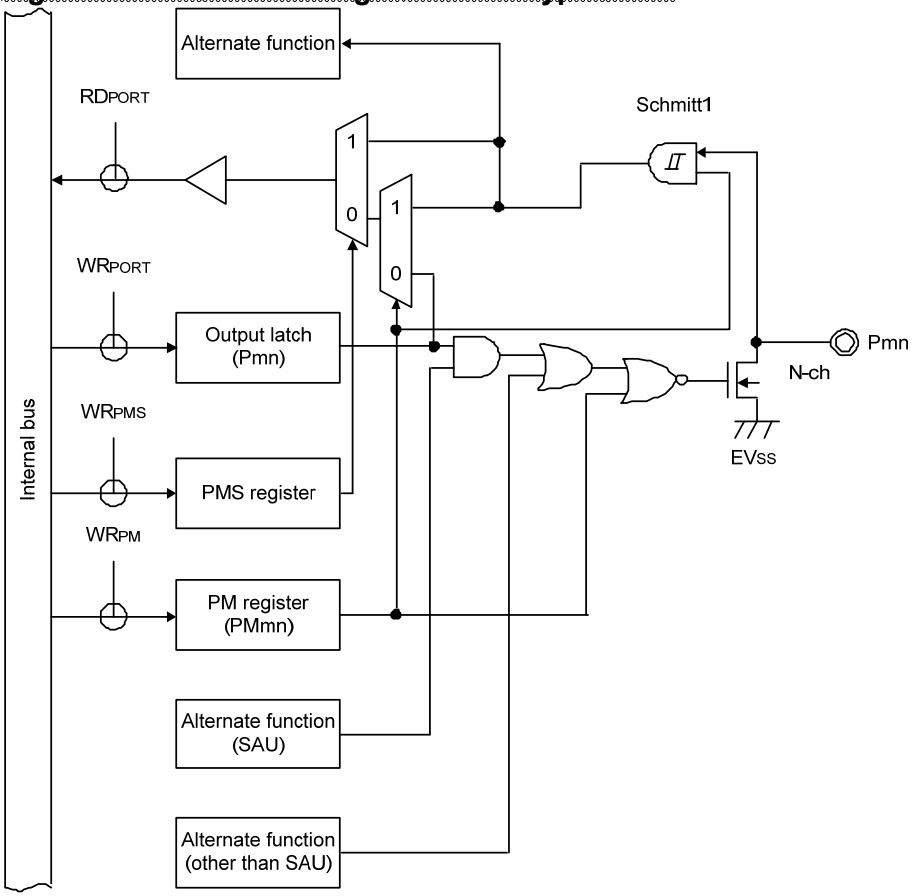
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

30. 2.4 Pin Block Diagrams
Figure 2-22 Pin Block Diagram of Pin Type12-1-2(Page 121)

Incorrect:

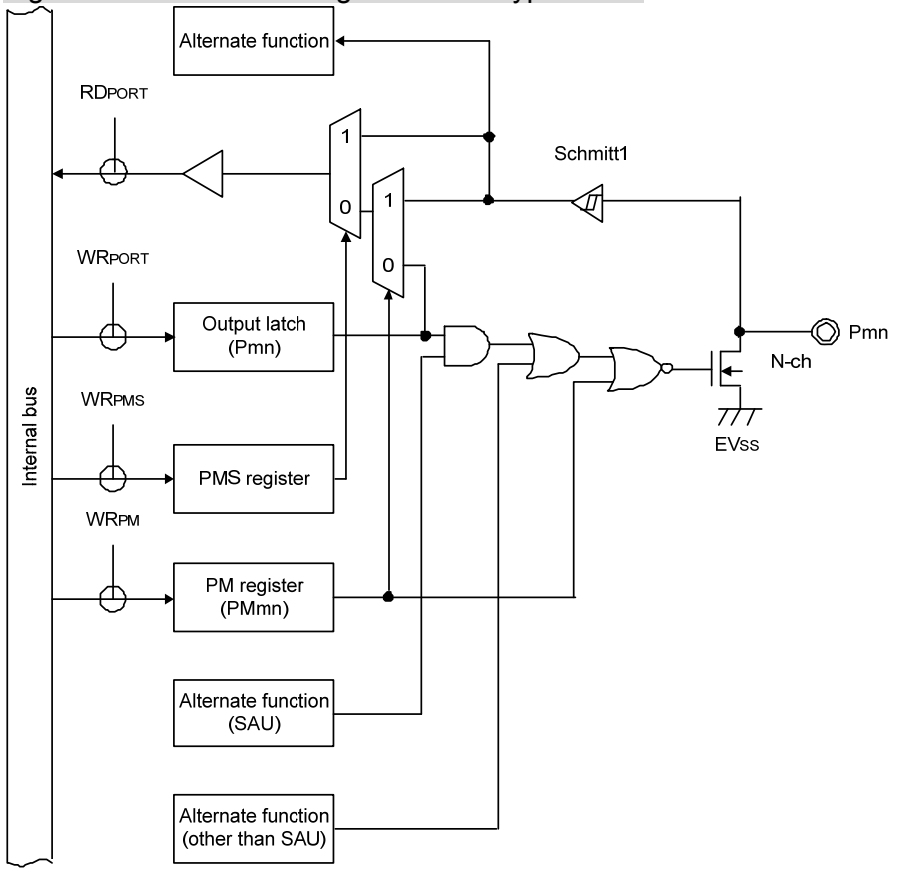
Figure 2-22 Pin Block Diagram of Pin Type12-1-2



Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

Correct:

Figure 2-22 Pin Block Diagram of Pin Type12-1-5



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is turned on when the pin is in output mode.

Remark 1. Refer to **2.1 Port Functions** for alternate functions.
Remark 2. SAU: Serial array unit

31. 4.5.3 Register setting examples for used port and alternate functions

Table4-17 Setting Examples of Registers When Using P30 to P120 Pin Function (1/6)(Page 225)

Incorrect:

Pin name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
	Function Name	I/O						SAU Output Function	Other Than SAU										
(Omitted)																			
P40	P40	Input	—	X	—	1	X	—	—	√	√	√	√	√	√	√	√	√	√
		Output	X	0	—	0	0/1	—	—										
(Omitted)																			

Correct:

Pin name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
	Function Name	I/O						SAU Output Function	Other Than SAU										
(Omitted)																			
P40	P40	Input	—	—	—	1	X	—	—	√	√	√	√	√	√	√	√	√	√
		Output	X	—	—	0	0/1	—	—										
(Omitted)																			

32. 8.3.9 Timer RD output control register (TRDOCR)

Figure 8 - 12 Format of Timer RD output control register (TRDOCR)
[Reset Synchronous PWM Mode, Complementary PWM Mode]

Old:

Nothing

New:

Figure 8 - 12 Format of Timer RD output control register (TRDOCR)
[Reset Synchronous PWM Mode, Complementary PWM Mode]

Address: F0269H After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0

TOD1,TOC1,TOB1, TOA1,TOD0, TOB0, TOA0	Setting these bits to 1 is invalid in the reset synchronous PWM mode and complementary PWM mode. Be sure to set these bits to 0. In the reset synchronous PWM mode and complementary PWM mode, the setting of the OLS1 and OLS0 bits in TRDFCR determine the initial level independently of the setting in these bits.

TOC0	TRDIOC1 initial output level select Note 2	
0	Initial output L	In the reset synchronous PWM mode, the output is inverted every PWM period. In complementary PWM mode, the output is inverted every 1/2 PWM period.
1	Initial output H	

Note 1. The value after reset is undefined when FRQSEL4 = 1 in the user option byte (000C2H) and TRD0EN = 0 in the PER1 register. If it is necessary to read the initial value, set fCLK to fIH and TRD0EN = 1 before reading.
Note 2. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

33. 8.3.11 Timer RD control register i (TRDCRi) (i = 0 or 1)

Figure8-18 Format of Timer RD control register 0 (TRDCR0) [Complementary PWM Mode](page 438)

Incorrect:

Figure8-18 Format of Timer RD control register 0 (TRDCR0)
[Complementary PWM Mode]

Address: F0270H After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0

(Omitted)

Correct:

Figure8-19 Format of Timer RD control register i (TRDCRi) (I = 0 or 1)
[Complementary PWM Mode]

Address: F0270H(TRDCR0), F0280H(TRDCR1) After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDCRi	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0

(Omitted)

34. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)

Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Reset Synchronous PWM Mode and PWM3 Mode](Page 454)

Incorrect:

Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Reset Synchronous PWM Mode and PWM3 Mode]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 32 Format of Timer RD counter 0 (TRD0)
[Reset Synchronous PWM Mode and PWM3 Mode]

Address: F0276H (TRD0) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD0																

(Omitted)

35. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)

Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Complementary PWM Mode (TRD0)] (Page 455)

Incorrect:

Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD0)]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 33 Format of Timer RD counter 0 (TRD0)
[Complementary PWM Mode (TRD0)]

Address: F0276H (TRD0) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD0																

(Omitted)

36. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)

Figure 8 - 33 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Complementary PWM Mode (TRD1)](Page 455)

Incorrect:

Figure 8 - 33 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD1)]

Address: F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 34 Format of Timer RD counter 1 (TRD1)
[Complementary PWM Mode (TRD1)]

Address: F0286H (TRD1) After Reset: 0000H Note R/W

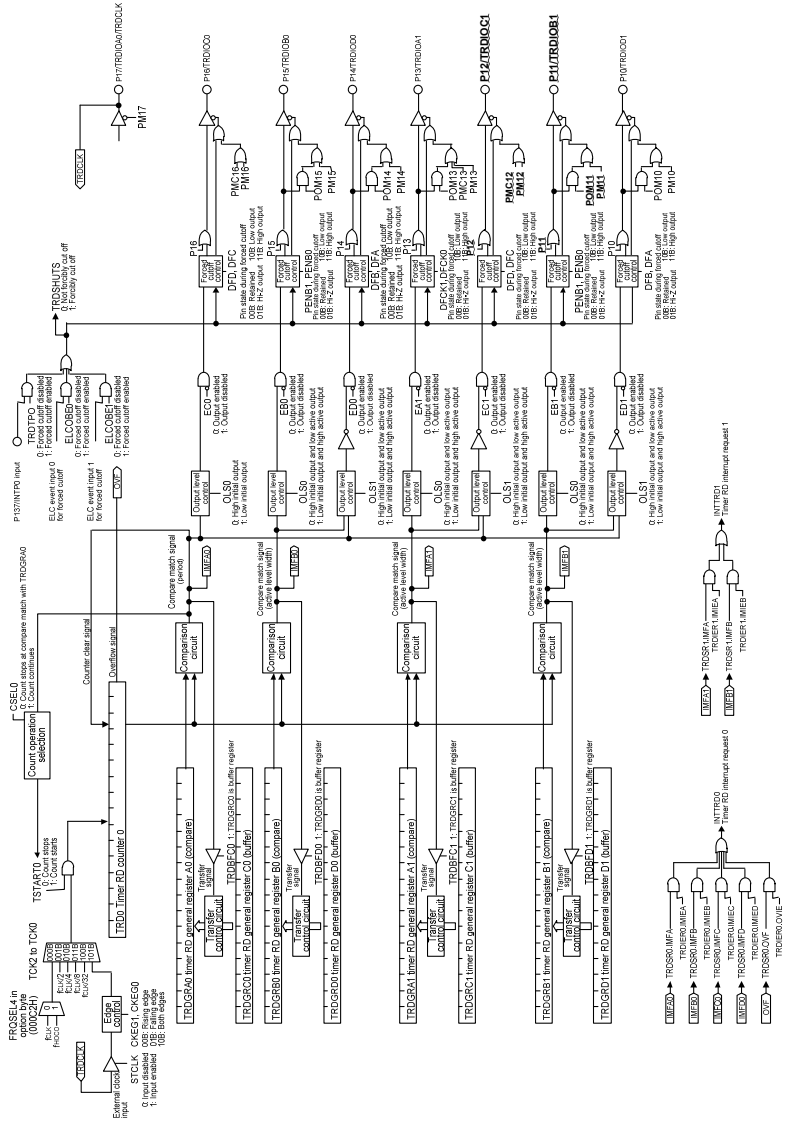
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD1																

(Omitted)

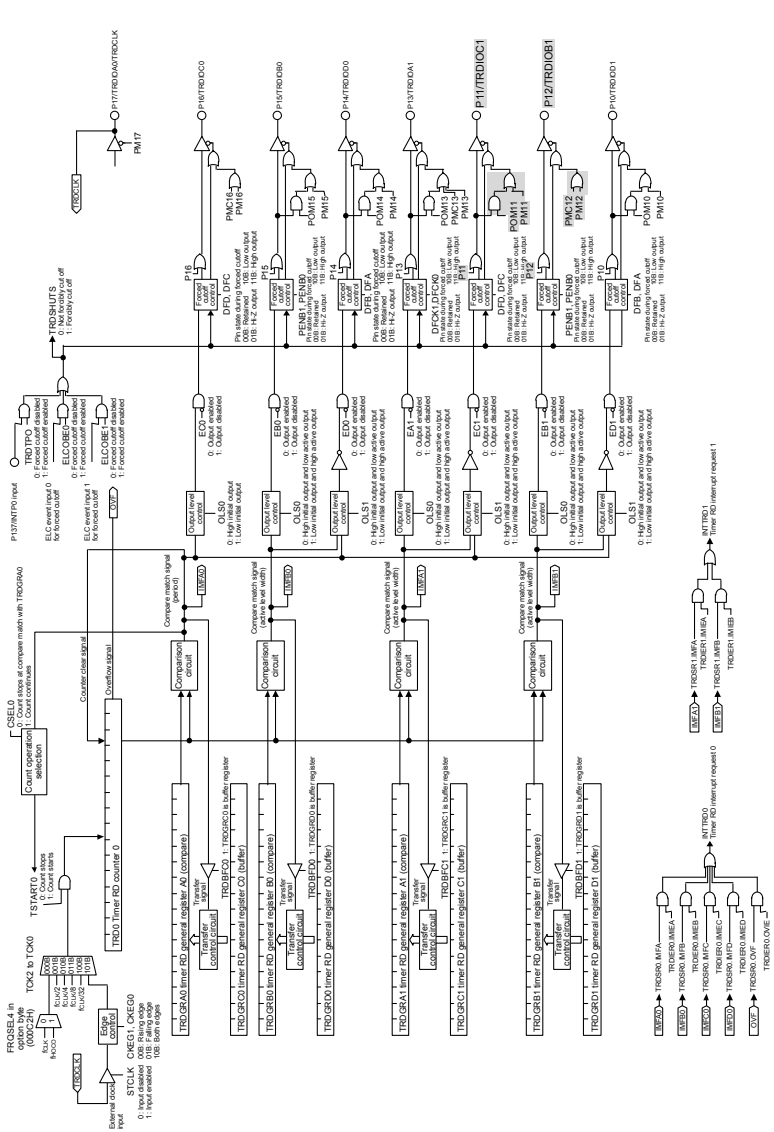
37. 8.5.4 Reset Synchronous PWM Mode

Figure 8 - 56 Block Diagram of Reset Synchronous PWM Mode (Page 493)

Incorrect:



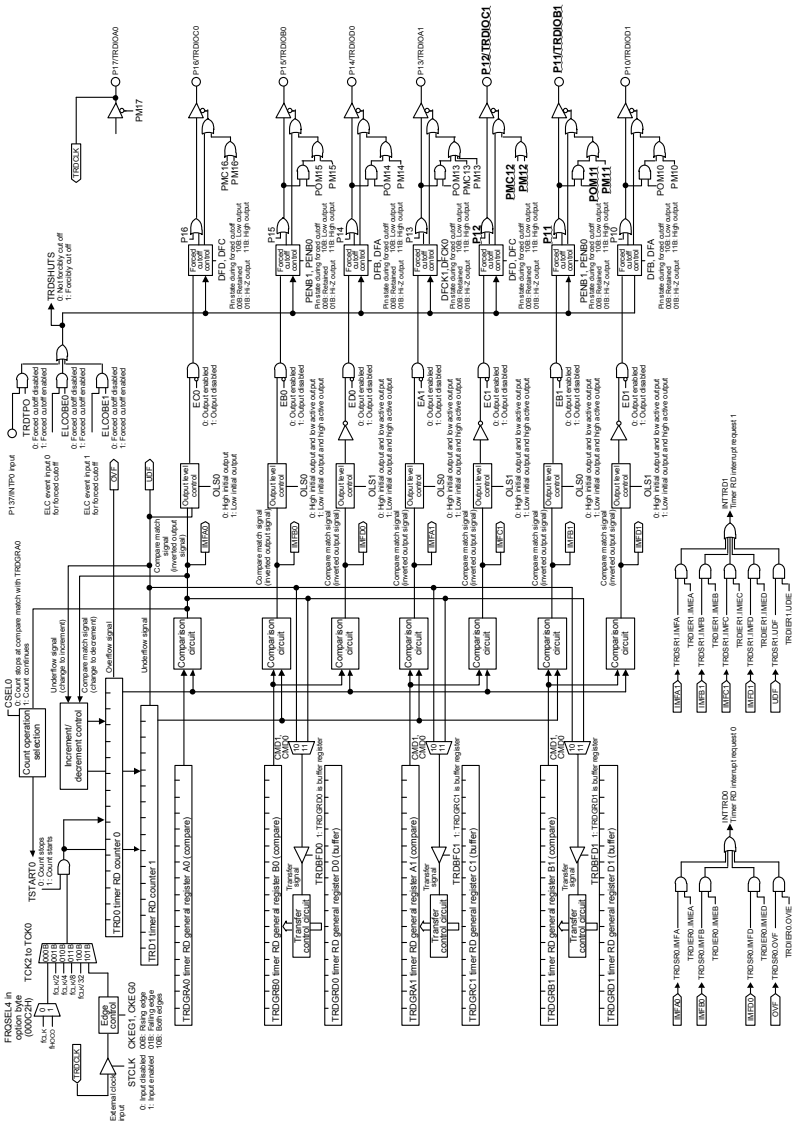
Correct:



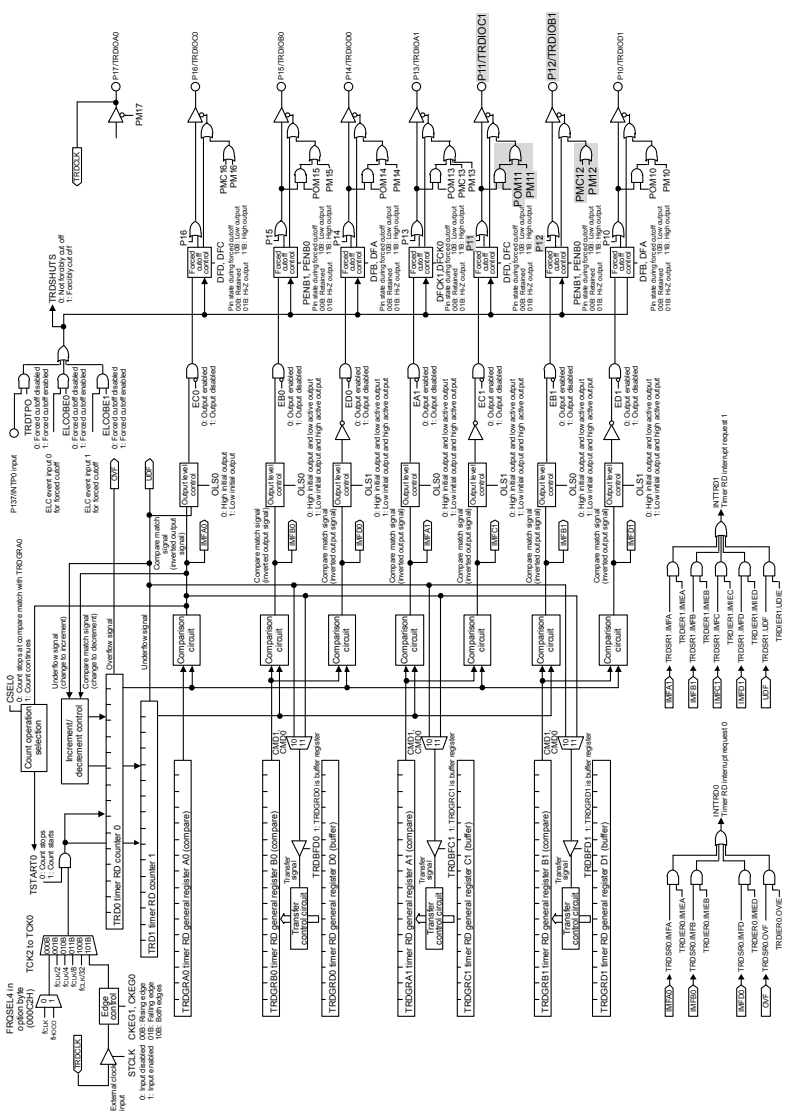
38. 8.5.5 Complementary PWM Mode

Figure 8 - 58 Block Diagram of Complementary PWM Mode (Page 497)

Incorrect:



Correct:



39. 35.3.2 Supply current characteristics

3) Flash ROM: 384 to 512 KB of 48- to 100-pin products (Page1251,1253)

T.B.D value fixed

Old:

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
(Omitted)									
Supply current Note1	I_{DD1}	Operating mode	Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.2	T.B.D	µA
						Resonator connection		5.2	T.B.D	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.9	T.B.D	
						Resonator connection		6.0	T.B.D	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		15.5	T.B.D	
						Resonator connection		15.5	T.B.D	
(Omitted)									

New:

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
(Omitted)										
Supply current Note1	I_{DD1}	Operating mode	Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.2	7.7	µA
						Resonator connection		5.2	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		15.5	77.8	
						Resonator connection		15.5	77.8	
(Omitted)										

Old:

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note1	I_{DD1} Note2	Halt mode	HS (high-speed main) mode Note7	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.93	TBD	mA
					V_{DD} = 3.0 V		0.93	TBD	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.5	TBD	
					V_{DD} = 3.0 V		0.5	TBD	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.72	TBD	
					V_{DD} = 3.0 V		0.72	TBD	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	TBD	
					V_{DD} = 3.0 V		0.42	TBD	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	TBD	
					V_{DD} = 3.0 V		0.39	TBD	
			HS (high-speed main) mode Note7	f_{MX} =20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	TBD	mA
					Resonator connection		0.41	TBD	
				f_{MX} =20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	TBD	
					Resonator connection		0.41	TBD	
				f_{MX} =10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21	TBD	
					Resonator connection		0.26	TBD	
				f_{MX} =10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	TBD	
					Resonator connection		0.26	TBD	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = -40°C	Square wave input		0.31	TBD	µA
					Resonator connection		0.50	TBD	
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.38	TBD	
					Resonator connection		0.57	TBD	
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.47	TBD	
					Resonator connection		0.70	TBD	
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.80	TBD	
					Resonator connection		1.00	TBD	
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		1.65	TBD	
					Resonator connection		1.84	TBD	
				f_{SUB} = 32.768 kHz Note 5, T_A = +105°C	Square wave input		8.00	TBD	
					Resonator connection		8.00	TBD	

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New:

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note1	I_{DD1} Note2	Halt mode	HS (high-speed main) mode Note7	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.93	5.16	mA
					V_{DD} = 3.0 V		0.93	5.16	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.5	4.47	
					V_{DD} = 3.0 V		0.5	4.47	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.72	4.08	
					V_{DD} = 3.0 V		0.72	4.08	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	3.51	
					V_{DD} = 3.0 V		0.42	3.51	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	2.38	
					V_{DD} = 3.0 V		0.39	2.38	
			HS (high-speed main) mode Note7	f_{MX} =20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	2.83	mA
					Resonator connection		0.41	2.92	
				f_{MX} =20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	2.83	
					Resonator connection		0.41	2.92	
				f_{MX} =10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21	1.46	
					Resonator connection		0.26	1.57	
				f_{MX} =10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	1.46	
					Resonator connection		0.26	1.57	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = -40°C	Square wave input		0.31	0.76	µA
					Resonator connection		0.50	0.95	
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.38	0.76	
					Resonator connection		0.57	0.95	
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.47	3.59	
					Resonator connection		0.70	3.78	
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.80	6.20	
					Resonator connection		1.00	6.39	
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		1.65	10.56	
					Resonator connection		1.84	10.75	
				f_{SUB} = 32.768 kHz Note 5, T_A = +105°C	Square wave input		8.00	65.7	
					Resonator connection		8.00	65.7	

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Old:

Supply current Note1	I_{DD3} Note6	STOP MODE Note8	T_A = -40°C		0.19	TBD	µA
			T_A = +25°C		0.30	TBD	
			T_A = +50°C		0.41	TBD	
			T_A = +70°C		0.80	TBD	
			T_A = +85°C		1.53	TBD	
			T_A = +105°C		6.50	TBD	

(Omitted)

New:

Supply current Note1	I_{DD3} Note6	STOP MODE Note8	T_A = -40°C		0.19	0.63	µA
			T_A = +25°C		0.30	0.63	
			T_A = +50°C		0.41	3.47	
			T_A = +70°C		0.80	6.08	
			T_A = +85°C		1.53	10.44	
			T_A = +105°C		6.50	67.14	

(Omitted)