RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A001A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G13 Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G13 Group R5F100xxx, R5F101xxx	Lot No.	Reference Document	RL78/G13 User's Manual: Hardware Rev. 1.00 R01UH0146EJ0100 (Sep. 2011)		
		All lot				

This document describes misstatements found in the RL78 hardware user's manual Rev. 1.00 (R01UH0146EJ0100).

Corrections

Applicable Page	Applicable Item	Contents
Pages 4, 17, 1055	64-pin plastic TQFP (7 x 7)	Incorrect descriptions deleted
Pages 439 to 444	Count registers in real-time clock	Incorrect descriptions deleted
Page 460	Interval timer control register (ITMC)	Explanations added
Page 483	Timing chart when A/D voltage comparator is used	Explanations added
Pages 489 to 491	A/D conversion time selection, there is stabilization wait time (6/8) to (8/8)	Incorrect descriptions revised
Pages 493, 497	Notes when entering A/D converter standby mode	Explanations added
Pages 842, 844	Maskable interrupt request acknowledgment	Incorrect descriptions revised
Pages 894, 896	Timing chart of voltage detector (LVD)	Incorrect descriptions revised
Pages 897 to 899	Voltage detector (LVD) interrupt and reset mode	Incorrect descriptions revised
Page 1005	Number (4) of the supply current characteristics in the Electrical Specifications chapter (section 29.4.2) is the same for all RL78/G13 Group products.	Explanations added

Incorrect: Bold with underline; Correct: Gray hatched

Document Improvement

The above corrections will be made for the next revision of the hardware user's manual around February, 2012. Contact a Renesas Electronics sales department details on the publishing schedule.

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Corrections in the hardware User's manual

No	Applicable Item			Rev 1.00	After Rev 2.00[Note]
	Document No.	Japanese		R01UH0146JJ0100	R01UH0146JJ0200
		English		R01UH0146EJ0100	R01UH0146EJ0200
1	Incorrect descriptions of 64-pin plastic TQFP (7 x 7) deleted			−	√
2	Incorrect descriptions of count registers, in real-time clock deleted			−	√
3	Explanations of interval timer control register (ITMC) added			−	√
4	Explanations of timing chart when A/D voltage comparator is used added			−	√
5	Incorrect descriptions of A/D conversion time selection, there is stabilization wait time (6/8) to (8/8) revised			−	√
6	Explanations when entering A/D converter standby mode added			−	√
7	Incorrect descriptions of maskable interrupt request acknowledgment operation			−	√
8	Incorrect descriptions of voltage detector (LVD) timing chart revised			−	√
9	Incorrect descriptions of voltage detector (LVD) interrupt and reset mode revised			−	√
10	Number (4) of the supply current characteristics in the Electrical Specifications chapter (section 29.4.2) is the same for all RL78/G13 Group products.			−	√

Note   A revised hardware user's manual is scheduled to be released around February, 2012.

Remarks   √: Corrected

              −: Items should be corrected

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1. **Descriptions of related information according to discontinued development of 64-pin plastic TQFP (7 x 7) package deleted**

Order information of 64-pin plastic TQFP (7 x 7) deleted (page 4)

Incorrect: (2/3)

Pin count	Package	Data flash	Part Number
			(Omitted)
64 pins	64-pin plastic LQFP (12x12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
	~~64-pin plastic TQFP (fine pitch) (7 × 7)~~	~~Mounted~~	~~R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAFC, R5F100LHAFC, R5F100LJAFC~~
		~~Not mounted~~	~~R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAFC, R5F101LHAFC, R5F101LJAFC~~
	64-pin plastic FBGA (4 × 4)	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
		Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG

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Correct: (2/3)

Pin count	Package	Data flash	Part Number
		(Omitted)	
64 pins	64-pin plastic LQFP (12x12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
	64-pin plastic FBGA (4 × 4)	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
		Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG

Pin configuration of 64-pin plastic TQFP (7 x 7) deleted (page 17)

Incorrect:

1.3.11 64-pin products

• 64-pin plastic LQFP (12 × 12)

• 64-pin plastic LQFP (fine pitch) (10 × 10)

• **64-pin plastic TQFP (fine pitch) (7 × 7)**

(Omitted)

Correct:

1.3.11 64-pin products

• 64-pin plastic LQFP (12 × 12)

• 64-pin plastic LQFP (fine pitch) (10 × 10)

(Omitted)

Package drawings of 64-pin plastic TQFP (7 x 7) deleted (page 1055)

Incorrect:

R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAFC, R5F100LHAFC, R5F100LJAFC
R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAFC, R5F101LHAFC, R5F101LJAFC

64-PIN PLASTIC TQFP (7x7)

Under development

Correct: Applicable page deleted

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2.   Incorrect descriptions of count registers in real-time clock deleted

Incorrect description of second count register (SEC) in real-time clock deleted (page 439)

Incorrect:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-count register overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f$_{RTC}$) later. Set a decimal value of 00 to 59 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-count register overflows. When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f$_{RTC}$) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

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Incorrect description of minute count register (MIN) in real-time clock deleted (page 439)

Incorrect:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of hour count register (HOUR) in real-time clock deleted (page 440)

Incorrect:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Correct:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Incorrect description of day count register (DAY) in real-time clock deleted (page 442)

Incorrect:

(8) Day count register (DAY)

    The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

    It counts up when the hour counter overflows.

    This counter counts as follows.

<div align="center">(Omitted)</div>

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. ~~**If a value outside the range is set, the register value returns to the normal value after 1 period.**~~

    The DAY register can be set by an 8-bit memory manipulation instruction.

    Reset signal generation clears this register to 01H.

Correct:

(8) Day count register (DAY)

    The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

    It counts up when the hour counter overflows.

    This counter counts as follows.

<div align="center">(Omitted)</div>

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.

    The DAY register can be set by an 8-bit memory manipulation instruction.

    Reset signal generation clears this register to 01H.

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Incorrect description of week count register (WEEK) in real-time clock deleted (page 443)

Incorrect:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of month count register (MONTH) in real-time clock deleted (page 444)

Incorrect:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Correct:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Incorrect description of year count register (YEAR) in real-time clock deleted (page 444)

Incorrect:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

3.   Caution of interval timer control register (ITMC) in 12-bit interval timer added (page 460)

Incorrect:

(3) Interval timer control register (ITMC)

(Omitted)

Cautions 1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt

servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.

2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.

3. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the

settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

Correct:

(3) Interval timer control register (ITMC)

(Omitted)

Cautions 1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt

servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt

servicing.

2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.

3. When setting the RINTE bit after returned from standby mode and entering standby mode again, confirm that the

written value of the RINTE bit is reflected, or wait that more than one clock of the count clock has elapsed after

returned from standby mode. Then enter standby mode.

4. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the

settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

4. Added Explanations of timing chart when A/D voltage comparator is used (page 483)

Incorrect:

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used
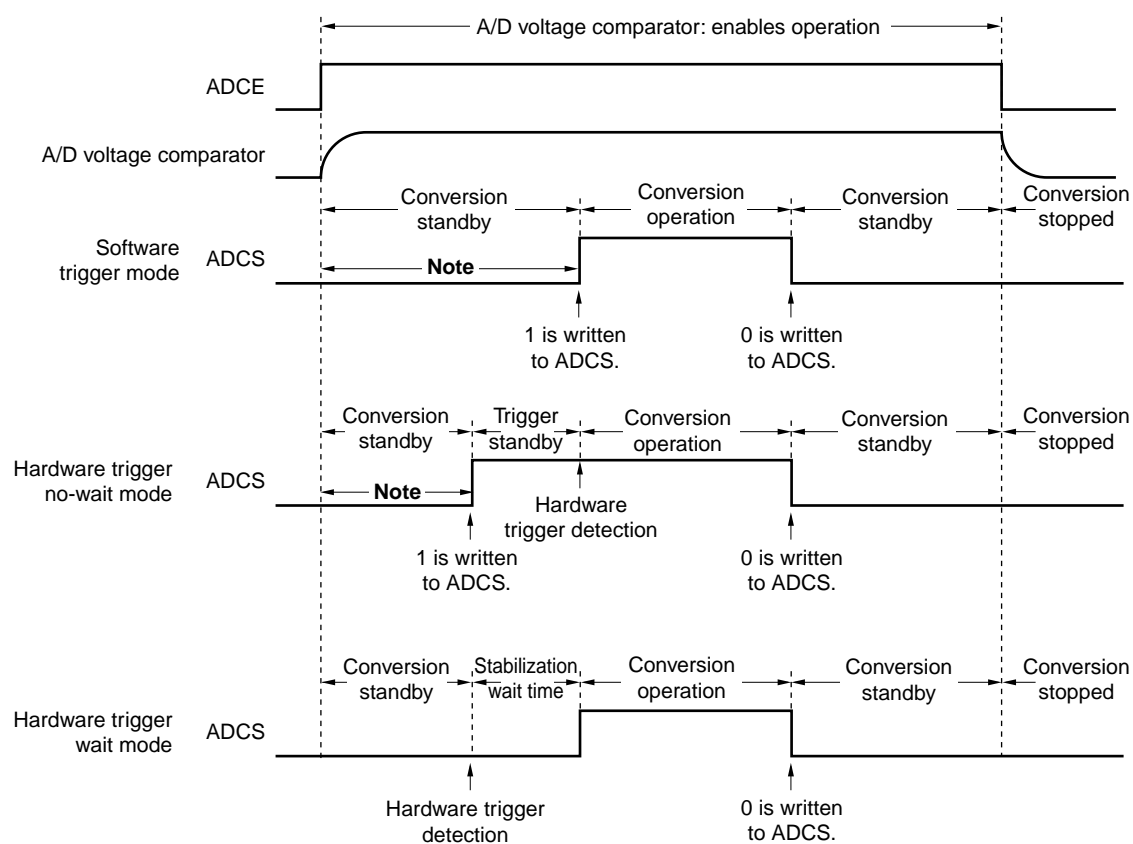
Note   (Omitted)

Correct:

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used
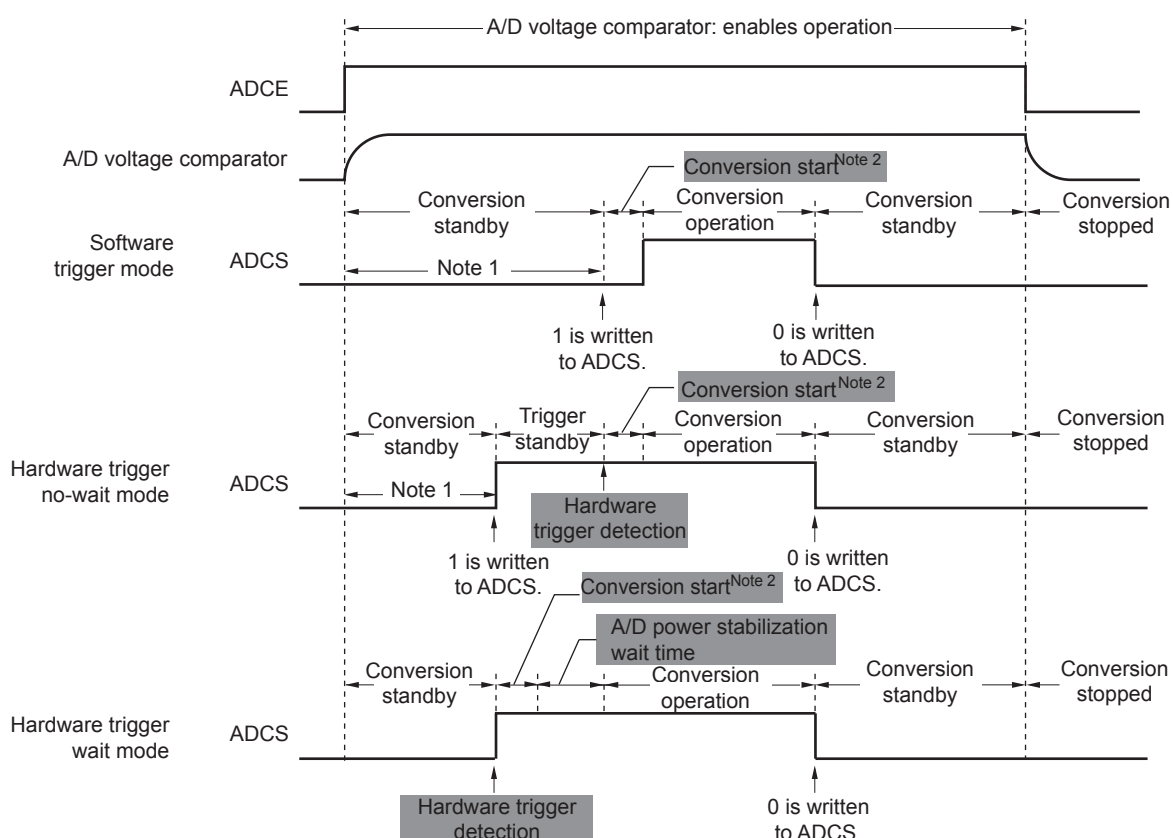
Note 1. (Omitted)

　　　2. The following time is the maximum amount of time necessary to start conversion.

ADM0			Conversion	Conversion Start Time (Number of f_{CLK} Clocks)	
FR2	FR1	FR0	Clock (f_{AD})	Software trigger mode/ Hardware trigger no wait mode	Hardware trigger wait mode
0	0	0	$f_{CLK}/64$	63	
0	0	1	$f_{CLK}/32$	31	
0	1	0	$f_{CLK}/16$	15	
0	1	1	$f_{CLK}/8$	7	
1	0	0	$f_{CLK}/6$	5	1
1	0	1	$f_{CLK}/5$	4	
1	1	0	$f_{CLK}/4$	3	
1	1	1	$f_{CLK}/2$	1	

Remark　f_{CLK}: CPU/peripheral hardware clock frequency

5. Incorrect descriptions of Table 11-3 A/D Conversion Time Selection (6/8) to (8/8) when there is stabilization wait time (pages 489 to 491)

Incorrect:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) 2.7 V $\leq$ V$_{DD}$ < 3.6 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f$_{AD}$)
FR2	FR1	FR0	LV1	LV0		f$_{CLK}$ = 1 MHz	f$_{CLK}$ = 2 MHz	f$_{CLK}$ = 4 MHz	f$_{CLK}$ = 8 MHz	f$_{CLK}$ = 16 MHz	f$_{CLK}$ = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	40.5 μs	20.25 μs	10.125 μs	5.0625 μs	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	33.75 μs	16.875 μs	8.4375 μs	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	f$_{CLK}$/4
1	1	1				54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	37.5 μs	18.75 μs	9.375 μs	4.6875 μs	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	31.25 μs	15.625 μs	7.8125 μs	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	f$_{CLK}$/4
1	1	1				50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	Setting prohibited	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	54 μs	27 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	40.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	33.75 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/4
1	1	1				54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	Setting prohibited	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	50 μs	25 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	37.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	31.25 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/4
1	1	1				50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/2

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Incorrect:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) 1.8 V ≤ VDD < 2.7 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (fAD)
FR2	FR1	FR0	LV1	LV0		fCLK = 1 MHz	fCLK = 2 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz (Note)	fCLK = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/64
0	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/32
0	1	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/16
0	1	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/64
0	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/32
0	1	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/16
0	1	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	fCLK/64
0	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	fCLK/32
0	1	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	Setting prohibited	fCLK/16
0	1	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	54 μs	27 μs	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	40.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	33.75 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	1	0	Low-Voltage 1	Setting prohibited	54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	1	0	Low-Voltage 1	54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	fCLK/64
0	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	fCLK/32
0	1	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	Setting prohibited	fCLK/16
0	1	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	50 μs	25 μs	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	37.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	31.25 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	1	1	Low-Voltage 2	Setting prohibited	50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	1	1	Low-Voltage 2	50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2

Note (Omitted)

Incorrect:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) 1.6 V ≤ V$_{DD}$ < 1.8 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f$_{AD}$)
FR2	FR1	FR0	LV1	LV0		f$_{CLK}$ = 1 MHz	f$_{CLK}$ = 2 MHz	f$_{CLK}$ = 4 MHz	f$_{CLK}$ = 8 MHz	f$_{CLK}$ = 16 MHz (Note 2)	f$_{CLK}$ = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/64
0	0	1										f$_{CLK}$/32
0	1	0										f$_{CLK}$/16
0	1	1										f$_{CLK}$/8
1	0	0										f$_{CLK}$/6
1	0	1										f$_{CLK}$/5
1	1	0										f$_{CLK}$/4
1	1	1										f$_{CLK}$/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/64
0	0	1										f$_{CLK}$/32
0	1	0										f$_{CLK}$/16
0	1	1										f$_{CLK}$/8
1	0	0										f$_{CLK}$/6
1	0	1										f$_{CLK}$/5
1	1	0										f$_{CLK}$/4
1	1	1										f$_{CLK}$/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	108 µs	Setting prohibited	f$_{CLK}$/64
0	0	1							108 µs			f$_{CLK}$/32
0	1	0						108 µs				f$_{CLK}$/16
0	1	1					108 µs					f$_{CLK}$/8
1	0	0					81 µs					f$_{CLK}$/6
1	0	1				135 µs	Setting prohibited					f$_{CLK}$/5
1	1	0				108 µs						f$_{CLK}$/4
1	1	1				Setting prohibited						f$_{CLK}$/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	100 µs	Setting prohibited	f$_{CLK}$/64
0	0	1							100 µs			f$_{CLK}$/32
0	1	0						100 µs				f$_{CLK}$/16
0	1	1					100 µs					f$_{CLK}$/8
1	0	0					Setting prohibited					f$_{CLK}$/6
1	0	1				125 µs						f$_{CLK}$/5
1	1	0				100 µs						f$_{CLK}$/4
1	1	1				Setting prohibited						f$_{CLK}$/2

Note (Omitted)

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Correct:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) 2.7 V ≤ V$_{DD}$ < 3.6 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f$_{AD}$)
FR2	FR1	FR0	LV1	LV0		f$_{CLK}$ = 1 MHz	f$_{CLK}$ = 2 MHz	f$_{CLK}$ = 4 MHz	f$_{CLK}$ = 8 MHz	f$_{CLK}$ = 16 MHz	f$_{CLK}$ = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	40.5 μs	20.25 μs	10.125 μs	5.0625 μs	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	33.75 μs	16.875 μs	8.4375 μs	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	f$_{CLK}$/4
1	1	1				54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	37.5 μs	18.75 μs	9.375 μs	4.6875 μs	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	31.25 μs	15.625 μs	7.8125 μs	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	f$_{CLK}$/4
1	1	1				50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	**31.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	**26.25 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/4
1	1	1				**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	f$_{CLK}$/64
0	0	1				Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	f$_{CLK}$/32
0	1	0				Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	f$_{CLK}$/16
0	1	1				Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	f$_{CLK}$/8
1	0	0				Setting prohibited	Setting prohibited	**28.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/6
1	0	1				Setting prohibited	Setting prohibited	**23.75 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/5
1	1	0				Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/4
1	1	1				**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f$_{CLK}$/2

Correct:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) 1.8 V $\leq$ V_{DD} < 2.7 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz[Note]	f_{CLK} = 32 MHz	
x	x	x	0	0	Normal 1	Setting prohibited						–
x	x	x	0	1	Normal 2	Setting prohibited						–
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	42 µs	f_{CLK}/64
0	0	1								42 µs	21 µs	f_{CLK}/32
0	1	0							42 µs	21 µs	Setting prohibited	f_{CLK}/16
0	1	1						42 µs	21 µs			f_{CLK}/8
1	0	0						31.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1						26.25 µs				f_{CLK}/5
1	1	0					42 µs	21 µs				f_{CLK}/4
1	1	1				42 µs	21 µs	Setting prohibited				f_{CLK}/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 µs	f_{CLK}/64
0	0	1								38 µs	19 µs	f_{CLK}/32
0	1	0							38 µs	19 µs	Setting prohibited	f_{CLK}/16
0	1	1						38 µs	19 µs			f_{CLK}/8
1	0	0						28.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1						28.75 µs				f_{CLK}/5
1	1	0					38 µs	19 µs				f_{CLK}/4
1	1	1				38 µs	19 µs	Setting prohibited				f_{CLK}/2

Note (Omitted)

Correct:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) 1.6 V ≤ VDD < 1.8 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz Note 2	f_{CLK} = 32 MHz	
x	x	x	0	0	Normal 1	Setting prohibited	–	x	x	x	0	0
x	x	x	0	1	Normal 2	Setting prohibited	–	x	x	x	0	1
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	84 μs	Setting prohibited	f_{CLK}/64
0	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	84 μs	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	84 μs	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	1	0	Low-Voltage 1	Setting prohibited	84 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	0	Low-Voltage 1	Setting prohibited	63 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	0	Low-Voltage 1	105 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	0	Low-Voltage 1	84 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	Setting prohibited	f_{CLK}/64
0	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	76 μs	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	1	1	Low-Voltage 2	Setting prohibited	76 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	1	Low-Voltage 2	Setting prohibited	76 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	1	Low-Voltage 2	95 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	1	Low-Voltage 2	76 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2

Note (Omitted)

6. Note when entering A/D converter standby mode added

Note on A/D converter mode register 2 (ADM2) added (page 493)

Incorrect:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Caution   Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

Correct:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Cautions 1. Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

   2. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADREFP1 to 1. When selecting internal reference voltage (ADREFP1, ADREFP0 = 1, 0), the current value of A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

Note on analog input channel specification register (ADS) added (page 497)

Incorrect:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H   After reset: 00H   R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.

7. If using AVREFM as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.

8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.

Correct:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H   After reset: 00H   R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.

7. If using AVREFM as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.

8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.

9. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADISS to 1. When setting ADISS to 1, the current value of the A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

RENESAS

7. Incorrect descriptions of maskable interrupt request acknowledgement operation revised

Revised incorrect description of time from generation of maskable interrupt until servicing in Table 16-4. (page 842)

Incorrect:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
Servicing time	9 clocks	**14 clocks**

Note If an interrupt request is generated just before the RET instruction, the wait time becomes longer.

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Correct:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
Servicing time	9 clocks	16 clocks

Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

RENESAS

Figure 16-9. Incorrect description of interrupt request acknowledgment timing (maximum time) revised (page 844)
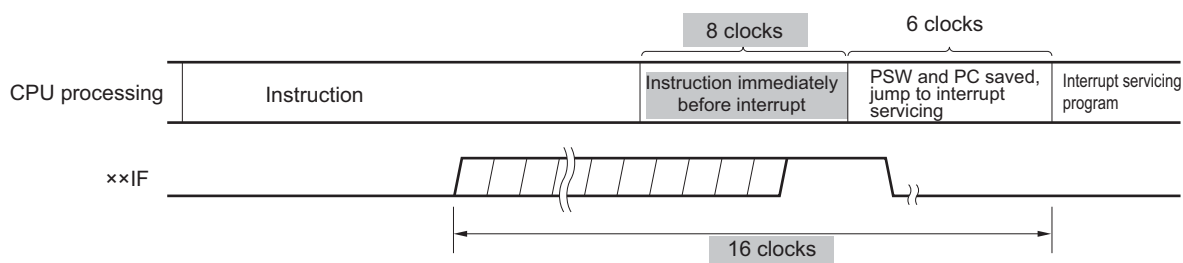
Incorrect:

Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)
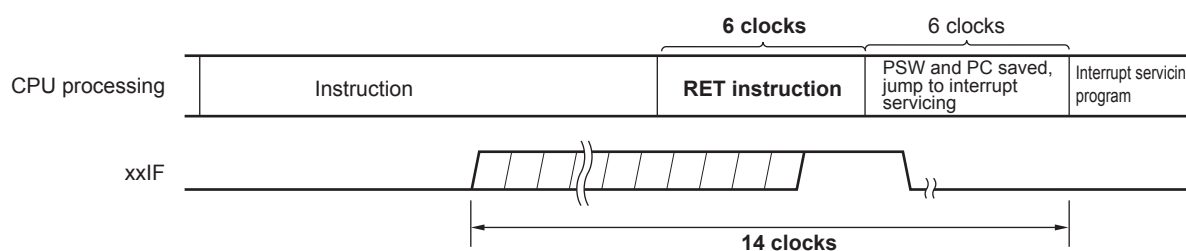
Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Correct:

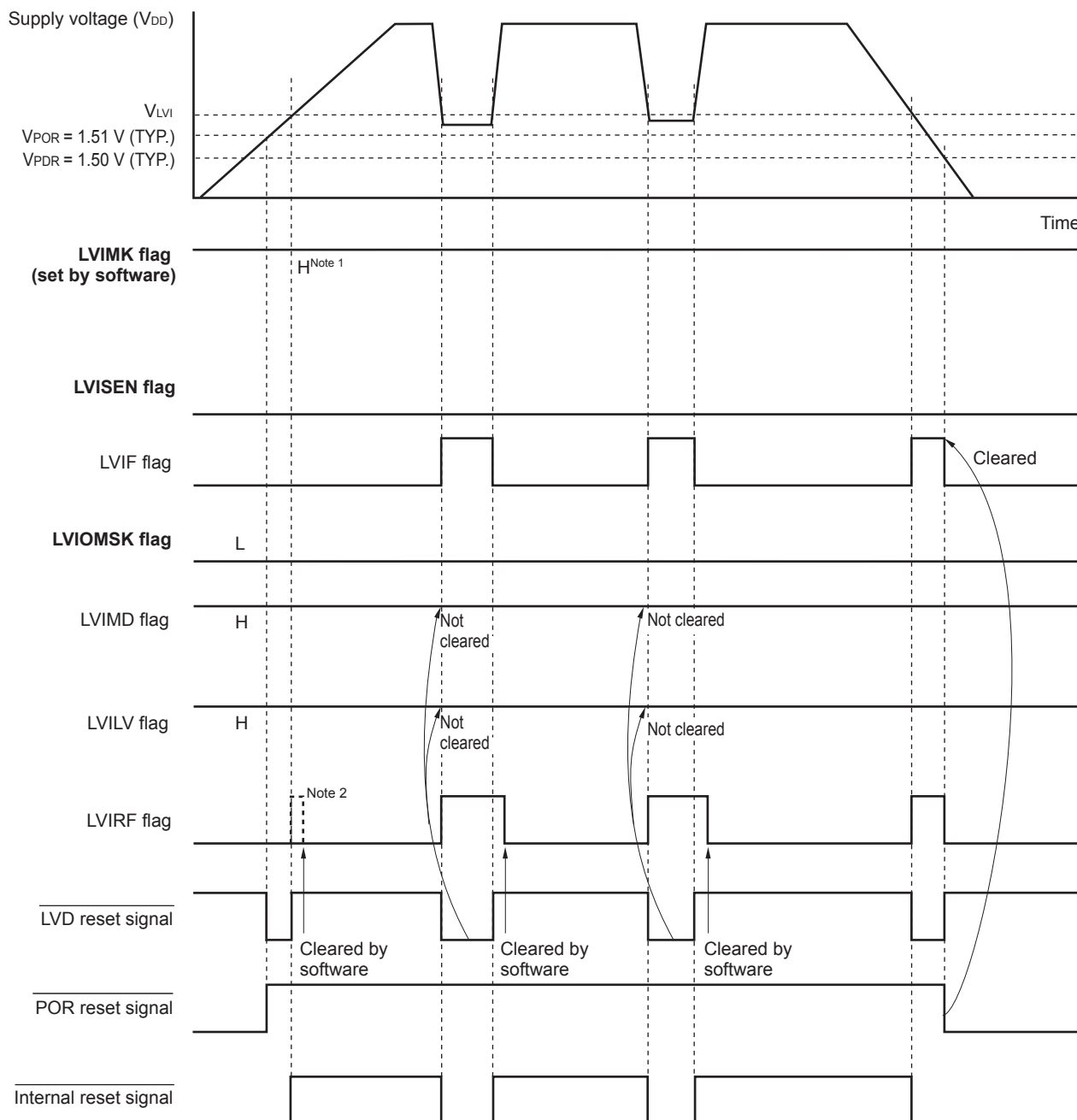Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

8. Incorrect descriptions of voltage detector (LVD) timing chart revised

Figure 21-4. Incorrect descriptions of timing of voltage detector internal reset signal generation revised (page 894)

Incorrect:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)

Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF).

The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

RENESAS

Correct:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)
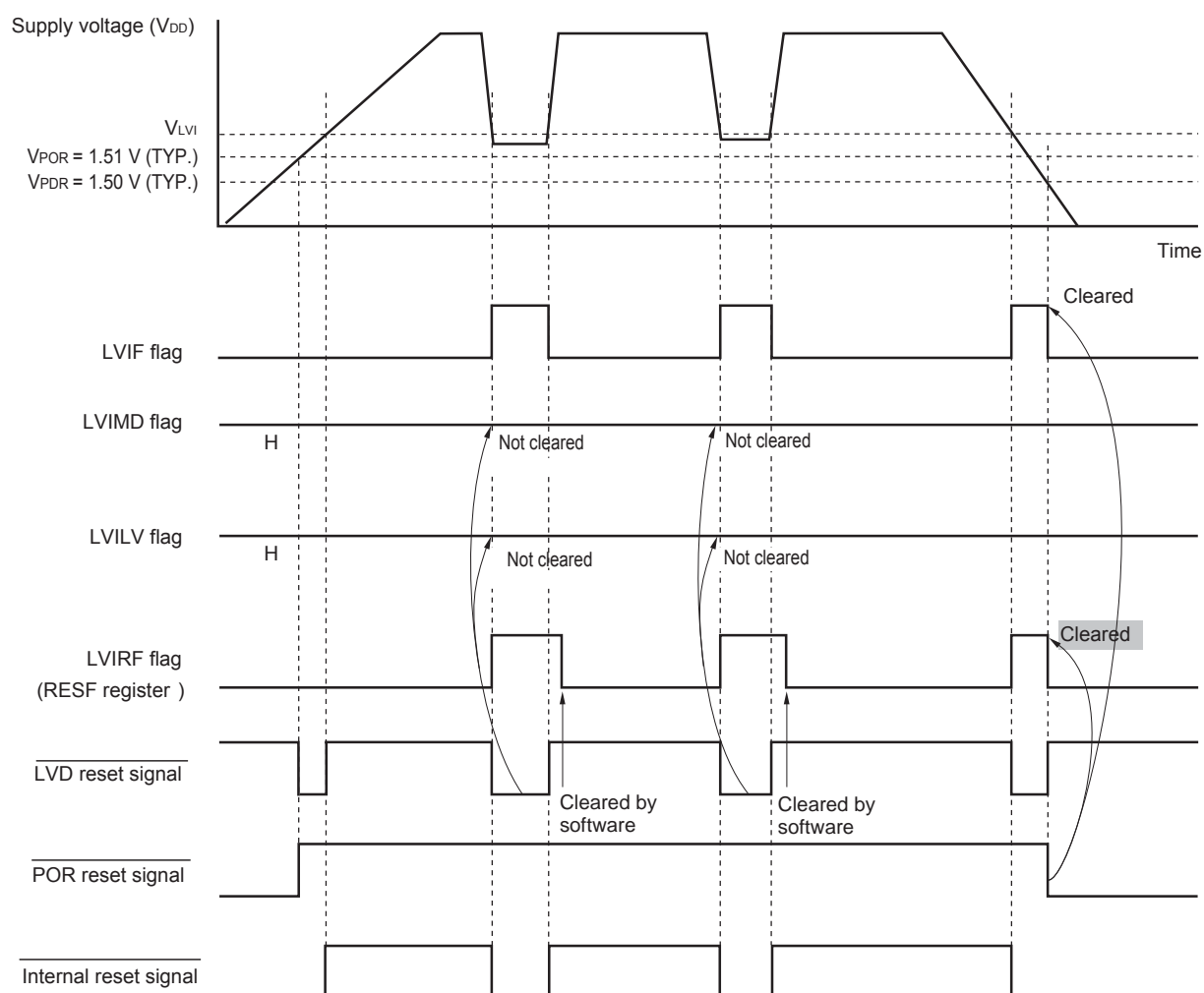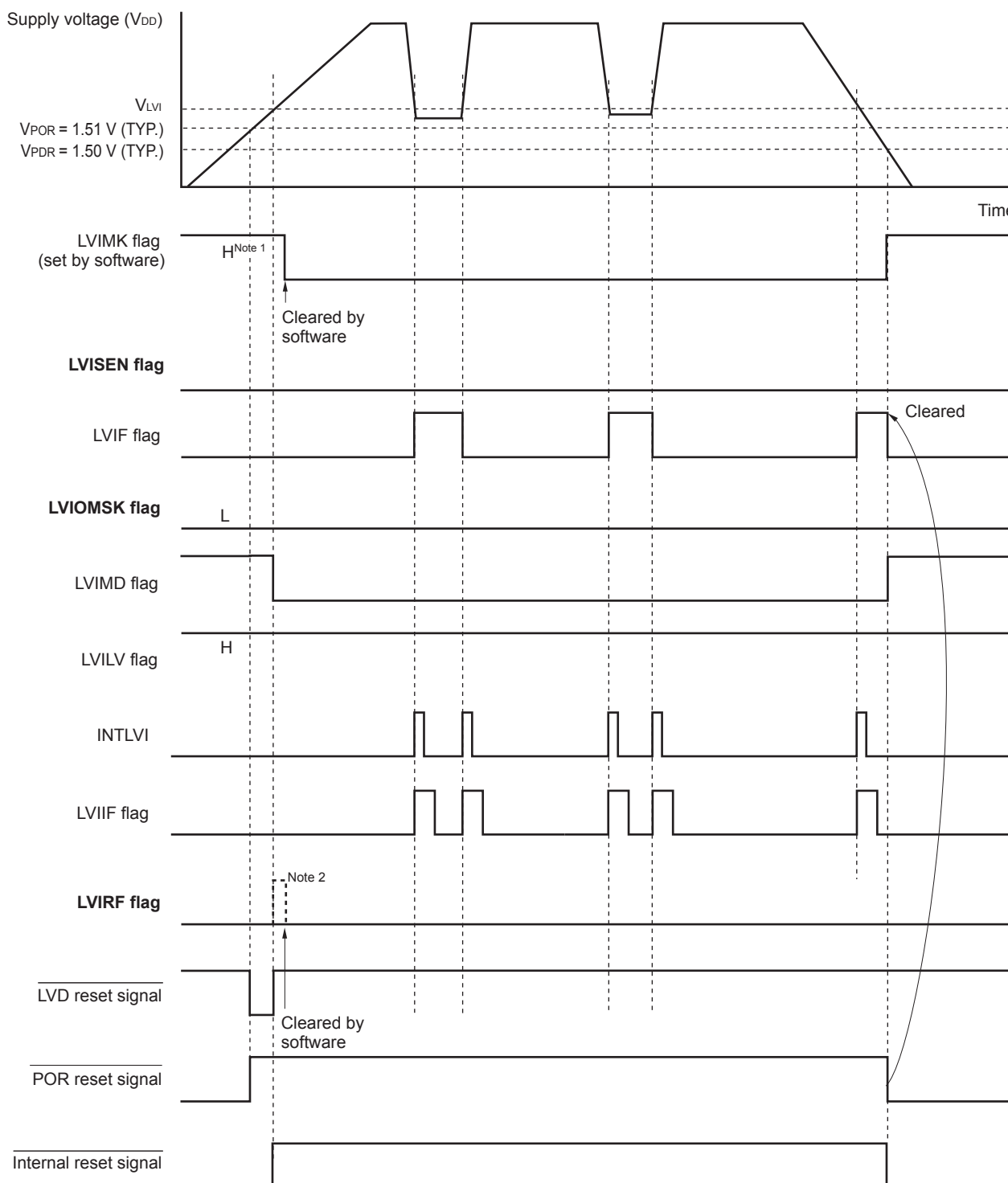
Figure 21-5. Incorrect description of voltage detector internal interrupt signal generation timing revised (page 896)

Incorrect:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 0, 1)

Notes 1. The LVIMK flag is set to "1" by reset signal generation.
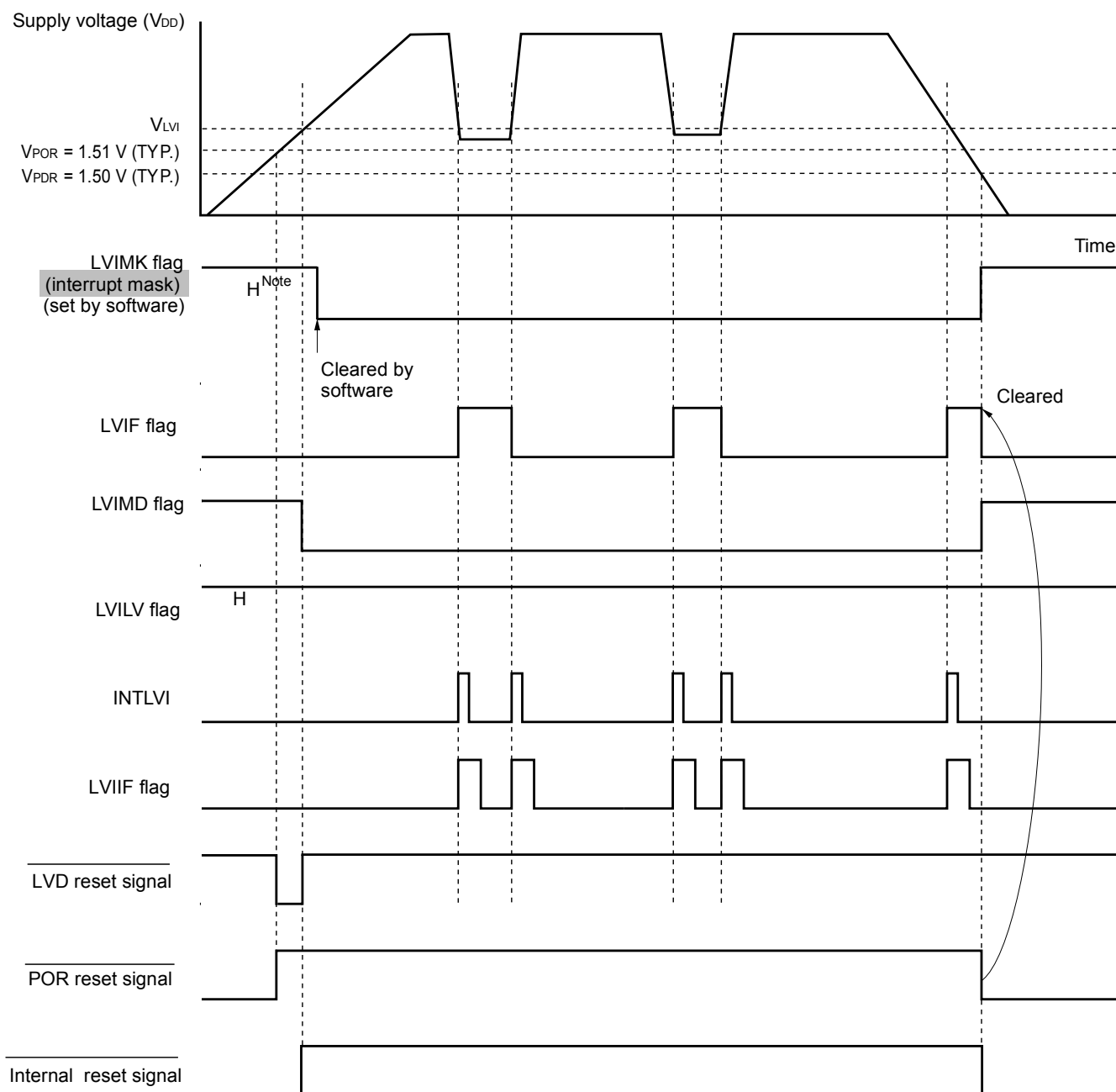
2. LVIRF flag is bit 0 of the reset control flag register (RESF).

The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

RENESAS

Correct:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 0, 1)

Note   The LVIMK flag is set to "1" by reset signal generation.

9.   Incorrect description of voltage detector (LVD) interrupt and reset mode revised

Incorrect description of when used as interrupt and reset mode revised (page 897)

Incorrect:

21.4.3 When used as interrupt and reset mode

- When starting operation

    Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage

    (V_{LVIH}, V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

Figure 21-6 shows the timing of the internal reset signal and interrupt signal generated by the voltage detector.

Caution   The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

21.4.3 When used as interrupt and reset mode

- When starting operation

    Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage

    (V_{LVIH}, V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

Figures 21-6 shows the Timing of Voltage Detector Reset Signal and Interrupt Signal Generation.

Perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated and figure 21-8

Initial Setting of Interrupt and Reset Mode.

Incorrect description of timing of voltage detector reset signal and interrupt signal generation revised (page 898)

Incorrect:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0)

RENESAS
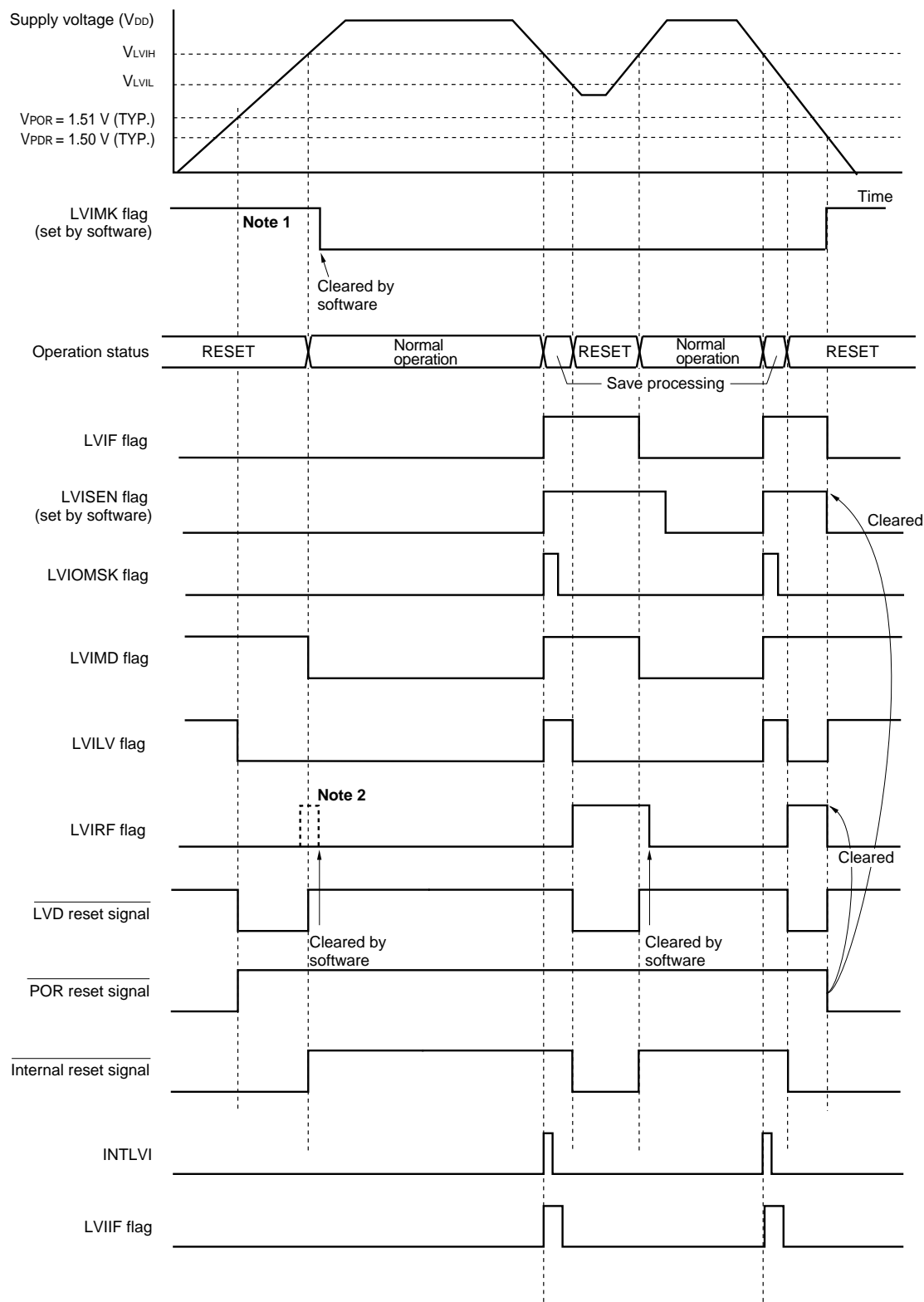
Notes 1. The LVIMK flag is set to "1" by reset signal generation.

   2. ~~LVIRF flag is bit 0 of the reset control flag register (RESF). The LVIRF flag may become 1 from the beginning due to the power-on waveform. For details of the RESF register, see CHAPTER 19 RESET FUNCTION.~~

Remark V_{POR}: POR power supply rise detection voltage

   V_{PDR}: POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)

If a reset is not generated after releasing the mask, determine that a condition of V_{DD} becomes $V_{DD} \geq V_{LVIH}$, clear LVIMD, and the MCU returns to normal operation.

Supply voltage (V_{DD})

V_{LVIH}

V_{LVIL}

V_{POR} = 1.51 V (TYP.)
V_{PDR} = 1.50 V (TYP.)

Time

LVIMK flag
(set by software)

H [Note 1]

Cleared by software

Cleared by software

Wait for stabilization by software
(400 μs or 5 clocks of f_{IL}) [Note 3]

Normal operation

Operation status   RESET   Normal operation   Save processing   RESET   Normal operation   RESET

Save processing

LVIF flag   Cleared

LVISEN flag
(set by software)

LVIOMSK flag

LVIMD flag

LVILV flag   Cleared by software [Note 3]

Cleared by software [Note 2]

LVIRF flag   Cleared

LVD reset signal

POR reset signal

Internal reset signal

INTLVI

LVIIF flag

RENESAS

Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.
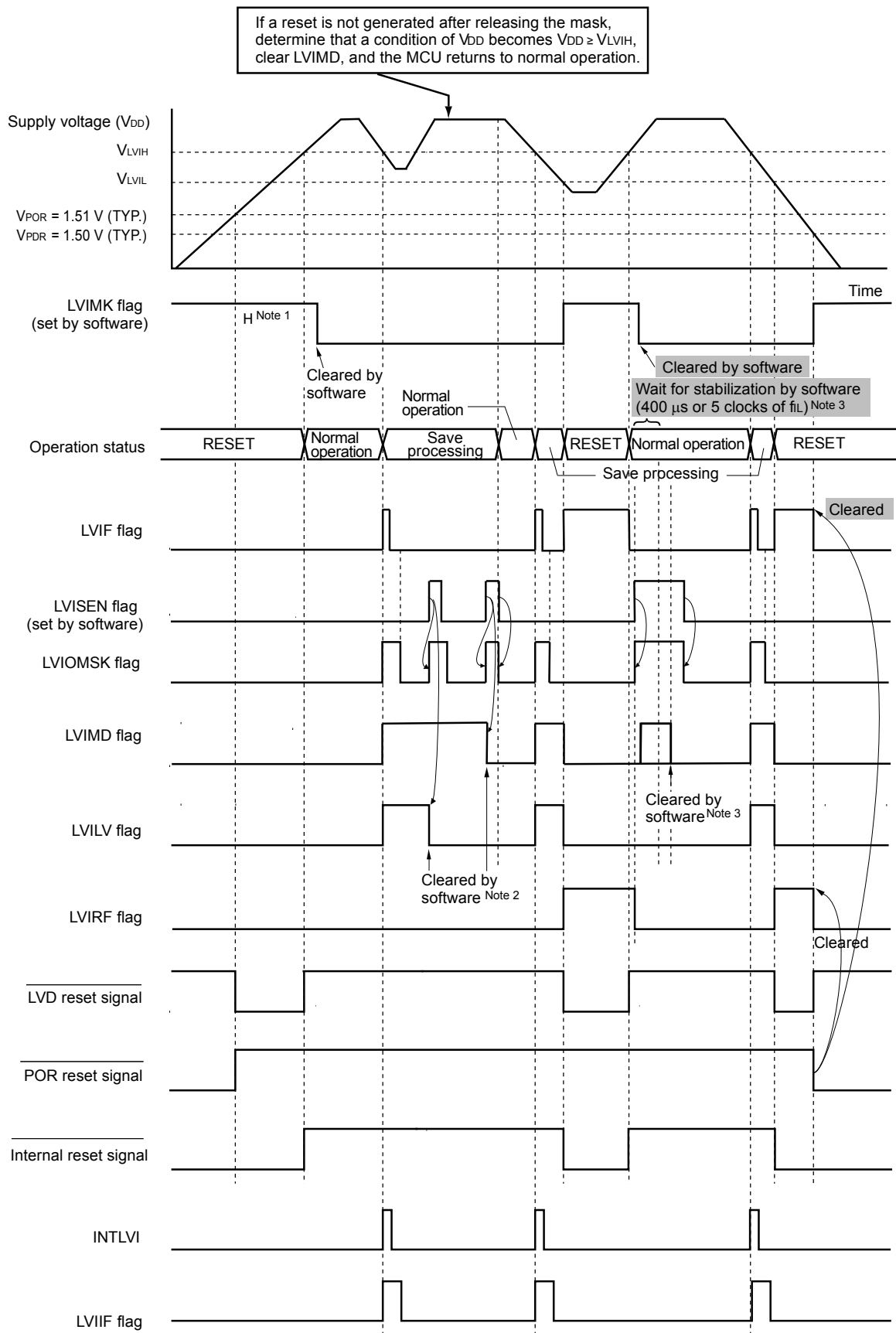
Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation
(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)

Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

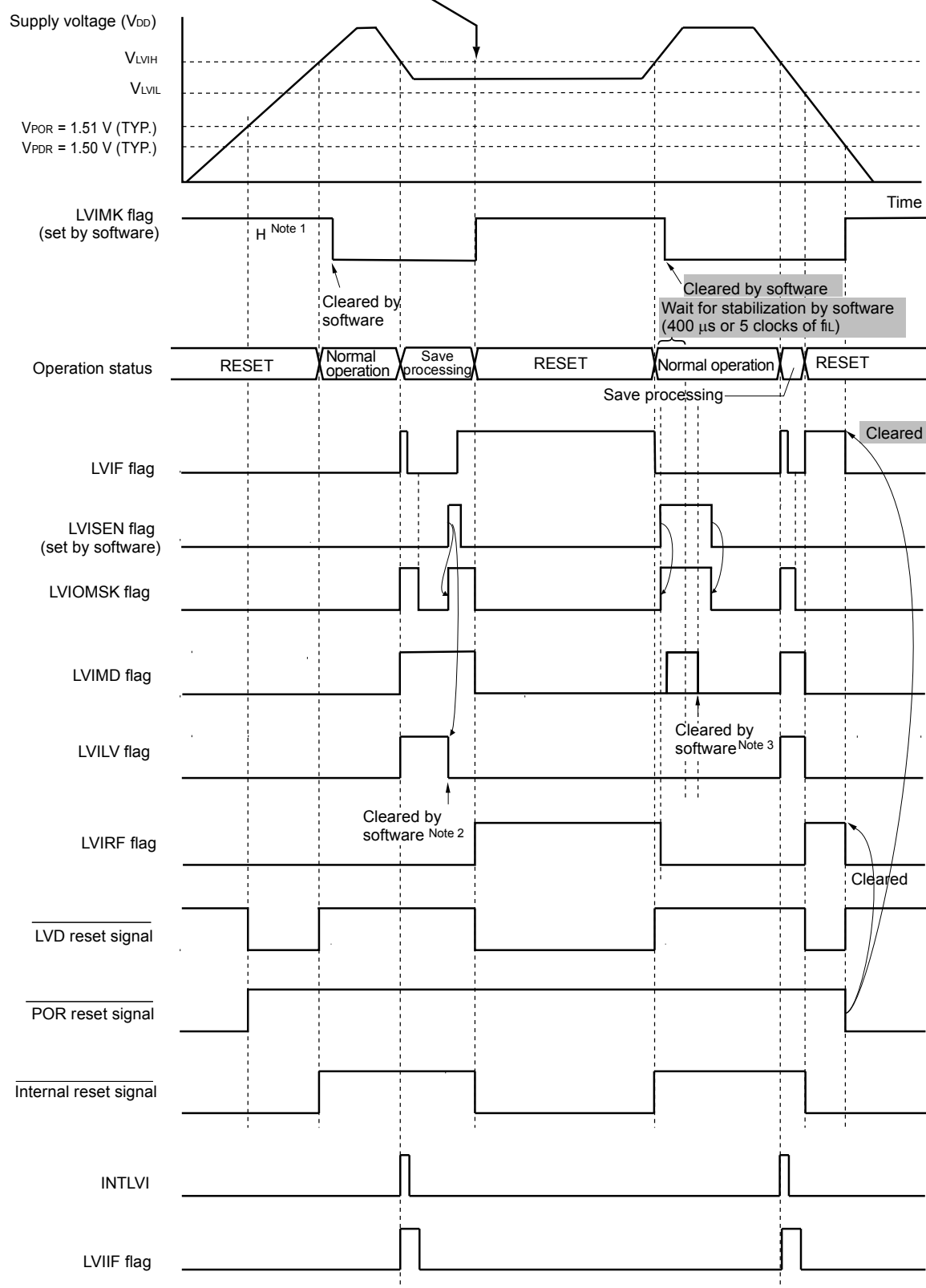Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

Figure 21-7. Processing Procedure After an Interrupt Is Generated

INTLVI generated

Save processing — Perform required save processing.

LVISEN = 1 — Set the LVISEN bit to 1 to mask voltage detection (LVIOMSK = 1).

LVILV = 0 — Set the LVILV bit to 0 to set the high-voltage detection level (VLVIH).

LVISEN = 0 — Set the LVISEN bit to 0 to enable voltage detection.

LVIOMSK = 0

No

Yes

LVD reset generated — The MCU returns to normal operation when internal reset by voltage detector (LVD) is not generated, since a condition of V_{DD} becomes $V_{DD} \geq V_{LVIH}$.

Yes

No

LVISEN = 1 — Set the LVISEN bit to 1 to mask voltage detection (LVIOMSK = 1)

LVIMD = 0 — Set the LVIMD bit to 0 to set interrupt mode.

LVISEN = 0 — Set the LVISEN bit to 0 to enable voltage detection.
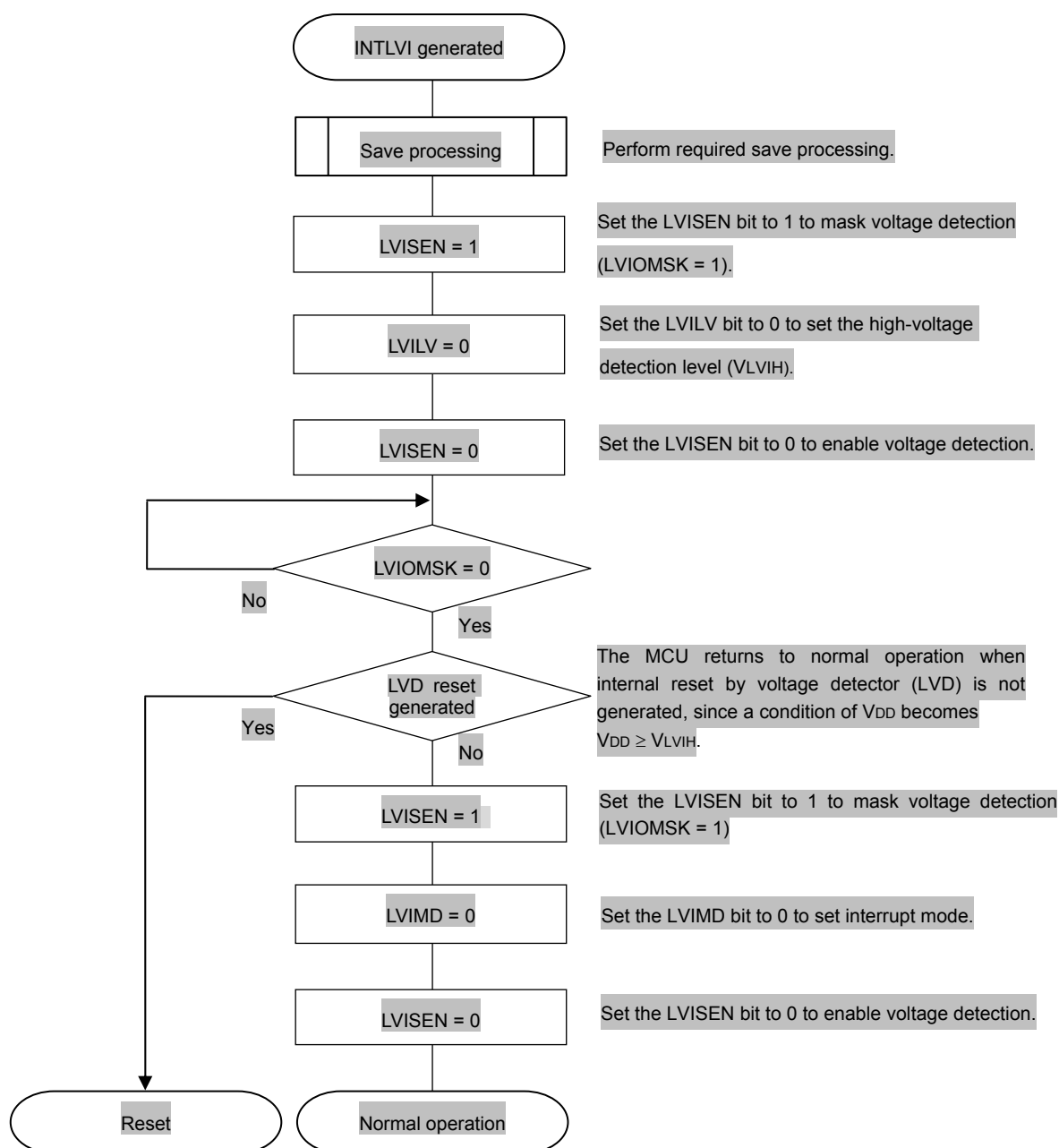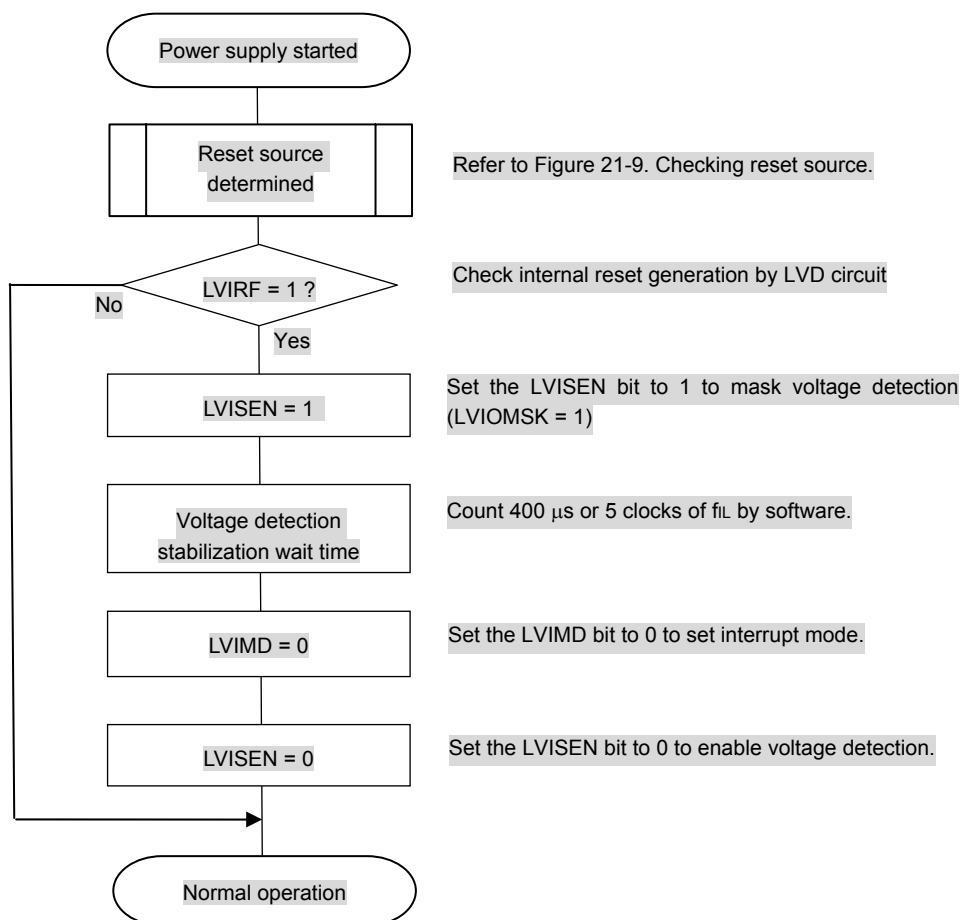
Reset

Normal operation

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Figure 21-8. Explanations of initial setting of interrupt and reset mode added (page 899)

When setting an interrupt and reset mode (LVIMDS1, LVIMDS0 = 1, 0), voltage detection stabilization wait time for 400 μs or 5 clocks of f_{IL} is necessary after LVD reset is released (LVIRF = 1). After waiting until voltage detection stabilizes, (0) clear the LVIMD bit for initialization. While voltage detection stabilization wait time is being counted and when the LVIMD bit is rewritten, set LVISEN to 1 to mask a reset or interrupt generation by LVD.

Figure 21-8. shows the procedure for initial setting of interrupt and reset mode.

Figure 21-8. Initial Setting of Interrupt and Reset Mode

```
           ┌─────────────────────┐
           │ Power supply started │
           └─────────────────────┘
                      │
           ┌─┬─────────────────┬─┐
           │ │  Reset source   │ │      Refer to Figure 21-9. Checking reset source.
           │ │   determined    │ │
           └─┴─────────────────┴─┘
                      │
                     ╱╲
       No          ╱    ╲              Check internal reset generation by LVD circuit
      ┌──────────<  LVIRF = 1 ? >
      │            ╲    ╱
      │              ╲╱
      │              │ Yes
      │     ┌─────────────────┐
      │     │   LVISEN = 1    │         Set the LVISEN bit to 1 to mask voltage detection
      │     └─────────────────┘         (LVIOMSK = 1)
      │              │
      │     ┌─────────────────┐
      │     │ Voltage detection │       Count 400 μs or 5 clocks of f_IL by software.
      │     │ stabilization wait time │
      │     └─────────────────┘
      │              │
      │     ┌─────────────────┐
      │     │   LVIMD = 0     │         Set the LVIMD bit to 0 to set interrupt mode.
      │     └─────────────────┘
      │              │
      │     ┌─────────────────┐
      │     │   LVISEN = 0    │         Set the LVISEN bit to 0 to enable voltage detection.
      │     └─────────────────┘
      │              │
      └──────────────┤
                     │
           ┌─────────────────────┐
           │  Normal operation   │
           └─────────────────────┘
```

Remark f_{IL}: Low-speed on-chip oscillator clock frequency

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10. Added common item for all RL78/G13 products in 29.4.2 Supply current characteristics of Electrical specifications (page 1005)

Incorrect:

(4) Common to RL78/G13 all products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	I_{WDT} Notes 2,3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
Temperature sensor operating current	I_{TMPS}				75		μA
LVD operating current	I_{LVI} Notes 5				0.08		μA
BGO operating current	I_{BGO} Notes 6				2.50	12.20	mA

Note (Omitted)

Correct:

(4) Common to RL78/G13 all products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	I_{WDT} Notes 2,3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}				75		μA
Temperature sensor operating current	I_{TMPS}				75		μA
LVD operating current	I_{LVI} Notes 5				0.08		μA
BGO operating current	I_{BGO} Notes 6				2.50	12.20	mA

Note (Omitted)

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Issued Document History

RL78/G13 Incorrect description notice, issued document history

Document Number	Issue Date	Description
TN-RL*-A001A/E	Dec. 5, 2011	First edition issued Incorrect descriptions of No.1 to No.10 revised