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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A027B/E	Rev.	2.00
Title	Correction for Incorrect Description Notice RL78/G12 Descriptions in the Hardware User's Manual Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G12 R5F102xxx, R5F103xxx	Lot No. All lots	Reference Document	RL78/G12 User's Manual: Hardware Rev.2.00 R01UH0200EJ0200 (Aug. 2013)		

This document describes misstatements found in the RL78/G12 User's Manual: Hardware Rev.2.00 (R01UH0200EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: T_A = −40 to +85°C)	Page 732	Content change
CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: T_A = −40 to +105°C)	Page 778	Content change

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

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Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0200EJ0200
1	1.4 Pin Configuration (Top View) 1.4.2 24-pin products 1.4.3 30-pin products			Pages 9 and 10	Pages 3 and 4
2	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)			Page 128	Page 5
3	11.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 11-71. and Figure 11-73.)			Pages 404 and 406	Pages 6 and 7
4	11.6.3 SNOOZE mode function			Page 429	Page 8
5	11.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 11-90., Figure 11-91. and Figure 11-93.)			Pages 431, 432 and 434	Pages 9 to 11
6	19.2 Configuration of Power-on-reset Circuit Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1)			Page 639	Page 12
7	28.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics			Page 776	Page 13
8	29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics			Page 818	Page 14
9	CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: TA = −40 to +85°C)			Page 732	Page 15
10	CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: TA = −40 to +105°C)			Page 778	Page 16

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G12 User's Manual: Hardware Rev.2.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A027A/E	May. 12, 2014	First edition issued No.1 to 8 in corrections
TN-RL*-A027B/E	Nov. 26, 2014	Second edition issued No.9 to 10 in corrections (This notice)

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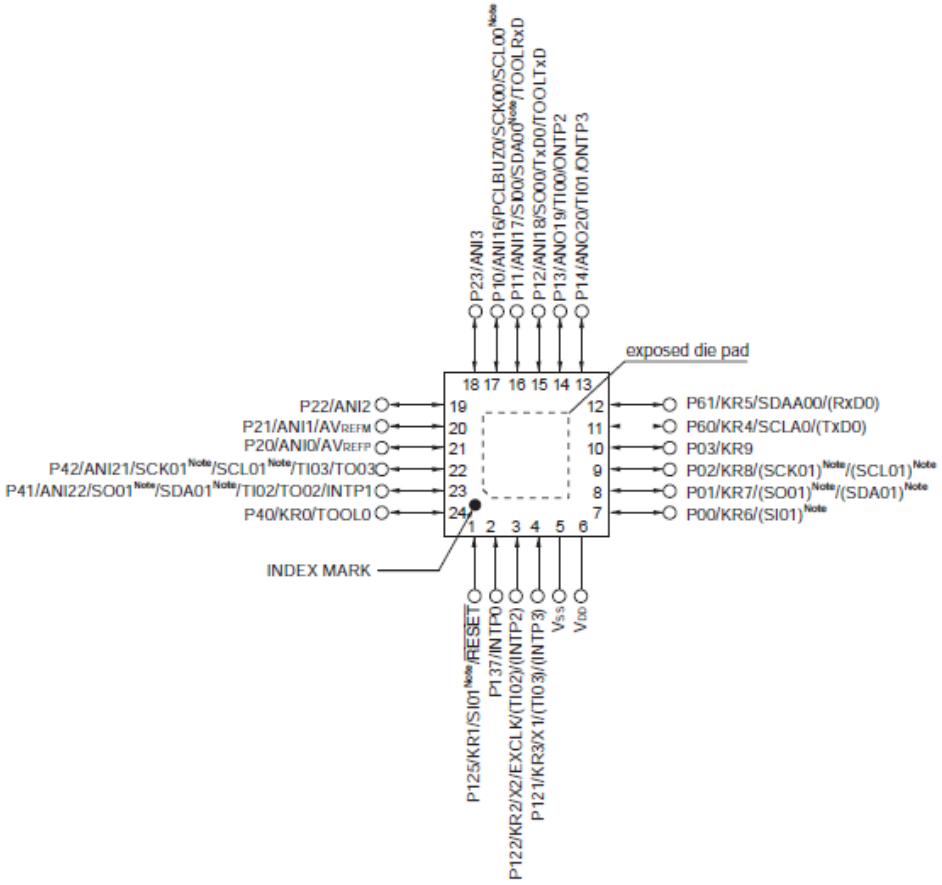
1. **1.4 Pin Configuration (Top View)**
   1.4.2 24-pin products, and 1.4.3 30-pin products (Pages 9 and 10)

Incorrect:

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

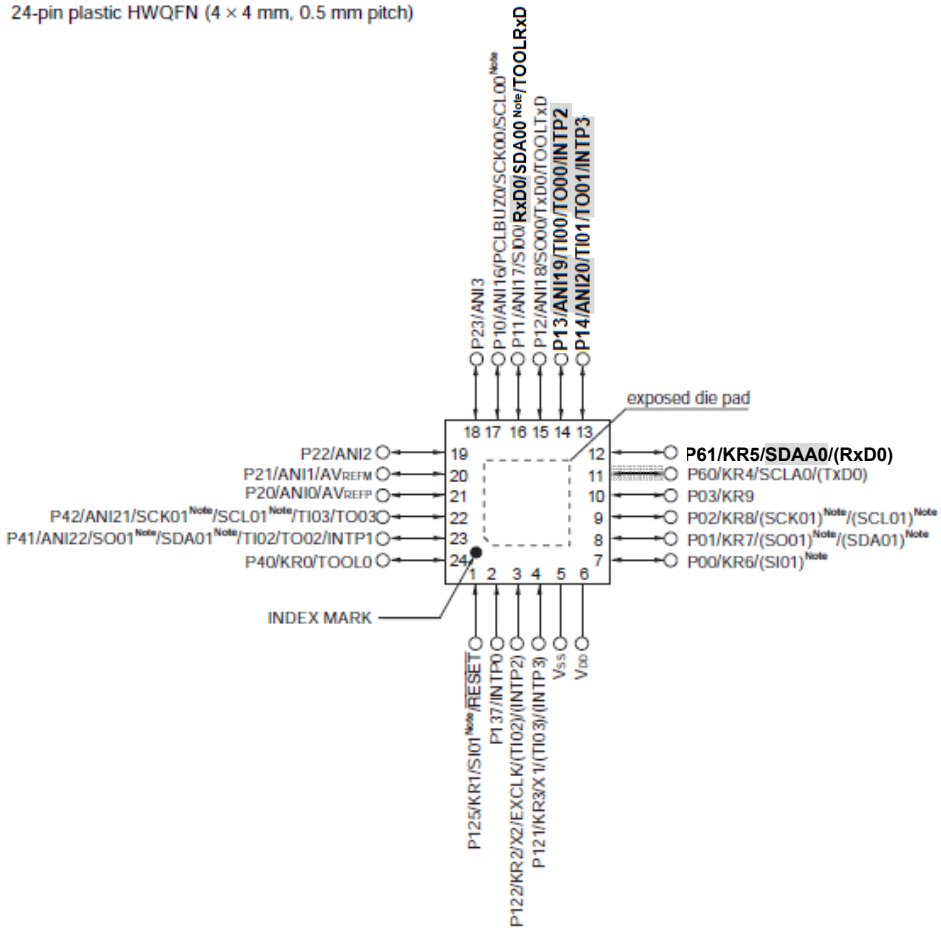


Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.
3. It is recommended to connect an exposed die pad to Vss.

Correct:

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.
3. It is recommended to connect an exposed die pad to Vss.

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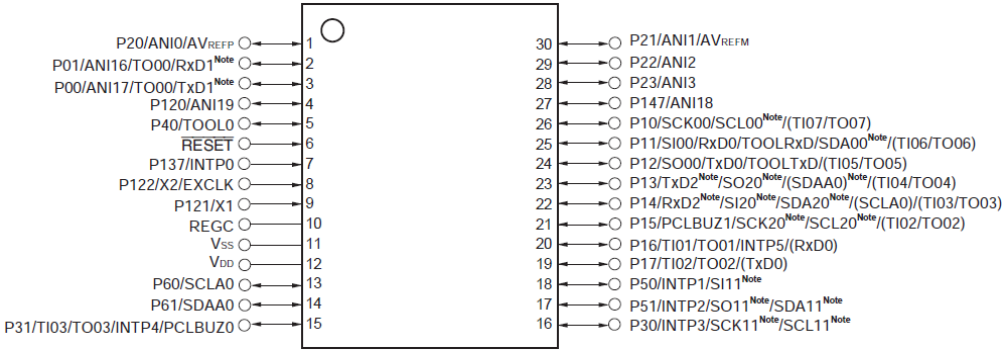
Incorrect:

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Provided only in the R5F102 products.

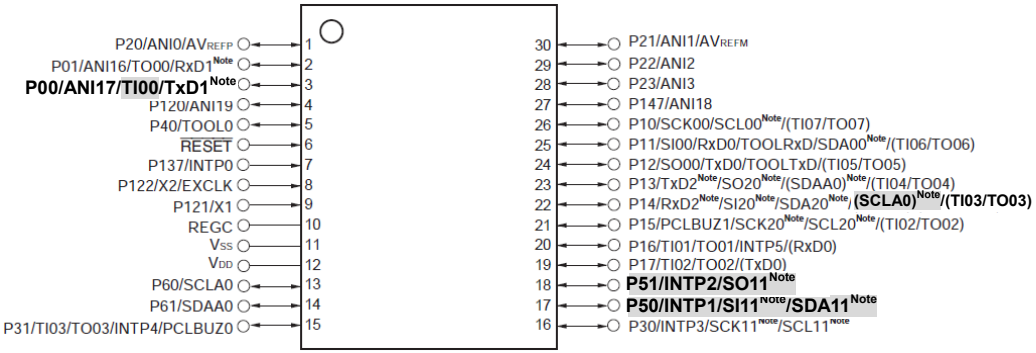
Caution Connect the REGC pin to Vss via capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).**

Correct:

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Provided only in the R5F102 products.

Caution Connect the REGC pin to Vss via capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).**

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2. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM) (Page 128)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	▲
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	▼
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	▲
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	▼
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

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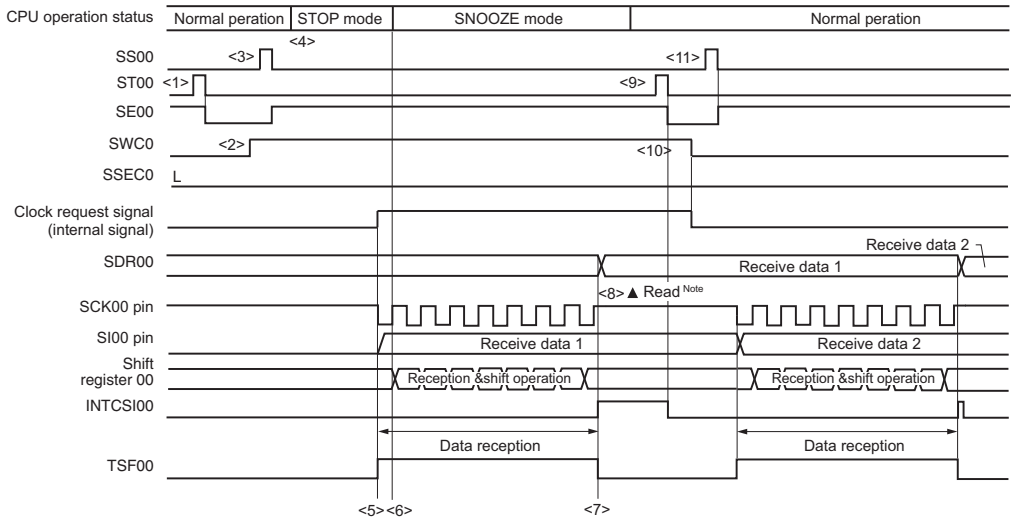
3. 11.5.7 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 11-71. and Figure 11-73.) (Pages 404 and 406)

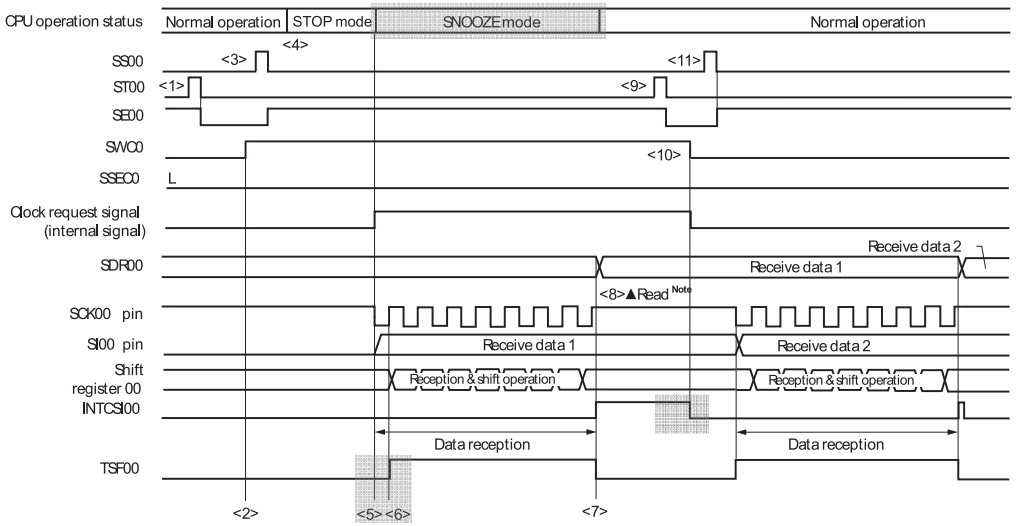
It is correction of “CPU operation status”, “INTCSI00” and “TSF00” in this Figure.

Incorrect:
Figure 11-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAP00 = 0, CKP00 = 0)



(omitted)

Correct:
Figure 11-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAP00 = 0, CKP00 = 0)



(omitted)

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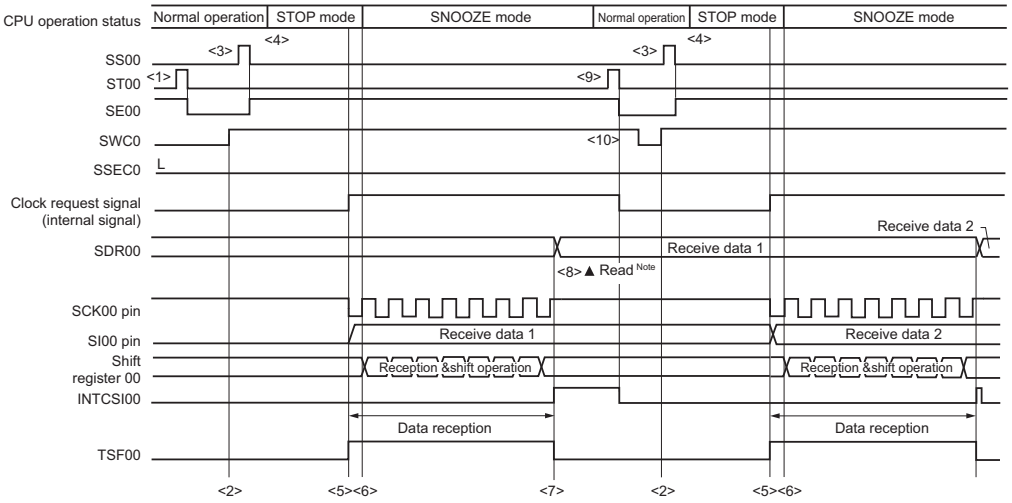
It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTCSI00” and “TSF00” in this Figure.

Incorrect:

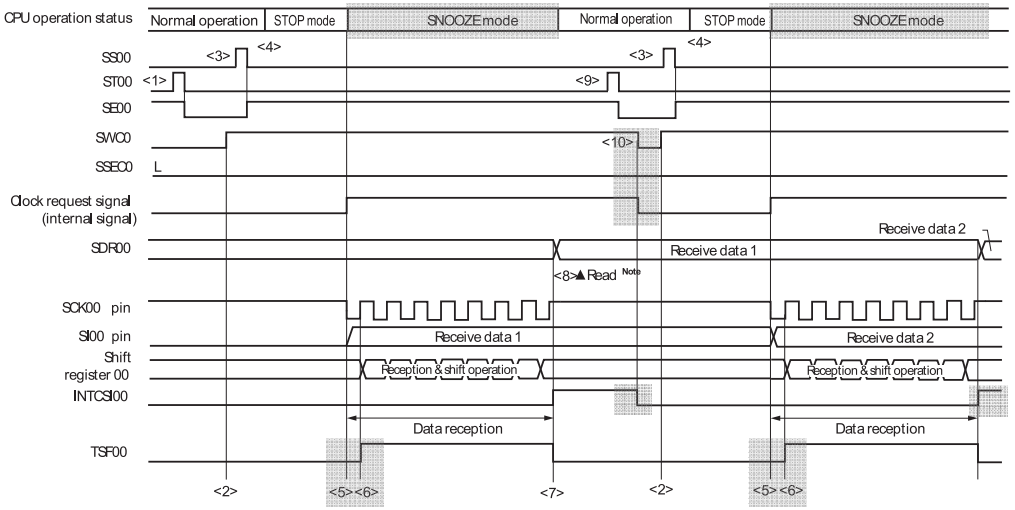
Figure 11-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAP00 = 0, CKP00 = 0)



(omitted)

Correct:

Figure 11-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAP00 = 0, CKP00 = 0)



(omitted)

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4. 11.6.3 SNOOZE mode function (Page 429)

Incorrect:

11.6.3 SNOOZE mode function

SNOOZE mode makes UART operate reception by RxD0 pin input detection while the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation. Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSEC0 bit is set to 1, the PEF01, FEF01, or OVF01 flag is not set and an error interrupt (INTSRE0) is not generated. Therefore, when the setting of SSEC0 = 1 is made, clear the PEF01, FEF01, or OVF01 flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxD0 register) of the SDR01 register.

Correct:

11.6.3 SNOOZE mode function

SNOOZE mode makes UART operate reception by RxD0 pin input detection while the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation. Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSEC0 bit is set to 1, the PEF01, FEF01, or OVF01 flag is not set and an error interrupt (INTSRE0) is not generated. Therefore, when the setting of SSEC0 = 1 is made, clear the PEF01, FEF01, or OVF01 flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxD0 register) of the SDR01 register.

5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxD0 signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxD0 pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

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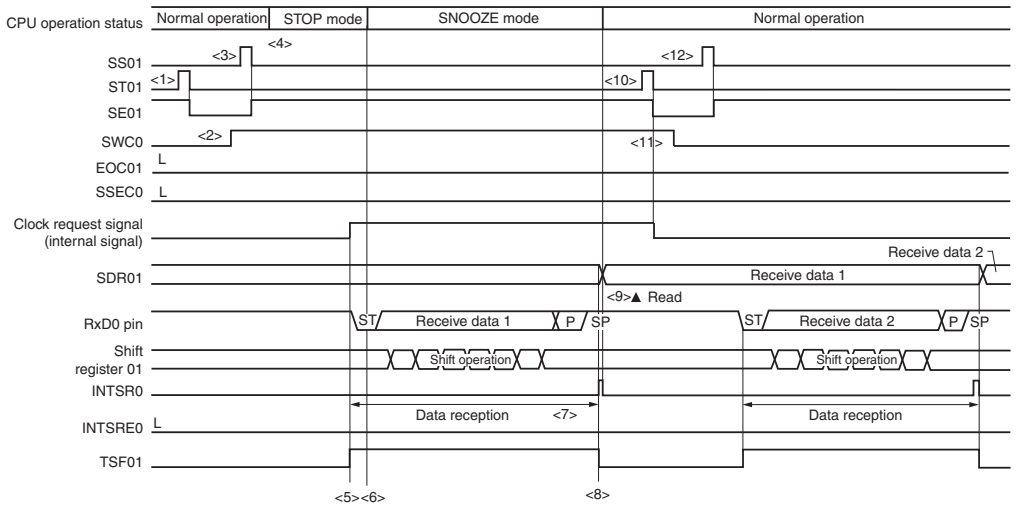
5. 11.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 11-90., Figure 11-91. and Figure 11-93.) (Pages 431, 432 and 434)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

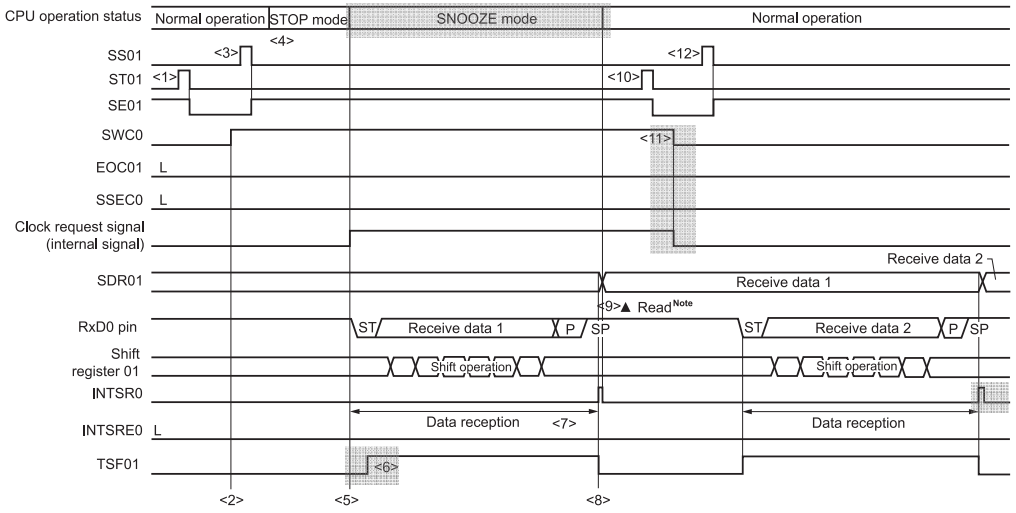
Figure 11-90. Timing Chart of SNOOZE Mode Operation (EOC01 = 0, SSEC0 = 0/1)



(omitted)

Correct:

Figure 11-90. Timing Chart of SNOOZE Mode Operation (EOC01 = 0, SSEC0 = 0/1)



(omitted)

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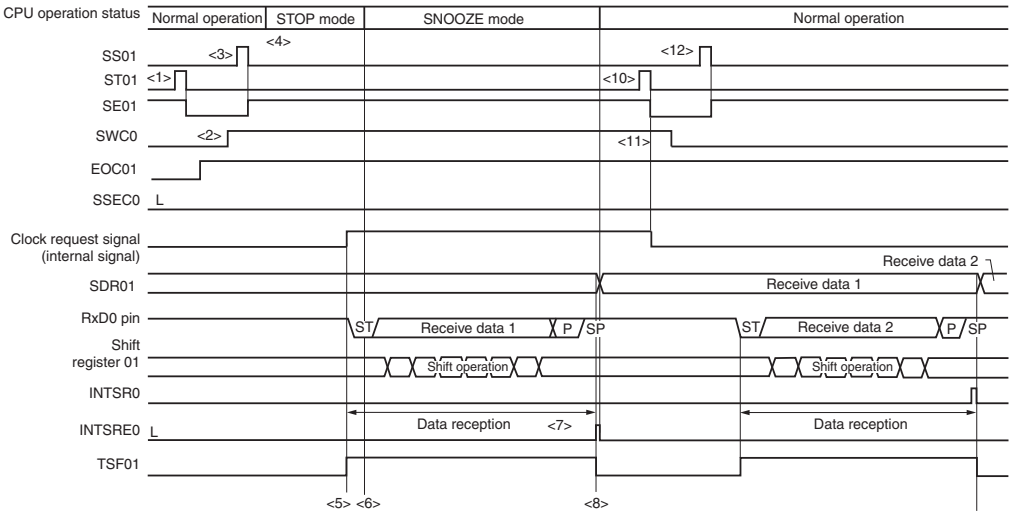
It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

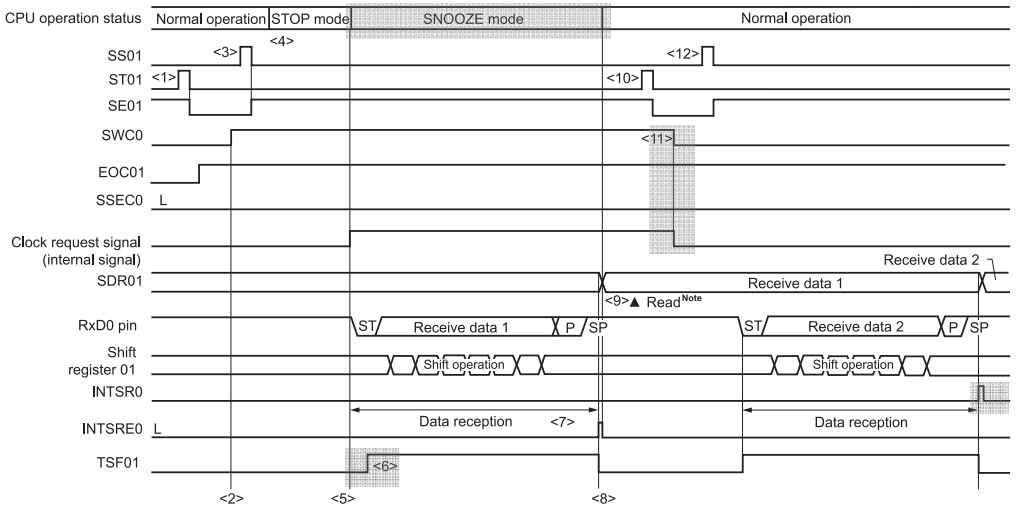
Figure 11-91. Timing Chart of SNOOZE Mode Operation (EOC01 = 1, SSEC0 = 0)



(omitted)

Correct:

Figure 11-91. Timing Chart of SNOOZE Mode Operation (EOC01 = 1, SSEC0 = 0)



(omitted)

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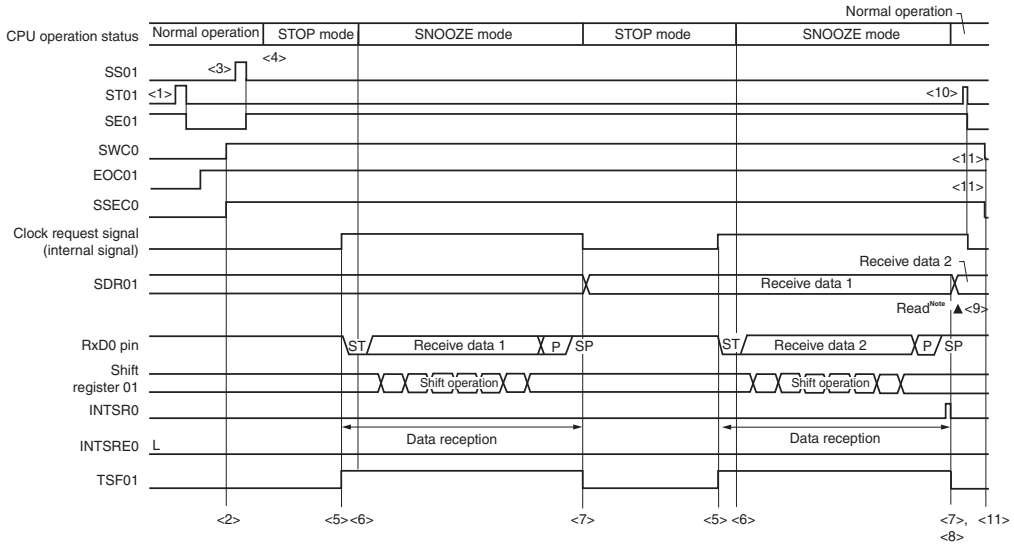
It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

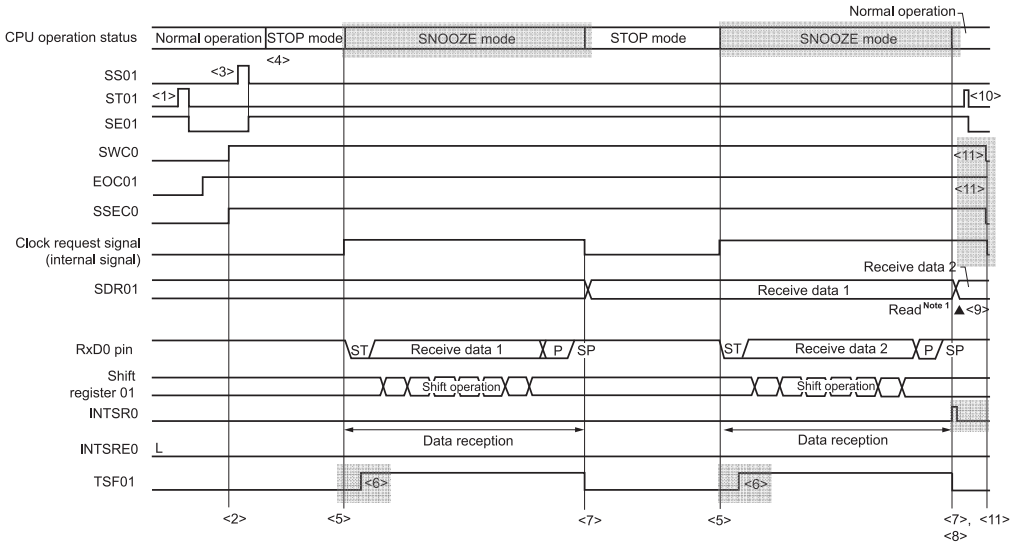
Figure 11-93. Timing Chart of SNOOZE Mode Operation (EOC01 = 1, SSEC0 = 1: Error interrupt (INTSRE0) generation is stopped)



(omitted)

Correct:

Figure 11-93. Timing Chart of SNOOZE Mode Operation (EOC01 = 1, SSEC0 = 1: Error interrupt (INTSRE0) generation is stopped)



(omitted)

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6. 19.2 Configuration of Power-on-reset Circuit
Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1) (Page 639)

Incorrect:

Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the external reset input via $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
After the first release of POR:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset processing time when the external reset is released after the second release of POR is shown below.
After the second release of POR:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)
(omitted)

Correct:

Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the external reset input via $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
Release from the first external reset following release from the POR state:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset times in cases of release from an external reset other than the above are listed below.
Release from the reset state for external resets other than the above case:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)
(omitted)

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7. 28.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 776)

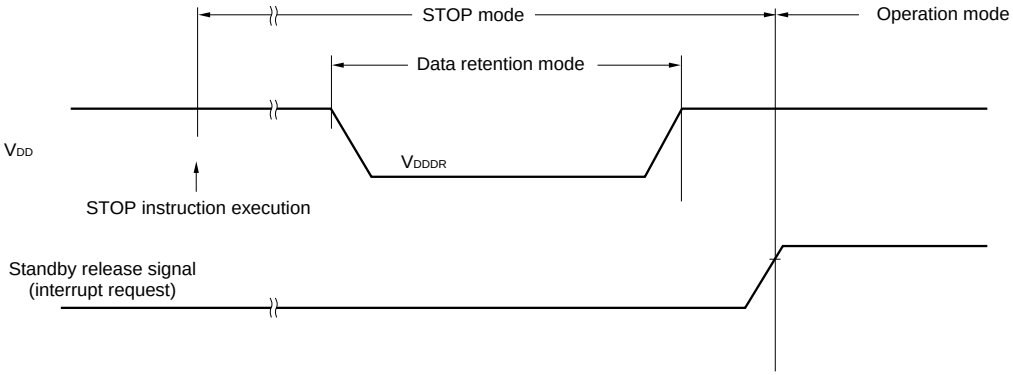
Old:

28.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is affected.



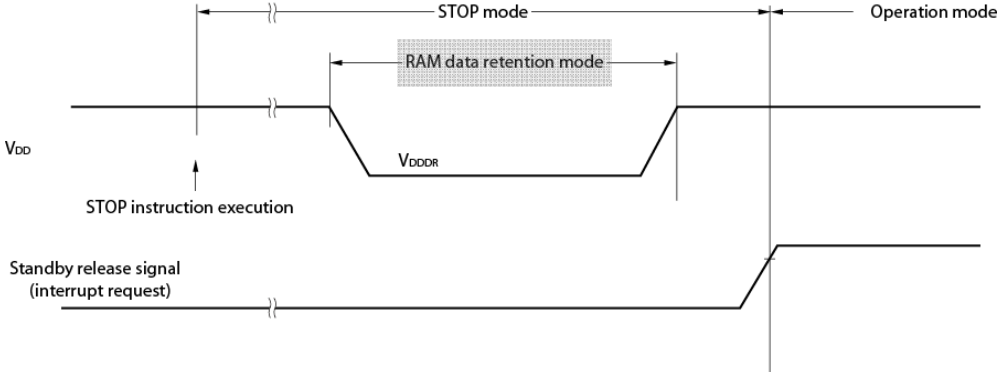
New:

28.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



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8. 29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 818)

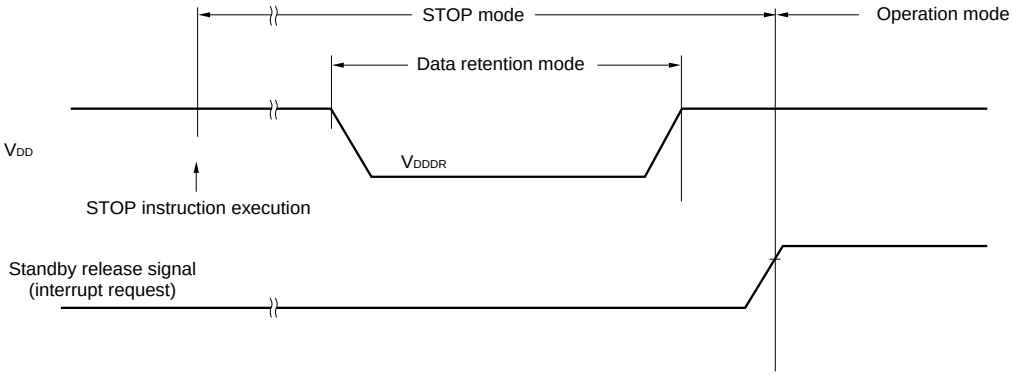
Old:

29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is affected, but data is not retained when a POR reset is affected.



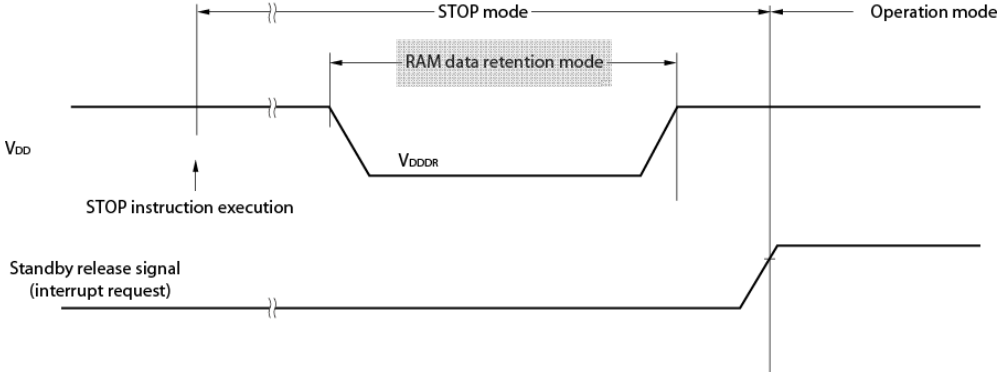
New:

29.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



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9. CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: T_A = –40 to +85°C)

Old:

CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: T_A = –40 to +85°C)

This chapter describes the electrical specifications for the products "A: Consumer applications (T_A = -40 to +85°C)" and "D: Industrial applications (T_A = -40 to +85°C)".

(omitted)

New:

CHAPTER 28 ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications T_A = −40 to +85°C
R5F102xxAxx, R5F103xxAxx
D: Industrial applications T_A = −40 to +85°C
R5F102xxDxx, R5F103xxDxx
G: Industrial applications when T_A = −40 to +105°C products is used in the range of T_A = −40 to +85°C
R5F102xxGxx

(omitted)

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10. CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: T_A = –40 to +105°C)

Old:

CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: T_A = –40 to +105°C)

This chapter describes the electrical specifications for the products "G: Industrial applications (T_A = -40 to +105°C)".

(omitted)

There are following differences between the products "G: Industrial applications (T_A = -40 to +105°C)" and the products “A: Consumer applications, and D: Industrial applications”.

(omitted)

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to **29.1** to **29.10**.

New:

CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T_A = −40 to +105°C

R5F102xxGxx

(omitted)

Remark When RL78/G14 is used in the range of T_A = -40 to +85°C, see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)**.

(omitted)

Operation of products rated “G: Industrial applications (T_A = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

(omitted)

Remark The electrical characteristics of products rated “G: Industrial applications (TA = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to **29.1** to **29.10**.

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