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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A002A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G12 Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G12 Group R5F102xxx, R5F103xxx	Lot No. All lot	Reference Document	RL78/G12 User's Manual: Hardware Rev. 1.00 R01UH0200EJ0100 (Mar. 2012)		

This document describes misstatements found in the RL78/G12 User's Manual: Hardware Rev. 1.00 (R01UH0200EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
1.1 Differences of 1.1 RL78/G12 products (R5F102 and R5F103)	Pages 1 and 2	Outline added
1.6 Outline of Functions	Page 11	Cautions added
Figure 3-1. Memory Map for the R5F10266 and R5F10366	Page 24	Cautions added
Cautions on internal data memory space/control register/general-purpose register	Pages 36, 44, 46	Explanations added
Figure 3-8. Correspondence Between Data Memory and Addressing for the R5F10266 and R5F10366	Page 38	Cautions added
High-speed on-chip oscillator frequency selection register (HOCODIV)	Page 155	Cautions changed
A/D converter mode register 0 (ADM0)	Page 297	Incorrect descriptions revised
A/D conversion time selection	Pages 302, 304	Incorrect descriptions revised
Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector	Pages 670, 671	Incorrect descriptions revised
24.4 Overview of the data flash memory	Page 722	Cautions added
24.6 Security Settings	Page 729	Incorrect descriptions revised
Table 24-12. Security Setting in Each Programming Mode	Page 730	Deleted
24.7 Flash memory programming by self-programming	Page 731	Cautions added
24.7.1 Flash shield window function	Page 733	Incorrect descriptions revised
28.8 Flash memory programming characteristics	Page 804	Specifications determined

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0200EJ0100	
1	1.1 Outline for differences of the RL78/G12 (R5F102 and R5F103) added		Pages 1, 2	Pages 3, 4
2	Cautions on Outline of Functions added		Page 11	Page 5, 6
3	Cautions for Figure 3-1. Memory Map (R5F10266, R5F10366) added		Pages 24	Page 7
4	Explanations for cautions on internal data memory space/control register/general-purpose register added		Pages 36, 44, 46	Page 8
5	Cautions on Figure 3-8. Correspondence Between Data Memory and Addressing for the R5F10266 and R5F10366 added		Page 38	Page 9
6	Cautions on the high-speed on-chip oscillator frequency selection register (HOCODIV) changed		Page 155	Page 10
7	Incorrect descriptions of A/D converter mode register 0 (ADM0) revised		Page 297	Page 11
8	Incorrect descriptions of A/D conversion time selection revised		Pages 302, 304	Pages 12 to 15
9	Incorrect descriptions of Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on reset Circuit and Voltage Detector revised		Pages 670, 671	Pages 16 to 19
10	Cautions on 24.4 Overview of the data flash memory added		Page 722	Page 20
11	Incorrect descriptions of 24.6 Security Settings revised		Page 729	Page 21
12	Table 24-12. Security Setting in Each Programmable Mode deleted		Page 730	Page 22
13	Cautions on 24.7 Flash Memory Programming by Self-Programming added		Page 731	Page 23
14	Incorrect descriptions of 24.7.1 Flash shield window function revised		Page 733	Page 24
15	Specifications of 28.8 Flash Memory Programming Characteristics determined		Page 804	Page 25

Incorrect: Bold with underline, Correct: Gray hatched

1. Outline for differences of the RL78/G12 (R5F102 and R5F103) added

Differences between the R5F102 and R5F103 (pages 1, 2)

Addition:

CHAPTER 1 OUTLINE

1.1 Differences between the R5F102 and R5F103

Differences between the R5F102 and R5F103 of the RL78/G12 are as follows:

- Data flash mounted/not mounted
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels of the serial interface
- DMA function mounted/not mounted
- Safety function mounted/not mounted

1.1.1 Data Flash

The R5F102 mounts 2KB data flash and the R5F103 does not mount the data flash.

Part Number	Data Flash
R5F102 R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 Note	2KB
R5F103 R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note Since the R5F10266 includes small RAM size of 256 bytes, a stack area to execute the data flash library cannot be saved depending on the customer's program specification and writing/erasing to the data flash may not be able to performed.

Caution Since individual library is used when rewriting the flash memory using the user program, flash ROM and RAM areas are used. Refer to the RL78 Family Flash Self-Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual before using these products.

1.1.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency accuracy of the R5F102

Oscillator	Condition	Min.	Max.	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = – 20 to + 85 °C	– 1	+ 1	%
	T_A = – 40 to – 20 °C	– 1.5	+ 1.5	

(2) High-speed on-chip oscillator oscillation frequency accuracy of the R5F103

Oscillator	Condition	Min.	Max.	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = – 40 to + 85 °C	– 5	+ 5	%

1.1.3 Peripheral functions

There are differences of peripheral functions listed in the table below between the R5F102 and R5F103.

RL78/G12		R5F102		R5F103	
		20- and 24-pin products	30-pin products	20- and 24-pin products	30-pin products
Serial Interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I^2C	2 channels	3 channels	None	
DMA Function		2 channels		None	
Safety Function	CRC calculation	Included		None	
	RAM guard	Included		None	
	SFR guard	Included		None	

2. Cautions on Outline of Functions added (Page 11)

Incorrect:

1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H (except timer output of **30-pin products with data flash**)

(1/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Code flash memory		**2 to 16 KB**		4 to 16 KB			
Data flash memory		2 KB	–	2 KB	–	2 KB	–
RAM		**256 B to 1.5 KB** Note 1		**512 B to 1.5 KB** Note 1		512 B to 2KB	
Memory space		1 MB					
(Omitted)							
Timer	16-bit timer	4 channels				8 channels	
	Watchdog timer	1 channel					
	12-bit Interval timer	1 channel					
	Timer output	4/8 Note 2 (PWM Output Note 3: 3/7 Note 2)					

Notes 1. **This is about 639 bytes when the self-programming function and data flash function are used. (For details, see CHAPTER 3)**

2. **In 30-pin products with data flash, when setting to PIOR0 = 1.**

3. The number of outputs varies, depending on the setting of channels in use and the number of the master (see 6.8.3 Operation as multiple PWM output function).

Correct:

1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H (except timer output of the R5F102Ax)

(1/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Code flash memory		2 to 16 KB Note 1		4 to 16 KB			
Data flash memory		2 KB	–	2 KB	–	2 KB	–
RAM		256 B to 1.5 KB		512 B to 1.5 KB		512 B to 2KB	
Address space		1 MB					
(Omitted)							
Timer	16-bit timer	4 channels				8 channels	
	Watchdog timer	1 channel					
	12-bit Interval timer	1 channel					
	Timer output	4/8 Note 2 (PWM Output Note 3: 3/7 Note 2)					

Notes 1. The self-programming function cannot be used for the R5F10266 and R5F10366.

2. In the R5F102Ax, when setting to PIOR0 = 1.

3. The number of outputs varies, depending on the setting of channels in use and the number of the master (see 6.8.3 Operation as multiple PWM output function).

Caution Since individual library is used when rewriting the flash memory using the user program, flash ROM and RAM areas are used. Confirm the RL78 Family Flash Self-Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual before using these products.

3. Cautions for Memory Map (R5F10266, R5F10366) added (Page 24)

Incorrect:

Figure 3-1. Memory Map for the R5F10266 and R5F10366

(Omitted)

Notes 1. **Use of the area FFE20H to FFEFFH is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.**

(Omitted)

Correct:

Figure 3-1. Memory Map for the R5F10266 and R5F10366

(Omitted)

Notes 1. When rewriting the data flash, allocate the stack used for the data flash library to FFEA2H to FFEDFH, and the RAM address used for the data flash and DMA transfer to FFE00H to FFE19H. Fore more details, refer to the RL78 Family Data Flash Library Type04 User's Manual.

(Omitted)

Cautions 2. Since the R5F10266 includes small RAM size of 256 bytes, a stack area to execute the data flash library cannot be saved depending on the customer's program specification and writing/erasing to the data flash may not be able to be performed. For more details, refer to the RL78 Family Data Flash Library Typ04 User's Manual.

3. The self-programming function cannot be used for the R5F10266 and R5F10366.

4. Explanations for cautions on internal data memory space/control register/general-purpose register added (Pages 36, 44, 46)

Incorrect:

Cautions 1. It is prohibited to use the general-purpose register space (FFEE0H to FFEFFH) for fetching instructions or as a stack area.

2. **The internal RAM in the following products cannot be used as stack memory when using the self-programming function and data flash function** (refer to figure 3-1 to 3-6 Memory Map).

R5F10x66, R5F10x67, R5F10x77, R5F10xA7, : FFE20H-FFEFFH
R5F10xA8, R5F10xA9, R5F10xAA
R5F10x68, R5F10x78: FFE20H to FFEFFH, FFC00H to FFC80H
R5F10x69, R5F10x79: FFE20H to FFEFFH, FFB00H to FFC80H
R5F10x6A, R5F10x7A: FFE20H to FFEFFH, FF900H to FFC80H
(x = 2, 3)

Correct:

(Omitted)

Cautions 1. It is prohibited to use the general-purpose register space (FFEE0H to FFEFFH) for fetching instructions or as a stack area.

2. When self-programming or rewriting the data flash, do not allocate the stack used by individual library and RAM address used for the data buffer and DMA transfer to RAM areas of the products shown below. For more details, refer to the RL78 Family Flash Self-Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

R5F10266 : FFE20H to FFEA1H, FFEE0H to FFEFFH
(Allocate the stack used for the data flash library to FFEA2H to FFEDFH, and the RAM address used for the data buffer and DMA transfer to FFE00H to FFE19H.)

R5F102mn, R5F103mn : FFE20H to FFEFFH
m: Pin count symbol (m = 6, 7, A), n: ROM size symbol (n = 7, 8, 9, A)

3. Since RAM areas of the products shown below is used for the self-programming library and data flash library, its area cannot be used (refer to Figures 3-3 to 3-5 Memory Map).

R5F102m8, R5F103m8 : FFC00H-FFC80H
R5F102m9, R5F103m9 : FFB00H-FFC80H
R5F102mA, R5F103mA : FF900H-FFC80H
m: Pin count symbol (m = 6, 7)

5. Cautions on Correspondence Between Data Memory and Addressing (R5F10266, R5F10366) added (page 38)

Incorrect:

Figure 3-8. Correspondence between Data Memory and Addressing for the R5F10266 and R5F10366

(Omitted)

Notes 1. **FFE20H to FFEFFH area used by the self-programming libraries cannot be used when the self-programming function and data flash function are used.**

(Omitted)

Correct:

Figure 3-8. Correspondence between Data Memory and Addressing for the R5F10266 and R5F10366

Notes 1. When rewriting the data flash, allocate the stack used for the data flash library to FFEA2H to FFEDFH, and RAM address for the data buffer and DMA transfer to FFE00H to FFE19H. For more details, refer to the RL78 Family Data Flash Library Type04 User's Manual.

(Omitted)

Cautions 2. Since the R5F10266 includes small RAM size of 256 bytes, a stack area to execute the data flash library cannot be saved depending on the customer's program specification and writing/erasing to the data flash may not be able to be performed. For more details, refer to the RL78 Family Data Flash Library Typ04 User's Manual.

3. The self-programming function cannot be used for the R5F10266 and R5F10366.

6. Cautions on the high-speed on-chip oscillator frequency selection register (HOCODIV) changed (page 155)

Incorrect:

(8) High-speed on-chip oscillator frequency selection register (HOCODIV)

(Omitted)

Cautions 1. Set the HOCODIV register within the operable voltage range before and after the frequency change.

2. When the frequency is changed with the HOCODIV register, use it within the voltage range of the flash operation mode set in the option byte (000C2H).

Option byte (000C2H) value		Flash operation mode	Operating frequency range	Operating voltage range
CMODE1	CMODE2			
1	0	LS (low-speed main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
1	1	HS (high-speed main) mode	1 MHz to 16 MHz	2.4 V to 5.5 V
			1 MHz to 24 MHz	2.7 V to 5.5 V

3. The device operates at the old frequency for the duration of 3 clocks after the frequency value has been changed by using the HOCODIV register. When setting of high-speed on-chip oscillator clock as system clock, and the clock oscillation stabilization wait three minutes further.

4. When changing the frequency of the high-speed on-chip oscillator while X1 oscillation/external oscillation input is set to the system clock, after set the bit 0 (HIOSTOP) of the CSC register to 1, to stop the high-speed on-chip oscillator.

Correct:

(8) High-speed on-chip oscillator frequency selection register (HOCODIV)

(Omitted)

Cautions 1. Set the HOCODIV register within the operable voltage range of the flash operation mode set in the option byte (000C2H) before and after the frequency change.

Option byte (000C2H) value		Flash operation mode	Operating frequency range	Operating voltage range
CMODE1	CMODE2			
1	0	LS (low-speed main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
1	1	HS (high-speed main) mode	1 MHz to 16 MHz	2.4 V to 5.5 V
			1 MHz to 24 MHz	2.7 V to 5.5 V

2. Set the HOCODIV register while the high-speed on-chip oscillator clock (f_{IH}) is selected as the CPU/peripheral hardware clock (f_{CLK}).

3. After the frequency has been changed using the HOCODIV register and the following transition time has been elapsed, the frequency is switched.

- The device operates at the frequency for the duration of 3 clocks before the frequency has been changed.
- The CPU/peripheral hardware clock waits for maximum 3 clocks at the frequency after the frequency has been changed.

7. Incorrect descriptions of A/D converter mode register 0 (ADM0) revised (page 297)

Incorrect:

(2) A/D converter mode register 0 (ADM0)

(Omitted)

Cautions **1. Change the ADMD, FR2 to FR0, LV1, LV0, and ADCE bits while conversion is stopped or on standby (ADCS = 0).**

2. Do not change the ADCE and ADCS bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in 10.7 A/D Converter Setup Flowchart.

Correct:

(2) A/D converter mode register 0 (ADM0)

(Omitted)

Cautions 1. Change the ADMD, FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).

2. Do not set ADCS = 1 and ADCE = 0.

3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction.

Be sure to set these bits in the order described in 10.7 A/D Converter Setup Flowchart.

8. Incorrect descriptions of A/D conversion time selection revised (pages 302 and 304)

Incorrect:

Table 10-3. A/D Conversion Time Selection

(2) Low voltage Mode[Note 1]

When there is no stabilization wait time (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock	Conversion Time	Conversion Time Selection					
									1.8 V ≤ V_{DD} ≤ 5.5 V				**Note 2**	**Note 3**
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	1	0	0	Low voltage 1	f_{CLK}/32	19 f_{AD} (Number of sampling clock : 7 f_{AD})	608/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	38 μs	25.33 μs
0	1	0				f_{CLK}/16		304/f_{CLK}			76 μs	38 μs	19 μs	12.67 μs
0	1	1				f_{CLK}/8		152/f_{CLK}		76 μs	38 μs	19 μs	9.5 μs **Note 4**	6.33 μs
1	0	0				f_{CLK}/6		114/f_{CLK}		57 μs	28.5 μs	14.25 μs **Note 4**	7.125 μs **Note 4**	4.75 μs
1	0	1				f_{CLK}/5		95/f_{CLK}	95 μs	47.5 μs	23.75 μs	11.875 μs **Note 4**	5.938 μs **Note 4**	3.96 μs
1	1	0				f_{CLK}/4		76/f_{CLK}	76 μs	38 μs	19 μs	9.5 μs **Note 4**	4.75 μs **Note 4**	3.17 μs **Note 5**
1	1	1				f_{CLK}/2		38/f_{CLK}	38 μs	19 μs	9.5 μs **Note 4**	4.75 μs **Note 4**	2.375 μs **Note 5**	Setting prohibited
0	0	1	0	1	Low voltage 2	f_{CLK}/32	17 f_{AD} (Number of sampling clock : 5 f_{AD})	544/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68 μs	34 μs	22.667 μs
0	1	0				f_{CLK}/16		272/f_{CLK}			68 μs	34 μs	17 μs	11.333 μs
0	1	1				f_{CLK}/8		136/f_{CLK}		68 μs	34 μs	17 μs	8.5 μs **Note 4**	5.667 μs
1	0	0				f_{CLK}/6		102/f_{CLK}		51 μs	25.5 μs	12.75 μs **Note 4**	6.375 μs **Note 4**	4.25 μs
1	0	1				f_{CLK}/5		85/f_{CLK}	85 μs	42.5 μs	21.25 μs	10.625 μs **Note 4**	5.313 μs **Note 4**	3.542 μs
1	1	0				f_{CLK}/4		68/f_{CLK}	68 μs	34 μs	17 μs	8.5 μs **Note 4**	4.25 μs **Note 4**	2.833 μs **Note 5**
1	1	1				f_{CLK}/2		34/f_{CLK}	34 μs	17 μs	8.5 μs **Note 4**	4.25 μs **Note 4**	2.125 μs **Note 5**	Setting prohibited
Other than the above						–	–	–	Setting prohibited					

(4) Low voltage Mode[Note 1]

When there is stabilization wait time [Note 2] (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of stabilization wait clock	Number of Conversion Clock	Stabilization Wait Time + Conversion Time	Stabilization Wait Time + Conversion Time Selection					
										1.8 V ≤ V_{DD} ≤ 5.5 V				**Note3**	**Note4**
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	1	**0**	0	Low voltage 1	f_{CLK}/32	2 f_{AD}	19 f_{AD} (Number of sampling clock :7 f_{AD})	672/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	84 μs	42 μs	28 μs
0	1	0				f_{CLK}/16			336/f_{CLK}			84 μs	42 μs	21 μs	14 μs
0	1	1				f_{CLK}/8			168/f_{CLK}		84 μs	42 μs	21 μs	10.5 μs **Note 5**	7 μs
1	0	0				f_{CLK}/6			126/f_{CLK}		63 μs	31.25 μs	15.75 μs **Note 5**	7.875 μs **Note 5**	5.25 μs
1	0	1				f_{CLK}/5			105/f_{CLK}	105 μs	52.5 μs	26.25 μs	13.125 μs **Note 5**	6.563 μs **Note 5**	4.38 μs
1	1	0				f_{CLK}/4			84/f_{CLK}	84 μs	42 μs	21 μs	10.5 μs **Note 5**	5.25 μs **Note 5**	3.5 μs **Note 6**
1	1	1				f_{CLK}/2			42/f_{CLK}	42 μs	21 μs	10.5 μs **Note 5**	5.25 μs **Note 5**	2.625 μs **Note 6**	Setting prohibited
0	0	1	**0**	1	Low voltage 2	f_{CLK}/32		17 f_{AD} (Number of sampling clock :5 f_{AD})	608/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	38 μs	25.33 μs
0	1	0				f_{CLK}/16			304/f_{CLK}			76 μs	38 μs	19 μs	12.67 μs
0	1	1				f_{CLK}/8			152/f_{CLK}		76 μs	38 μs	19 μs	9.5 μs **Note 5**	6.33 μs
1	0	0				f_{CLK}/6			114/f_{CLK}		57 μs	28.5 μs	14.25 μs **Note 5**	7.125 μs **Note 5**	4.75 μs
1	0	1				f_{CLK}/5			95/f_{CLK}	95 μs	47.5 μs	23.75 μs	11.875 μs **Note 5**	5.938 μs **Note 5**	3.96 μs
1	1	0				f_{CLK}/4			76/f_{CLK}	76 μs	38 μs	19 μs	9.5 μs **Note 5**	4.75 μs **Note 5**	3.17 μs **Note 6**
1	1	1				f_{CLK}/2			38/f_{CLK}	38 μs	19 μs	9.5 μs **Note 5**	4.75 μs **Note 5**	2.375 μs **Note 6**	Setting prohibited
Other than the above						–	–	–	–	Setting prohibited					

(Omitted)

Cautions 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

Correct:

Table 10-3. A/D Conversion Time Selection

(2) Low voltage Mode[Note 1]

When there is no stabilization wait time (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock	Conversion Time	Conversion Time Selection					
									1.8 V ≤ V_{DD} ≤ 5.5 V				**Note 2**	**Note 3**
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	1	1	0	Low voltage 1	f_{CLK}/32	19 f_{AD} (Number of sampling clock : 7 f_{AD})	608/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	38 μs	25.33 μs
0	1	0				f_{CLK}/16		304/f_{CLK}			76 μs	38 μs	19 μs	12.67 μs
0	1	1				f_{CLK}/8		152/f_{CLK}		76 μs	38 μs	19 μs	9.5 μs **Note 4**	6.33 μs
1	0	0				f_{CLK}/6		114/f_{CLK}		57 μs	28.5 μs	14.25 μs **Note 4**	7.125 μs **Note 4**	4.75 μs
1	0	1				f_{CLK}/5		95/f_{CLK}	95 μs	47.5 μs	23.75 μs	11.875 μs **Note 4**	5.938 μs **Note 4**	3.96 μs
1	1	0				f_{CLK}/4		76/f_{CLK}	76 μs	38 μs	19 μs	9.5 μs **Note 4**	4.75 μs **Note 4**	3.17 μs **Note 5**
1	1	1				f_{CLK}/2		38/f_{CLK}	38 μs	19 μs	9.5 μs **Note 4**	4.75 μs **Note 4**	2.375 μs **Note 5**	Setting prohibited
0	0	1	1	1	Low voltage 2	f_{CLK}/32	17 f_{AD} (Number of sampling clock : 5 f_{AD})	544/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68 μs	34 μs	22.667 μs
0	1	0				f_{CLK}/16		272/f_{CLK}			68 μs	34 μs	17 μs	11.333 μs
0	1	1				f_{CLK}/8		136/f_{CLK}		68 μs	34 μs	17 μs	8.5 μs **Note 4**	5.667 μs
1	0	0				f_{CLK}/6		102/f_{CLK}		51 μs	25.5 μs	12.75 μs **Note 4**	6.375 μs **Note 4**	4.25 μs
1	0	1				f_{CLK}/5		85/f_{CLK}	85 μs	42.5 μs	21.25 μs	10.625 μs **Note 4**	5.313 μs **Note 4**	3.542 μs
1	1	0				f_{CLK}/4		68/f_{CLK}	68 μs	34 μs	17 μs	8.5 μs **Note 4**	4.25 μs **Note 4**	2.833 μs **Note 5**
1	1	1				f_{CLK}/2		34/f_{CLK}	34 μs	17 μs	8.5 μs **Note 4**	4.25 μs **Note 4**	2.125 μs **Note 5**	Setting prohibited
Other than the above						–	–	–	Setting prohibited					

(Omitted)

Cautions 1. Rewrite the FR2 to FR0, LV1, and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

(4) Low voltage Mode[Note 1]

When there is stabilization wait time [Note 2] (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of stabilization wait clock	Number of Conversion Clock	Stabilization Wait Time + Conversion Time	Stabilization Wait Time + Conversion Time Selection					
										1.8 V ≤ V_{DD} ≤ 5.5 V				**Note3**	**Note4**
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	1	1	0	Low voltage 1	f_{CLK}/32	2 f_{AD}	19 f_{AD} (Number of sampling clock :7 f_{AD})	672/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	84 μs	42 μs	28 μs
0	1	0				f_{CLK}/16			336/f_{CLK}			84 μs	42 μs	21 μs	14 μs
0	1	1				f_{CLK}/8			168/f_{CLK}		84 μs	42 μs	21 μs	10.5 μs **Note 5**	7 μs
1	0	0				f_{CLK}/6			126/f_{CLK}		63 μs	31.25 μs	15.75 μs **Note 5**	7.875 μs **Note 5**	5.25 μs
1	0	1				f_{CLK}/5			105/f_{CLK}	105 μs	52.5 μs	26.25 μs	13.125 μs **Note 5**	6.563 μs **Note 5**	4.38 μs
1	1	0				f_{CLK}/4			84/f_{CLK}	84 μs	42 μs	21 μs	10.5 μs **Note 5**	5.25 μs **Note 5**	3.5 μs **Note 6**
1	1	1				f_{CLK}/2			42/f_{CLK}	42 μs	21 μs	10.5 μs **Note 5**	5.25 μs **Note 5**	2.625 μs **Note 6**	Setting prohibited
0	0	1	1	1	Low voltage 2	f_{CLK}/32		17 f_{AD} (Number of sampling clock :5 f_{AD})	608/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	38 μs	25.33 μs
0	1	0				f_{CLK}/16			304/f_{CLK}			76 μs	38 μs	19 μs	12.67 μs
0	1	1				f_{CLK}/8			152/f_{CLK}		76 μs	38 μs	19 μs	9.5 μs **Note 5**	6.33 μs
1	0	0				f_{CLK}/6			114/f_{CLK}		57 μs	28.5 μs	14.25 μs **Note 5**	7.125 μs **Note 5**	4.75 μs
1	0	1				f_{CLK}/5			95/f_{CLK}	95 μs	47.5 μs	23.75 μs	11.875 μs **Note 5**	5.938 μs **Note 5**	3.96 μs
1	1	0				f_{CLK}/4			76/f_{CLK}	76 μs	38 μs	19 μs	9.5 μs **Note 5**	4.75 μs **Note 5**	3.17 μs **Note 6**
1	1	1				f_{CLK}/2			38/f_{CLK}	38 μs	19 μs	9.5 μs **Note 5**	4.75 μs **Note 5**	2.375 μs **Note 6**	Setting prohibited
Other than the above						–	–	–	–	Setting prohibited					

(Omitted)

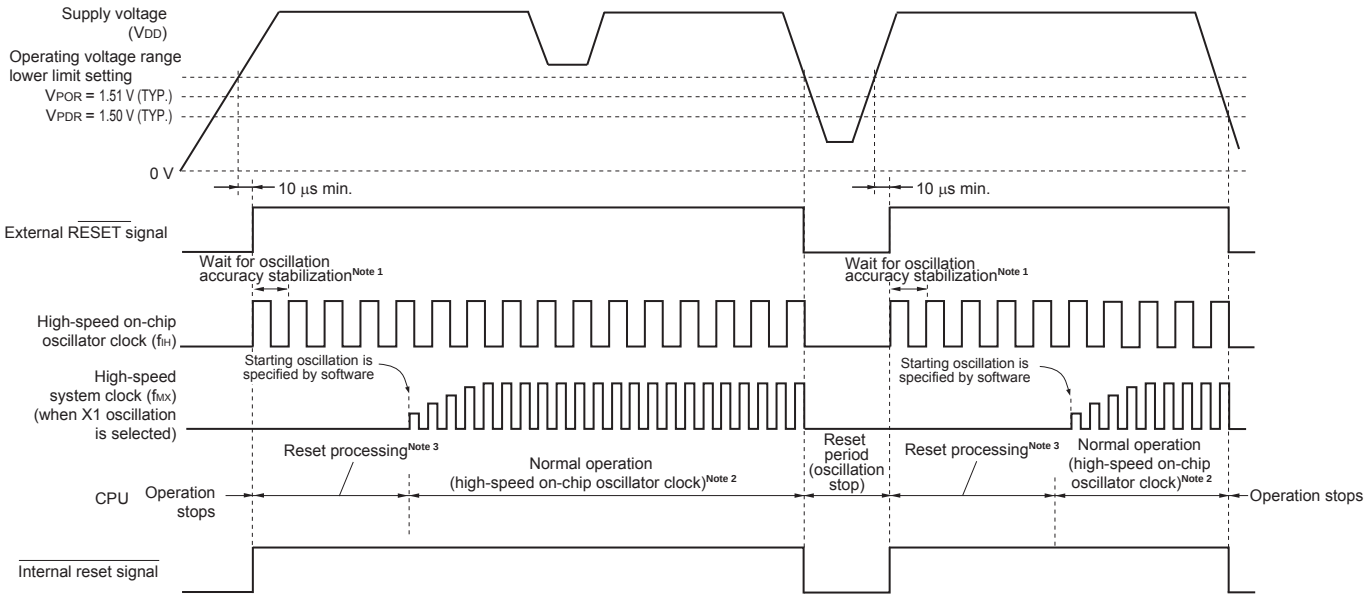
Cautions 1. Rewrite the FR2 to FR0, LV1, and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

9. Incorrect descriptions of the power-on reset circuit on Figure 19-2 revised (pages 670 and 671)

Incorrect:

Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector

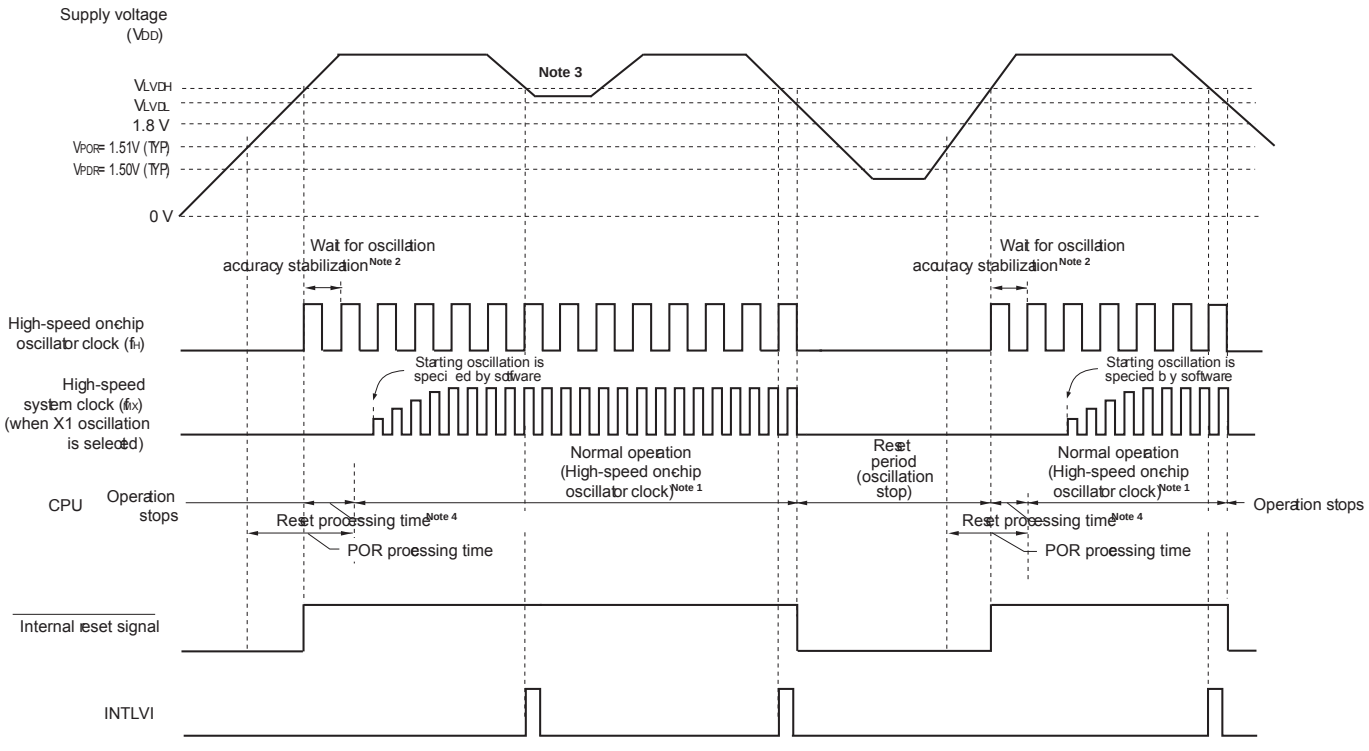
(a) When LVD is OFF (option byte 000C1H: VPOC2 = 1)



(Omitted)

Notes 3. Reset processing time: 265 to 407 μs

(b) When LVD is interrupt & reset mode (option byte 000C1H/LVIMDS1, LVIMDS0 = 1, 0)



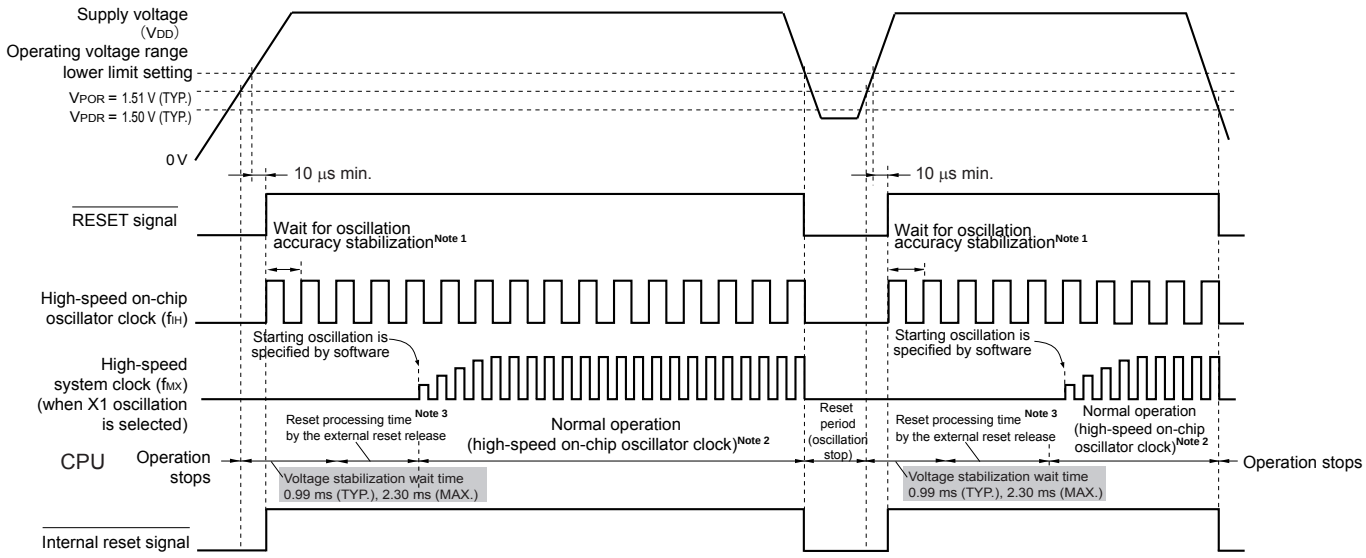
(Omitted)

Notes 4. Reset processing time: 497 to 720 μs

Correct:

Figure 19-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector

(1) When the external reset input via $\overline{\text{RESET}}$ pin is used



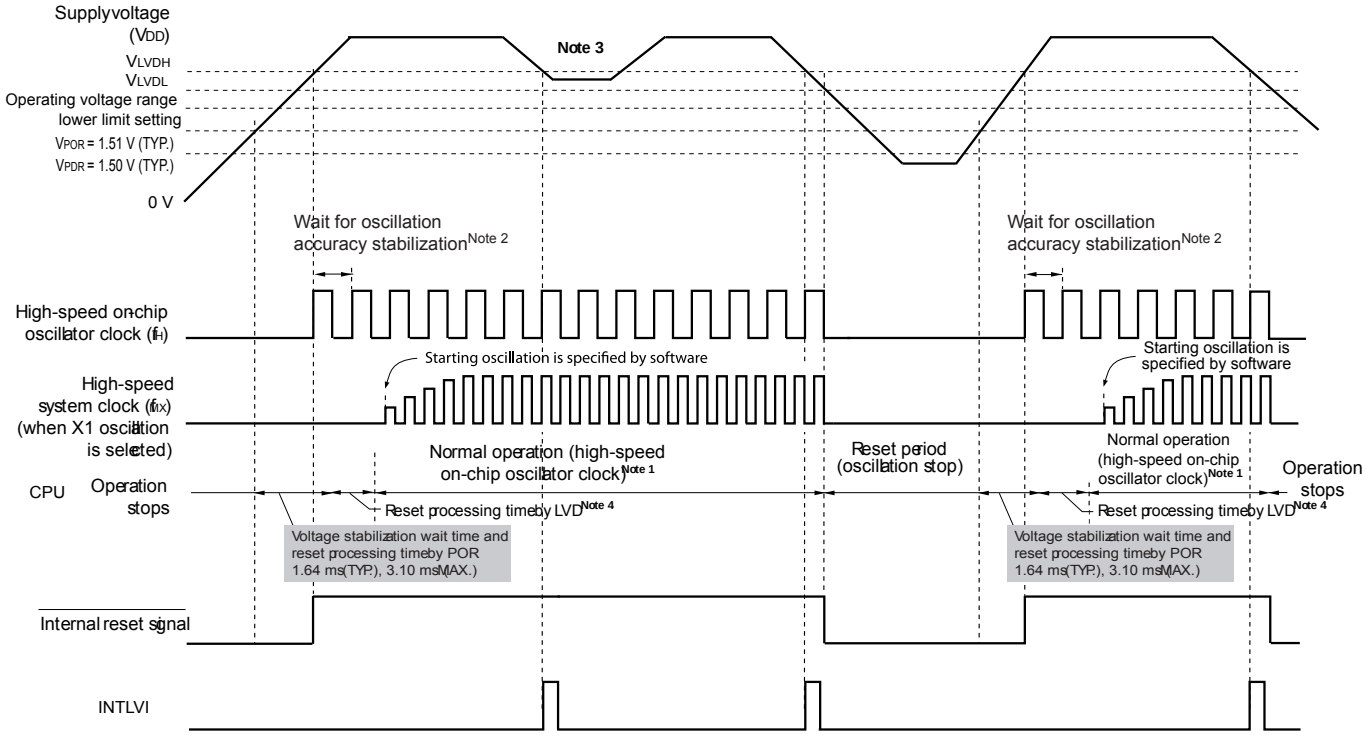
(Omitted)

Notes 3. The time until normal operation is started require the following “the reset processing time by the external reset release” required after $\overline{\text{RESET signal}}$ has been set to high-level(1), in addition to “the voltage stabilization wait time” required after the voltage has reached VPOR (1.51 V (TYP.)).

Reset processing time by the external reset release: 0.672 ms (TYP.), 0.832 ms (MAX.) (When LVD is used)

0.399 ms (TYP.), 0.519 ms (MAX.) (When LVD off)

(2) LVD interrupt & reset mode (option byte 000C1H/LVIMDS1, LVIMDS0 = 1, 0)

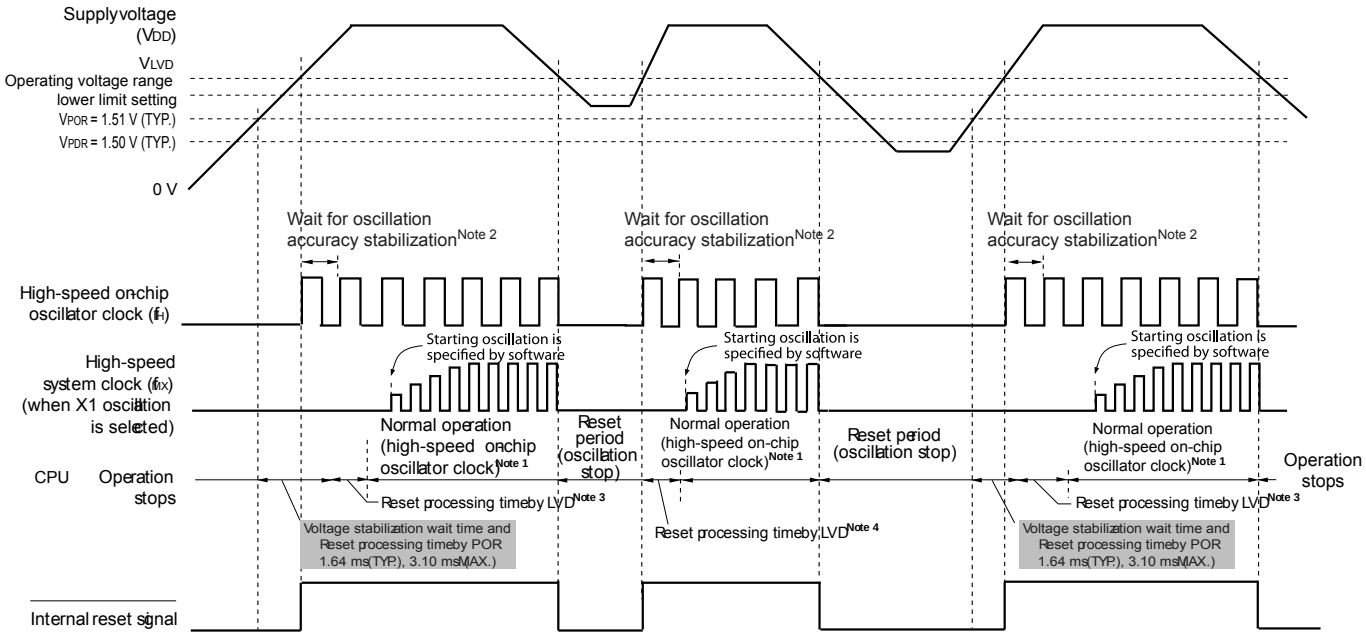


(Omitted)

Note 4. The time until normal operation is started require the following “the reset processing time by LVD” required after the voltage has reached LVD detection level (VLVDH), in addition to “the reset processing time by POR” and “the voltage stabilization wait time” required after the voltage has reached VPOR (1.51 V (TYP.)).

Reset processing time by LVD: 0 ms to 0.0701 ms (MAX.)

(3) LVD reset mode (option byte 000C1H/LVIMDS1, LVIMDS0 = 1, 1)



(Omitted)

Note 3. The time until normal operation is started require the following “the reset processing time by LVD” required after the voltage has reached LVD detection level (VLVD), in addition to “the reset processing time by POR” and “the voltage stabilization wait time” required after the voltage has reached VPOR (1.51 V (TYP.)).

Reset processing time by LVD: 0 ms to 0.0701 ms (MAX.)

4. When supply voltage falls and returns after only an internal reset occurs by the voltage detection circuit (LVD), the following “the reset processing time by LVD” is required after the voltage has reached LVD detection level (VLVD).

Reset processing time by LVD: 0.0629 ms (TYP.), 0.0701 ms (MAX.)

10. Cautions on overview of the data flash memory added (page 722)

Incorrect:

An overview of the data flash memory is provided below.

- The data flash memory can be written to by using the flash memory programmer or an external device
- Programming is performed in 8-bit units
- Blocks can be deleted in 1 KB units
- The only access by CPU instructions is byte reading (**4 clock + wait 3 clock cycles**)
- Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions (code fetching)
- Instructions can be executed from the code flash memory while rewriting the data flash memory (That is, Back Ground Operation (BGO) is supported)
- Accessing the data flash memory is not possible while rewriting the code flash memory (during self programming)
- Because the data flash memory is stopped after a reset ends, the data flash control register (DFLCTL) must be set up in order to use the data flash memory
- Manipulating the DFLCTL register is not possible while rewriting the data flash memory
- Transition the HALT, STOP mode is not possible while rewriting the data flash memory

Correct:

An overview of the data flash memory is provided below. For more details of rewriting the data flash memory, refer to the RL78 Family Data Flash Library Type04 User's Manual.

- The data flash memory can be written to by using the flash memory programmer or an external device
- Programming is performed in 8-bit units
- Blocks can be deleted in 1 KB units
- The only access by CPU instructions is byte reading (1 clock + wait 3 clock cycles)
- Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions (code fetching)
- Instructions can be executed from the code flash memory while rewriting the data flash memory (That is, Back Ground Operation (BGO) is supported)
- Accessing the data flash memory is not possible while rewriting the code flash memory (during self programming)
- Because the data flash memory is stopped after a reset ends, the data flash control register (DFLCTL) must be set up in order to use the data flash memory
- Manipulating the DFLCTL register is not possible while rewriting the data flash memory
- Transition the HALT, STOP mode is not possible while rewriting the data flash memory

Cautions 1. While the data flash is being rewritten, interrupts are disabled only for the R5F10266. Execute the data flash library in the state where the IE flag is cleared (0) by the DI instruction.

2. The high-speed on-chip oscillator needs to oscillate while the data flash is being rewritten. When stopping the high-speed on-chip oscillator, oscillate the high-speed on-chip oscillator clock (HIOSTOP = 0) and execute the data flash library after 30 μs elapses.

11. Incorrect descriptions of Security Settings revised (page 729)

Incorrect:

24.6 Security Settings

The RL78/G12 supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed by using the Security Set command.

(Omitted)

The block erase, write, and rewriting boot cluster0 commands are enabled by default when the flash memory is shipped. **Security can be set by on-board/off-board programming and self programming.** The security settings can be used in combination.

Table 24-11 shows the relationship between the erase and write commands when the RL78/G12 security function is enabled.

Caution The security function of the flash programmer does not support self-programming.

Correct:

24.6 Security Settings

The RL78/G12 supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed by using the Security Set command.

(Omitted)

The block erase, write, and rewriting boot cluster0 commands are enabled by default when the flash memory is shipped. Security can be set only by on-board/off-board programming. The security settings can be used in combination.

Table 24-11 shows the relationship between the erase and write commands when the RL78/G12 security function is enabled.

Caution The security function of the flash programmer does not support self-programming.

12. Security Settings in self-programming mode deleted (page 730)

Incorrect:

Table 24-12. Security Setting in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erasure	Use the GUI of dedicated flash memory programmer.	Cannot be disabled after setting.
Prohibition of writing		Execute security release command
Prohibition of rewriting boot cluster 0		Cannot be disabled after setting.

Caution The security release command can be applied only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erasure	Use the set sets information library.	Cannot be disabled after setting.
Prohibition of writing		Execute the security release command during on-board/off-board programming. (The security setting cannot be disabled during self programming.)
Prohibition of rewriting boot cluster 0		Cannot be disabled after setting.

Correct:

Table 24-12. Security Setting in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erasure	Use the GUI of dedicated flash memory programmer.	Cannot be disabled after setting.
Prohibition of writing		Execute security release command
Prohibition of rewriting boot cluster 0		Cannot be disabled after setting.

Caution The security release command can be applied only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.

13. Cautions on Flash Memory Programming by Self-Programming added (page 731)

Incorrect:

24.7 Flash Memory Programming by Self-Programming

The RL78/G12 supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/G12 self-programming library, it can be used to upgrade the program in the field.

Cautions 1. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.

(Omitted)

Correct:

The RL78/G12 supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/G12 self-programming library, it can be used to upgrade the program in the field.

Cautions 1. Interrupts are disabled during self-programming. Execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction.

(Omitted)

3. The high-speed on-chip oscillator needs to oscillate during self-programming. When stopping the high-speed on-chip oscillator, oscillate the high-speed on-chip oscillator clock (HIOSTOP = 0) and execute the self-programming library after 30 μs elapses.

4. The self-programming function cannot be used for the R5F10266 and R5F10366.

14. Incorrect descriptions of the Flash shield window function revised (page 733)

Incorrect:

24. 7.1 Flash shield window function

(Omitted)

The window range can be set by specifying the start and end blocks. The window range can be set or changed during both on-board/off-board programming **and self programming**.

(Omitted)

Figure 24-14. Setting and changing of the flash shield window function and relations with commands

Programming condition	Setting/Changing window range	Execution command	
		Block erasure	Writing
During self-programming	Specify the start block and end block of the window in the set flash self programming.	Block erasure can be done only in the window range.	Writing can be done only in the window range.
During on-board/off-board programming	Specify the start block and end block of the window on the GUI of the dedicated flash memory programmer.	Block erasure can be done also outside the window range.	Writing can be done also outside the window range.

Note To prohibit writing and erasing during on-board/off-board programming, refer to "24.6 Security Settings."

Correct:

24. 7.1 Flash shield window function

(Omitted)

The window range can be set by specifying the start and end blocks. The window range can be set or changed only during on-board/off-board programming.

(Omitted)

Figure 24-14. Setting and changing of the flash shield window function and relations with commands

Programming condition	Setting/Changing window range	Execution command	
		Block erasure	Writing
During on-board/off-board programming	Specify the start block and end block of the window on the GUI of the dedicated flash memory programmer.	Block erasure can be done also outside the window range.	Writing can be done also outside the window range.

Note To prohibit writing and erasing during on-board/off-board programming, refer to "24.6 Security Settings."

15. Specifications of the Flash Memory Programming Characteristics determined (page 804)

Incorrect:

28.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Code flash memory rewritable times	C_{erwr}	1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.	Retained for 20 years (Self/serial programming)Note	1,000			Times
Data flash memory rewritable times			Retained for 1 years (Self/serial programming)Note		1,000,000		
			Retained for 5 years (Self/serial programming)Note	**100,000**			

Note When using flash memory programmer and Renesas Electronics self programming library.

Caution This specifications show target values, which may change after device evaluation.

Correct:

28.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Code flash memory rewritable times Note 1,2,3	C_{erwr}	Retaining years: 20 years	Ta = 85 °C Note 3	1,000			Times
Data flash memory rewritable times Note 1,2,3		Retaining year: 1 year	Ta = 25 °C Note 3		1,000,000		
		Retaining years: 5 years	Ta = 85 °C Note 3	100,000			
		Retaining years: 20 years	Ta = 85 °C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library.

3. This characteristics is shown as the flash memory characteristics and based on Renesas Electronics reliability test.

Issued Document History

RL78/G12 User's Manual: Hardware Rev 1.00, incorrect description notice, issued document history

Document Number	Issue Date	Description
TN-RL*- A002A /E	Oct. 11, 2012	First edition issued Incorrect descriptions of No.1 to No.15 revised