To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A744A/E	Rev.	1.00
Title	Correction of errors in the SH7280 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7280 Group	Lot No. All lots	Reference Document	SH7280 Group Hardware Manual Rev1.00 REJ09B0393-0100		

This update is to inform you of corrections to errors in the hardware manual for the applicable products indicated above.

The required changes are given in detail below.

<Addition and corrections>

Section 7 User Break Controller

- The following has been added to section 7, User Break Controller (UBC), on page 196.

[After change]

The UBC has the user break interrupt as an interrupt source.

Table 7.4 gives details of this interrupt source.

A user break interrupt is generated when any of the compare–match flag bits (SCMFD3 to 0 and SCMFC3 to 0) in the break control register (BRCR) is set to 1.

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 7.4 Interrupt Source

Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	Interrupt Level
User break	User break Interrupt	—	SCMFD3, SCMFD2, SCMFD1, SCMFD0, SCMFC3, SCMFC2, SCMFC1, SCMFC0	Fixed at 15

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Section 8 Data Transfer Controller (DTC)

- The following has been added to the notes for table 8.11 under 8.5.9, DTC Bus Release Timing on page 234 in section 8, Data Transfer Controller (DTC)

  [After change]

  The following limitation applies to setting 2.

  Set the frequency control register (FRQCR) so that IΦ:BΦ:PΦ:MΦ:AΦ is 8:4:4:4:4 or 8:4:4:8:4.

  The following limitation applies to setting 3.

  Set the DTPR bit in BSCEHR to 0. Setting this bit to 1 is prohibited.

- The following has been added to the notes for 8.5.10, DTC Activation Priority Order on page 236, in section 8, Data Transfer Controller (DTC).

  [After the change]

  Although transfer starts for the first source from which a request was received when a DTC request is generated before the next activation trigger, when an activation trigger with higher priority has arrived before generation of the DTC request, transfer starts for the source with higher priority. Generation of the DTC request varies depending on the operation state of the internal bus.

Section 9 Bus State Controller (BSC)

- The following amendments have been made to the explanation under 9.4.8, Bus Function Extending Register (BSCEHR) on page 302 in section 9, Bus State Controller (BSC).

  [Before change]

  Description of the DTBST bit

  1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ: Mϕ: Aϕ = 8 : 4 : 4 : 4 : 4, 4 : 2 : 2 : 2 : 2, or 2 : 1 : 1 : 1 : 1.

  Description of the DTPR bit

  Note that DTC transfer is always started according to the DTC activation priority when multiple DTC activation requests are generated while the DTC is active.

  Notes: When this bit is set to 1, the following restrictions apply.

  1. The vector information must be stored in the on-chip ROM or on-chip RAM.
  2. The transfer information must be stored in the on-chip RAM.
  3. The function for skipping the transfer information read step is always disabled.

  [After change]

  Description of the DTBST bit

  1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ: Mϕ: Afϕ = 8 : 4 : 4 : 4 : 4, or 8 : 4 : 4 : 8 : 4.

Description of the DTPR bit

For details, refer to section 8.5.10, DTC Activation Priority Order.

Notes: When this bit is set to 1, the following restrictions apply.

1. The vector information must be stored in the on-chip ROM or on-chip RAM.
2. The transfer information must be stored in the on-chip RAM.
3. The function for skipping the transfer information read step is always disabled.
4. Set DTLOCK = 0. The setting DTLOCK = 1 is prohibited.

- The following has been added to the notes for table 9.17 under 9.5.7, Burst ROM (Clock Asynchronous) Interface on page 360 in section 9, Bus State Controller (BSC).

[After change]

Only the DMAC is capable of transfer with 16 bytes as the unit of access. The largest unit of access for the DTC and CPU is 32 bits.

- The following amendment has been made to the explanation under 9.5.9, Burst ROM (Clock Synchronous) Interface on page 367 in section 9, Bus State Controller (BSC).

[Before change]

These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, using 16-byte read by cache fill in the cache-enabled space or 16-byte read by the DMA is recommended.

[After change]

These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, 16-byte read by the DMA is recommended.

- The following explanation has been added on page 380 in section 9, Bus State Controller (BSC).

[After change]

9.6.1 Interrupt Sources

The BSC has the compare–match interrupt (CMI) as an interrupt source.

Table 9.23 gives details of this interrupt source. The compare–match interrupt enable (CMIE) bit in the refresh timer control/status register (RTCSR) enables or disables this interrupt source.

Setting of the compare–match flag in the RTCSR to 1 while the setting of the compare–match interrupt enable (CMIE) bit is 1 leads to the generation of a compare–match interrupt (CMI).

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 9.23

Name	Interrupt Sources	Interrupt enable bit	Interrupt Flag
CMI	compare–match interrupt	CMIE	CMF

Section 10 Direct Memory Access Controller (DMAC)

- The following explanation has been added on page 431 in section 10, Direct Memory Access Controller (DMAC).

[After change]

10.5 Interrupt Sources

10.5.1 Interrupt Sources and Order of Priority

The interrupt sources of the DMAC are the data transfer end interrupt (DEI) and data transfer half-end interrupt (HEI) for each channel.

The interrupt sources and their order of priority are listed in table 10.11.

The IE bit and HIE bits in the DMA channel control registers (CHCRs) enable or disable the respective interrupt sources. Furthermore, the interrupt requests are independently conveyed to the interrupt controller.

A data-transfer end interrupt(DEI) is generated when, in the DMA channel control register (CHCR), the transfer end flag is set to 1 while the setting of the transfer end interrupt enable (IE) bit is 1.

A data-transfer 1/2 end interrupt (HEI) is generated when, in the DMA channel control register (CHCR), the half-end flag is set to 1 while the setting of the half-end interrupt enable (HIE) bit is 1.

Clearing the interrupt flag bits to 0 cancels the interrupt requests.

Priority among the channels is adjustable by the interrupt controller. The order of priority for interrupts of a given channel is fixed. For details, refer to section 6, Interrupt Controller.

Table 10.11 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable	Interrupt Flag	Priority
0	Data transfer end interrupt (TEI_0)	IE	TE	High
	Data transfer half end interrupt (HEI_0)	HIE	HE	
1	Data transfer end interrupt (TEI_1)	IE	TE	
	Data transfer half end interrupt (HEI_1)	HIE	HE	
2	Data transfer end interrupt (TEI_2)	IE	TE	
	Data transfer half end interrupt (HEI_2)	HIE	HE	
3	Data transfer end interrupt (TEI_3)	IE	TE	
	Data transfer half end interrupt (HEI_3)	HIE	HE	
4	Data transfer end interrupt (TEI_4	IE	TE	
	Data transfer half end interrupt (HEI_4)	HIE	HE	
5	Data transfer end interrupt (TEI_5)	IE	TE	
	Data transfer half end interrupt (HEI_5)	HIE	HE	
6	Data transfer end interrupt (TEI_6)	IE	TE	
	Data transfer half end interrupt (HEI_6)	HIE	HE	
7	Data transfer end interrupt (TEI_7)	IE	TE	
	Data transfer half end interrupt (HEI_7)	HIE	HE	Low

Section 14 Compare Match Timer (CMT)

- The following has been added to the explanation under 14.4.1, Interrupt Sources and DTC/DMA Transfer Requests on page 730 in section 14, Compare Match Timer (CMT).

[After change]

Table 14.2 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag Bit	DMAC/DTC Activation	Priority
0	CMI0	CMIE	CMF	Possible	High
1	CMI1	CMIE	CMF	Possible	Low

Section 15 Watchdog Timer (WDT)

- The following has been added to section 15, Watchdog Timer (WDT), on page 749.

[After change]

15.5.1 Interrupt Sources

The watchdog timer has the interval timer interrupt as an interrupt source.

Table 15.3 gives details of this interrupt source.

This source generates an interval timer interrupt when the interval timer overflow flag (IOVF) bit in the watchdog timer control/status register (WTCSR) is set to 1.

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 15.3 Interrupt Sources

Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag Bit
ITI	Interval timer	—	Interval timer overflow flag (IOVF)

Section 16 Serial Communication Interface (SCI)

- The following amendments have been made to the explanation under 16.3.7, Serial Status Register (SCSSR) on page 763 to 768 in section 16, Serial Communication Interface (SCI).

[Before change]

By a power-on reset or in standby mode

[After change]

By a power-on reset or in module standby mode

- The following amendments have been made to the figure 16.12, Sample Flowchart for Receiving Serial Data (1) on page 801 in section 16, Serial Communication Interface (SCI).

[Before change]

Set the CKE1 and CKE0 bits in SCSCR (TE and RE bits are 0).

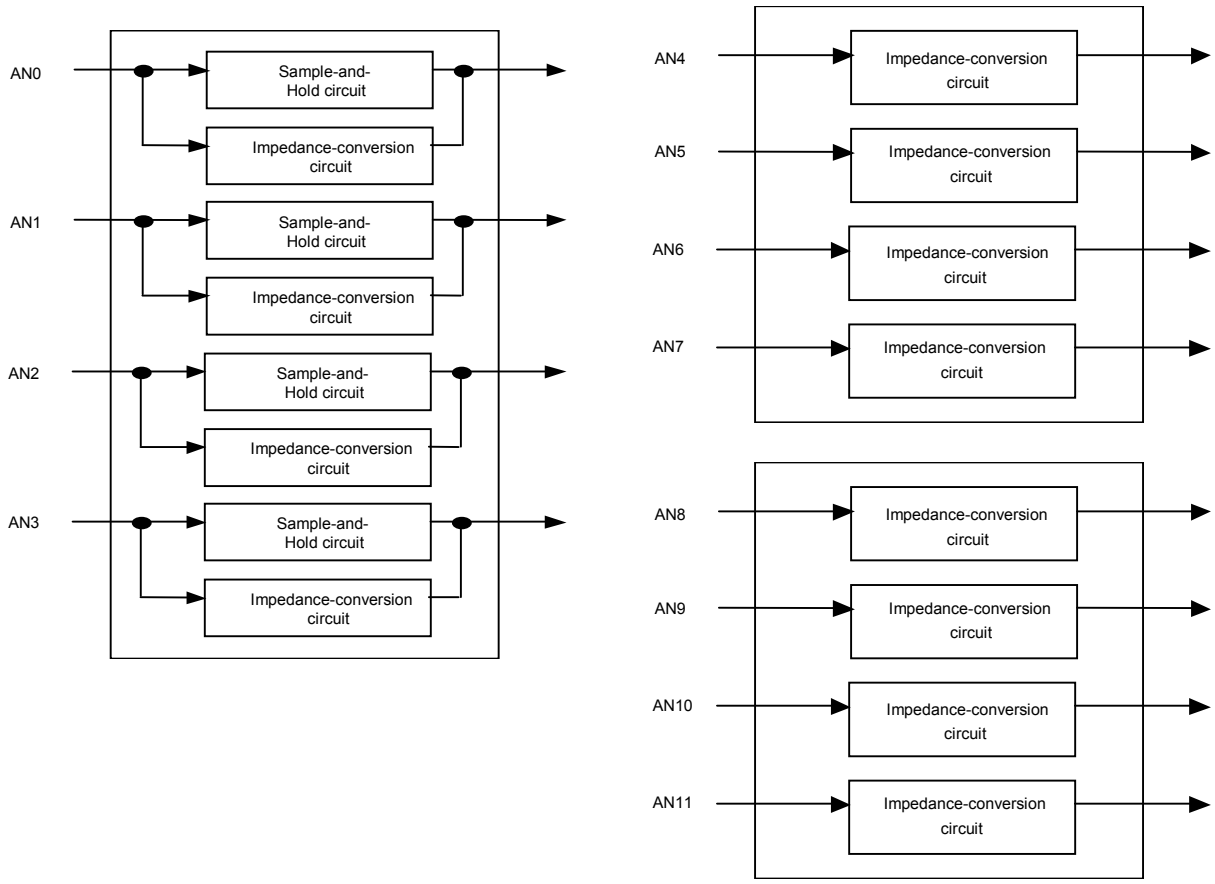
[After change]

Read the receive data register (SCRDR) and clear the RDRF flag in SCSSR to 0.

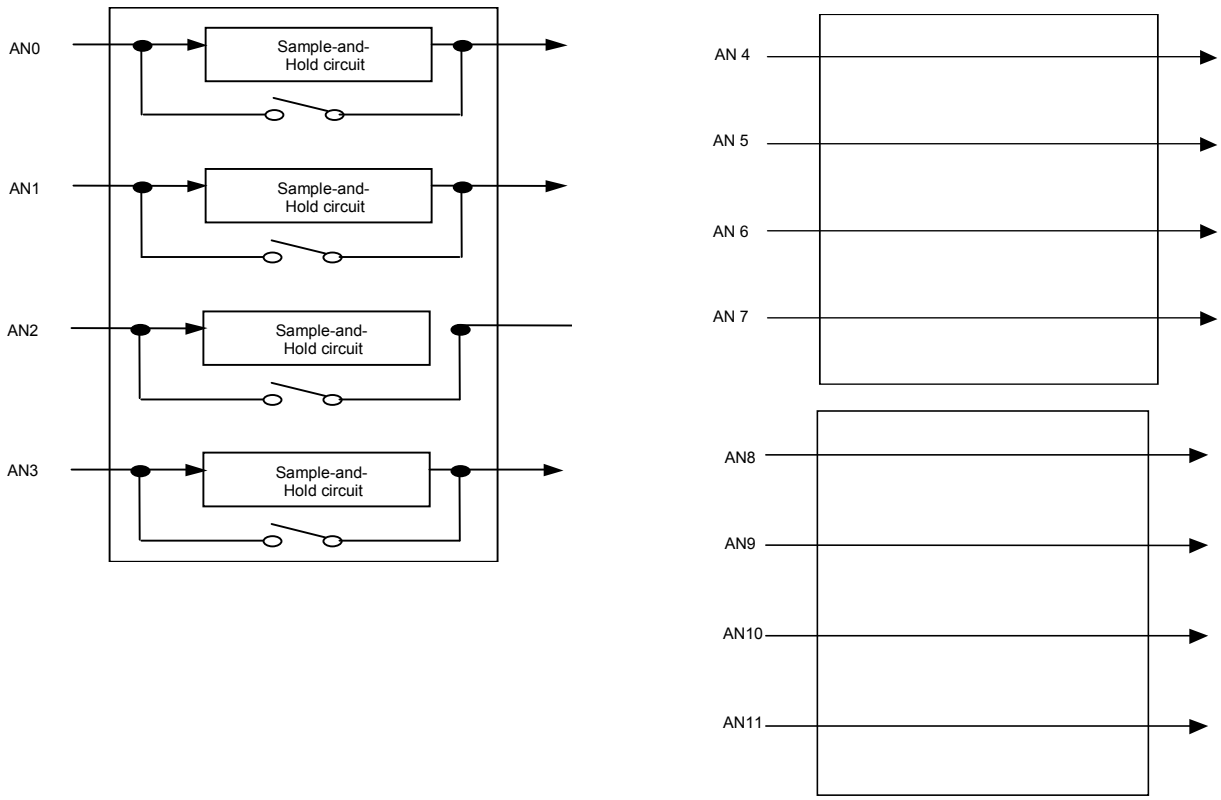
Section 20 A/D Converter Serial Communication Interface (SCI)

- The following amendments have been made to the figure 20.1, Block Diagram of A/D Converter on page 973 in section 20, A/D Converter (ADC).

[Before change]



[After change]



- The following amendments have been made to the explanation under 20.7.5, Notes on Noise Countermeasures on page 1038 in section 20, A/D Converter (ADC).

  [Before change]

  The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the AVss.

  [After change]

  The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the AVREFVSS.

  0.1µF capacitor shown in figure 20.14 should be placed as close to the pins as possible.

Section 22 Controller Area Network (RCAN-ET)

- The following amendment has been made to the explanation under 22.3.3 RCAN-ET Control Registers, (3) Bit Configuration Register BCR0, BCR1 on page 1041 in section 22, Controller Area Network (RCAN-ET).

  BCR0 (Address = H'006)

  [Before change]

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BPR[7:0]	00000000	R/W	Baud Rate Pre-scale These bits are used to define the peripheral bus clock periods contained in a Time Quantum. 00000000 : 2 x peripheral bus clock 00000001 : 4 x peripheral bus clock 00000010 : 6 x peripheral bus clock : : 2 x (register value + 1) x peripheral bus clock 00000000 : 2 x peripheral bus clock 11111111 : 512 x peripheral bus clock

  [After change]

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BPR[7:0]	00000000	R/W	Baud Rate Pre-scale These bits are used to define the peripheral bus clock periods contained in a Time Quantum. 00000000 : 2 x peripheral bus clock 00000001 : 4 x peripheral bus clock 00000010 : 6 x peripheral bus clock : : 2 x (register value + 1) x peripheral bus clock : : 2 x peripheral bus clock 01111111 : 512 x peripheral bus clock

- The following has been added to section 22, Controller Area Network (RCAN-ET), on page 1077.

[After change]
22.9 Usage Notes

22.9.1 Module Standby Mode

Settings to run or stop the clock for the RCAN-ET module can be made in standby control register 6 (STBCR6). The initial value stops the clock for the module. Change the setting after release from module-stop mode.

22.9.2 Reset

The RCAN-ET module has a hardware reset and a software reset.

- Hardware reset

The RCAN-ET module is initialized in the hardware reset and module standby states.

- Software reset

The CAN communications function and contents of registers other than the MCR0 bit are initialized by the MCR0 bit in the master control register (MCR).

Since the IRR0 bit in the interrupt request register (IRR) becomes set through initialization at the time of a reset, clear it as indicated in the “configuration mode” section of the reset sequence.
Since regions other than message control field 1 (CONTROL1) in mailboxes are configured as RAM, they are not initialized by a reset. Accordingly, initialize all mailboxes as indicated in the “configuration mode” section of the reset sequence.

22.9.3 CAN Sleep Mode

In CAN sleep mode, supply of the clock signal within the module is largely stopped. Accordingly, do not attempt access to registers other than the MCR, GSR, IRR, and IMR during periods in CAN sleep mode.

22.9.4 Register Access

During the period where the CAN communications function within the RCAN-ET module is storing a frame received over the CAN bus in a mailbox, a wait of zero to five cycles of the peripheral bus clock is generated for access to regions of the mailboxes.

22.9.5 Interrupts

Mailbox 0 reception interrupt is capable of activating the DTC or DMAC as indicated in table 21.2. When the Mailbox 0 reception interrupt source is in use as an activation source for DTC or DMAC operation, read from message control field 0 (CONTROL0) to message control field 1 (CONTROL1) by using the block transfer mode etc. of the DTC or the transfer counter mode etc. of the DMAC.

- The following amendment has been made to the explanation under 24.1.3, Port A Port Registers H and L (PAPRH and PAPRL on page 1281 in section 24, I/O Ports.

  [Before change]

  PAPRH and PAPRL are 16-bit readable/writable registers, which always return the states of the pins regardless of the PFC setting.

  [After change]

  PAPRH and PAPRL are 16-bit readable/writable registers, which always return the states of the pins. However, when the SCIF pin function has been selected for PA8, TE = 0 in SCSCR, and SPBIO = 0 in SCSPTR, the states of the corresponding pins cannot be read out.

- The following amendment has been made to the explanation under 24.4.3, Port D Port Registers H and L (PDPRH and PDPRL on page 1310 in section 24, Port A Port Registers H and L.

  [Before change]

  PDPRH and PDPRL are 16-bit read-only registers, which always return the states of the pins regardless of the PFC setting.

  [After change]

  PDPRH and PDPRL are 16-bit read-only registers, which always return the states of the pins. However, when the SCIF pin function has been selected for PD18, TE = 0 in SCSCR, and SPBIO = 0 in SCSPTR, the states of the corresponding pins cannot be read out.

Section 31 Electrical Characteristics

- The following amendments have been made to the explanation under 31.1, Absolute Maximum on page 1591 in section 31, Electrical Characteristics.

  [Before change]

Item	Symbol	Value	Unit
Power supply voltage	D_rV_{cc}	– 0.3 to + 4.3	V

  [After change]

Item	Symbol	Value	Unit
Power supply voltage	D_rV_{cc}	– 0.2 to + 7.0	V

- The following has been added to the notes for table 31.10 under 31.3.6, MTU2, MTU2S Module Timing on page 1635 in section 31, Electrical Characteristics.

  [Before change]

  Note: t_{pcyc} indicates peripheral clock (Pϕ) cycle.

  [After change]

  Note: t_{pcyc} indicates the period of the peripheral clock (Pϕ) except in the case of the MTU2S module, where it indicates the period of the MTU2S clock (Mϕ).