To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-SH7-A729A/E	Rev.	1.00
Title	Correction of errors in the SH7280 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7280 Group SH7243 Group	Lot No. All lots	Reference Document	SH7280 Group Hardware Manual Rev1.00 REJ09B0393-0100		

We would like to inform you of the corrections in the above listed hardware manuals.

Please refer to the following for details.

<Addition and corrections>

Section 1 Overview

- The following has been added to the specification of bus state controller (BSC) in table 1.1, SH7286, SH7285, and SH7243 Features.

  [After change]

  SRAM, SRAM with byte selection, SDRAM and burst ROM (clock synchronous or asynchronous) can be directly connected by specifying memories connecting to each area. Furthermore, address/data multiplexed I/O (MPX) interface is supported.

  Specification of power supply voltage in table 1.1, SH7286, SH7285, and SH7243 Features, has been revised as follows.

  [Before change]

  VCC: 3.0 to 3.6 V or 4.5 to 5.5 V, AVCC: 4.5 to 5.5 V

  [After change]

  VCC : 3.0 to 5.5 V, AVCC: 4.5 to 5.5 V

  DrVcc : 3.0 to 3.6 V (USB in use)

  : 3.0 to 5.5 V (USB not in use)

Section 3 MCU Operating Modes

- Boundary addresses between on-chip RAM (24KB) (Modes 0 and 1) and reserved area shown in figures 3.3 and 3.5 in section 3.4, Address Map have been revised as follows.

  [Before change]
  H'FFF8 7FFF
  H'FFF8 8000

  [After change]
  H'FFF8 5FFF
  H'FFF8 6000

- Boundary addresses between on-chip RAM (8KB) (Modes 0 and 1) and reserved area shown in figure 3.7 in section 3.4, Address Map have been revised as follows.

  [Before change]
  H'FFF8 2FFF
  H'FFF8 3000

  [After change]
  H'FFF8 1FFF
  H'FFF8 2000

Section 5 Exception Handling

- Table 5.6 Bus Cycles and Address Errors in section 5.3.1, Address Error Sources has been revised as follows.

[Before change]

Data read/write	CPU, DMAC, or DTC	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	None (normal)
		External memory space accessed when in single chip mode	Address error occurs

[After change]

Data read/write	CPU, DMAC, or DTC	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Double-longword data accessed from a double-longword boundary	None (normal)
		Double-longword accessed from other than a double-long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	None (normal)
		External memory space accessed when in single chip mode	Address error occurs

Section 6 Interrupt Controller (INTC)

- Table 6.2 Register Configuration in section 6.3, Register Descriptions has been revised as follows.

[Before change]

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Interrupt control register 0	ICR0	R/W	*1	H'FFFE0800	16, 32
Interrupt control register 1	ICR1	R/W	H'0000	H'FFFE0802	16, 32
IRQ interrupt request register	IRQRR	R/(W)*2	H'0000	H'FFFE0806	16, 32
Bank control register	IBCR	R/W	H'0000	H'FFFE080C	16, 32
Bank number register	IBNR	R/W	H'0000	H'FFFE080E	16, 32
Interrupt priority register 01	IPR01	R/W	H'0000	H'FFFE0818	16, 32
Interrupt priority register 02	IPR02	R/W	H'0000	H'FFFE081A	16, 32
Interrupt priority register 05	IPR05	R/W	H'0000	H'FFFE0820	16, 32
Interrupt priority register 06	IPR06	R/W	H'0000	H'FFFE0C00	16, 32
Interrupt priority register 07	IPR07	R/W	H'0000	H'FFFE0C02	16, 32
Interrupt priority register 08	IPR08	R/W	H'0000	H'FFFE0C04	16, 32
Interrupt priority register 09	IPR09	R/W	H'0000	H'FFFE0C06	16, 32
Interrupt priority register 10	IPR10	R/W	H'0000	H'FFFE0C08	16, 32
Interrupt priority register 11	IPR11	R/W	H'0000	H'FFFE0C0A	16, 32
Interrupt priority register 12	IPR12	R/W	H'0000	H'FFFE0C0C	16, 32
Interrupt priority register 13	IPR13	R/W	H'0000	H'FFFE0C0E	16, 32
Interrupt priority register 14	IPR14	R/W	H'0000	H'FFFE0C10	16, 32
Interrupt priority register 15	IPR15	R/W	H'0000	H'FFFE0C12	16, 32
Interrupt priority register 16	IPR16	R/W	H'0000	H'FFFE0C14	16, 32
Interrupt priority register 17	IPR17	R/W	H'0000	H'FFFE0C16	16, 32
Interrupt priority register 18	IPR18	R/W	H'0000	H'FFFE0C18	16, 32
USB-DTC transfer interrupt	USDTENDRR	R/(W)*2	H'0000	H'FFFE0C50	16, 32

[After change]

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Interrupt control register 0	ICR0	R/W	*1	H'FFFE0800	16, 32
Interrupt control register 1	ICR1	R/W	H'0000	H'FFFE0802	16
IRQ interrupt request register	IRQRR	R/(W)*2	H'0000	H'FFFE0806	16
Bank control register	IBCR	R/W	H'0000	H'FFFE080C	16, 32
Bank number register	IBNR	R/W	H'0000	H'FFFE080E	16
Interrupt priority register 01	IPR01	R/W	H'0000	H'FFFE0818	16, 32
Interrupt priority register 02	IPR02	R/W	H'0000	H'FFFE081A	16
Interrupt priority register 05	IPR05	R/W	H'0000	H'FFFE0820	16
Interrupt priority register 06	IPR06	R/W	H'0000	H'FFFE0C00	16, 32
Interrupt priority register 07	IPR07	R/W	H'0000	H'FFFE0C02	16
Interrupt priority register 08	IPR08	R/W	H'0000	H'FFFE0C04	16, 32
Interrupt priority register 09	IPR09	R/W	H'0000	H'FFFE0C06	16
Interrupt priority register 10	IPR10	R/W	H'0000	H'FFFE0C08	16, 32
Interrupt priority register 11	IPR11	R/W	H'0000	H'FFFE0C0A	16
Interrupt priority register 12	IPR12	R/W	H'0000	H'FFFE0C0C	16, 32
Interrupt priority register 13	IPR13	R/W	H'0000	H'FFFE0C0E	16
Interrupt priority register 14	IPR14	R/W	H'0000	H'FFFE0C10	16, 32
Interrupt priority register 15	IPR15	R/W	H'0000	H'FFFE0C12	16
Interrupt priority register 16	IPR16	R/W	H'0000	H'FFFE0C14	16, 32
Interrupt priority register 17	IPR17	R/W	H'0000	H'FFFE0C16	16
Interrupt priority register 18	IPR18	R/W	H'0000	H'FFFE0C18	16
USB-DTC transfer interrupt	USDTENDRR	R/(W)*2	H'0000	H'FFFE0C50	16

- Table 6.3 Interrupt Request Sources and IPR01, IPR02, and IPR05 to IPR18 in section 6.3.1, Interrupt Priority Registers 01, 02, 05 to 18 (IPR01, IPR02, IPR05 to IPR18) has been revised as follows.

[Before change]

Register Name	Bit			
	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
Interrupt priority register 01	IRQ0	IRQ1	IRQ2	IRQ3
Interrupt priority register 02	IRQ4	IRQ5	IRQ6	IRQ7
Interrupt priority register 05	Reserved	Reserved	ADI0	ADI1
Interrupt priority register 06	DMAC0	DMAC1	DMAC2	DMAC3
Interrupt priority register 07	DMAC4	DMAC5	DMAC6	DMAC7
Interrupt priority register 08	CMT0	CMT1	BSC	WDT
Interrupt priority register 09	MTU0 (TGI0A to TGI0D)	MTU0 (TCI0V, TGI0E, TGI0F)	MTU1 (TGI1A, TGI1B)	MTU1 (TCI1V, TCI1U)
Interrupt priority register 10	MTU2 (TGI2A, TGI2B)	MTU2 (TCI2V, TCI2U)	MTU3 (TGI3A to TGI3D)	MTU3 (TCI3V)
Interrupt priority register 11	MTU4 (TGI4A to TGI4D)	MTU4 (TCI4V)	MTU5 (TGI5U, TGI5V, TGI5W)	POE2 (OEI1, OEI2)
Interrupt priority register 12	MTU3S (TGI3A to TGI3D)	MTU3S (TCI3V)	MTU4S (TGI4A to TGI4D)	MTU4S (TCI4V)
Interrupt priority register 13	MTU5S (TGI5U, TGI5V, TGI5W)	POE2 (OEI3)	IIC3[*1]	Reserved
Interrupt priority register 14	Reserved	Reserved	Reserved	SCIF3
Interrupt priority register 15	Reserved	Reserved	Reserved	Reserved
Interrupt priority register 16	SCI0	SCI1[*1]	SCI2	Reserved
Interrupt priority register 17	SSU[*1]	SCI4[*1]	ADI2[*2]	Reserved
Interrupt priority register 18	USB[*1]	RCAN[*2]	EP1-FIFO full DTC transfer end[*1]	EP2-FIFO empty DTC transfer end[*1]

[After change]

Register Name	Bit			
	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
Interrupt priority register 01	IRQ0	IRQ1	IRQ2	IRQ3
Interrupt priority register 02	IRQ4	IRQ5	IRQ6	IRQ7
Interrupt priority register 05	Reserved	Reserved	ADI0	ADI1
Interrupt priority register 06	DMAC0	DMAC1	DMAC2	DMAC3
Interrupt priority register 07	DMAC4	DMAC5	DMAC6	DMAC7
Interrupt priority register 08	CMI0	CMI1	BSC	WDT
Interrupt priority register 09	MTU2_0 (TGIA_0 to TGID_0)	MTU2_0 (TCIV_0, TGIE_0, TGIF_0)	MTU2_1 (TGIA_1, TGIB_1)	MTU2_1 (TCIV_1, TCIU_1)
Interrupt priority register 10	MTU2_2 (TGIA2, TGIB_2)	MTU2_2 (TCIV_2, TCIU_2)	MTU2_3 (TGIA_3 to TGID_3)	MTU2_3 (TCIV_3)
Interrupt priority register 11	MTU2_4 (TGIA_4 to TGID_4)	MTU2_4 (TCIV_4)	MTU2__5 (TGIU_5, TGIV_5, TGIW_5)	POE2 (OEI1, OEI2)
Interrupt priority register 12	MTU2S_3 (TGIA_3 to TGID_3)	MTU2S_3 (TCIV_3)	MTU2S_4 (TGIA_4 to TGID_4)	MTU2S_4 (TCIV_4)
Interrupt priority register 13	MTU2S_5 (TGIU_5, TGIV_5, TGIW_5)	POE2 (OEI3)	IIC3[*1]	Reserved
Interrupt priority register 14	Reserved	Reserved	Reserved	SCIF3
Interrupt priority register 15	Reserved	Reserved	Reserved	Reserved
Interrupt priority register 16	SCI0	SCI1[*1]	SCI2	Reserved
Interrupt priority register 17	SSU[*1]	SCI4[*1]	ADI2[*2]	Reserved
Interrupt priority register 18	USB[*1] (USI0, USI1)	RCAN_ET[*2]	EP1-FIFO full DTC transfer end[*1] (USBRXI)	EP2-FIFO empty DTC transfer end[*1] (USBTX1)

- Table 6.4, Interrupt Exception Handling Vectors and Priorities in section 6.5, Interrupt Exception Handling Vector Table and Priority, has been revised as follows.

  [Before change]

USB	EP1-FIFO full DTC transfer end	
	EP2-FIFO empty DTC transfer end	
MTU2	MTU0	TGIA_0
		TGIB_0
		TGIC_0
		TGID_0
		TCIV_0
		TGIE_0
		TGIF_0
	MTU1	TGIA_1
		TGIB_1
		TCIV_1
		TCIU_1
	MTU2	TGIA_2
		TGIB_2
		TCIV_2
		TCIU_2
	MTU3	TGIA_3
		TGIB_3
		TGIC_3
		TGID_3
		TCIV_3
	MTU4	TGIA_4
		TGIB_4
		TGIC_4
		TGID_4
		TCIV_4
	MTU5	TGIU_5
		TGIV_5
		TGIW_5

MTU2S	MTU3S	TGIA_3
		TGIB_3
		TGIC_3
		TGID_3
		TCIV_3
	MTU4S	TGIA_4
		TGIB_4
		TGIC_4
		TGID_4
		TCIV_4
	MTU5S	TGIU_5
		TGIV_5
		TGIW_5

[After change]

USB	EP1-FIFO full DTC transfer end (USBRXI)	
	EP2-FIFO empty DTC transfer end (USBTXI)	
MTU2	MTU2_0	TGIA_0
		TGIB_0
		TGIC_0
		TGID_0
		TCIV_0
		TGIE_0
		TGIF_0
	MTU2_1	TGIA_1
		TGIB_1
		TCIV_1
		TCIU_1
	MTU2_2	TGIA_2
		TGIB_2
		TCIV_2
		TCIU_2
	MTU2_3	TGIA_3
		TGIB_3
		TGIC_3
		TGID_3
		TCIV_3
	MTU2_4	TGIA_4
		TGIB_4
		TGIC_4
		TGID_4
		TCIV_4
	MTU2_5	TGIU_5
		TGIV_5
		TGIW_5

MTU2S	MTU2S_3	TGIA_3S
		TGIB_3S
		TGIC_3S
		TGID_3S
		TCIV_3S
MTU2S	MTU2S_4	TGIA_4S
		TGIB_4S
		TGIC_4S
		TGID_4S
		TCIV_4S
	MTU2S_5	TGIU_5S
		TGIV_5S
		TGIW_5S

- The following has been added to section 6.10, Usage Note.

  [After change]

  6.10.2 When NMI is not in Use

  When NMI is not in use, the pin should be fixed to high with the resistance connected to Vcc.

Section 7 User Break Controller (UBC)

- The following paragraphs have been added to section 7.5, Usage Note.

  [After change]

  9. Do not set a pre-execution break at an instruction that follows DIVU or DIVS. If a break is set at the instruction after DIVU or DIVS, an interrupt or exception during the execution of DIVU or DIVS will cause suspension of the DIVU or DIVS instruction, but the pre-execution break for the next instruction will still occur.
  10. Do not set a pre-execution and post-execution break at the same address. For example, if a pre-execution break on channel_0 and a post-execution break on channel_1 are set for the same address, the pre-execution break on channel 0 will cause the match flag for the condition for the post-execution break on channel 1 to be set.

Section 8 Data Transfer Controller (DTC)

- Note in section 8 has been revised as follows.

  [Before change]

  Note: When the transfer information is stored in the on-chip RAM, the RAME bit in RAMCR must be set to 1.

  [After change]

  Note: When the transfer information is stored in the on-chip RAM, the RAME bit in SYSCR1 must be set to 1.

- Table 8.2 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs in section 8, Data Transfer Controller (DTC), has been revised as follows.

[Before change]

Origin of activation Source	Origin of Activation Source
:	:
RCAN	RM0_0
:	:
USB	USRDTCEND
	USTDTCEND
:	:
MTU2S_CH3	TGISA_3
	TGISB_3
	TGISC_3
	TGISD_3
MTU2S_CH4	TGISA_4
	TGISB_4
	TGISC_4
	TGISD_4
	TCISV_4
MTU2S_CH5	TGISU_5
	TGISV_5
	TGISW_5

[After change]

Origin of Activation Source	Origin of Activation Source
:	:
RCAN_ET	RM0_0
:	:
USB	EP1 FIFO FULL as DTC activation source (USBRXI)
	EP2 FIFO EMPTY as DTC activation source (USBTXI)
:	:
MTU2S_CH3	TGISA_3S
	TGISB_3S
	TGISC_3S
	TGISD_3S
MTU2S_CH4	TGISA_4S
	TGISB_4S
	TGISC_4S
	TGISD_4S
	TCISV_4S
MTU2S_CH5	TGISU_5S
	TGISV_5S
	TGISW_5S

Section 10 Direct Memory Access Controller (DMAC)

- Section 10.3.9, DMA Extension Resource Selectors 0 to 3 (DMARS0 to DMARS3), has been revised as follows.

[Before change]

DMARS can specify transfer requests from eight SCIF sources, two IIC3 sources, two A/D sources, five MTU2 sources and two CMT sources.

[After change]

DMARS can specify transfer requests from among two SCIF sources, two IIC3 sources, one A/D source, five MTU2 sources, two CMT sources, two USB sources, one RCAN_ET source and two SSU sources.

- Table 10.4, DMARS Settings in section10.3.9, DMA Extension Resource Selectors 0 to 3 (DMARS0 to DMARS3), has been revised as follows.

[Before change]

Peripheral Module	
USB	EP1FIFO
	EP2FIFO
RCAN	RM0_0
SSU	SSTXI
	SSRXI
SCIF_3	TXI3
	RXI3
IIC3	TXI
	RXI
A/D converter_0	ADI0
MTU2_0	TGI0A
MTU2_1	TGI1A
MTU2_2	TGI2A
MTU2_3	TGI3A
MTU2_4	TGI4A
CMT_0	CMT_0
CMT_1	CMT_1

[After change]

Peripheral Module	
USB	USBRXI
	USBTXI
RCAN_ET	RM0_0
SSU	SSTXI
	SSRXI
SCIF_3	TXI3
	RXI3
IIC3	TXI
	RXI
A/D converter_0	ADI0
MTU2_0	TGIA_0
MTU2_1	TGI A_1
MTU2_2	TGI A_2
MTU2_3	TGI A_3
MTU2_4	TGI A_4
CMT_0	CMI0
CMT_1	CMI1

- Table 10.8, Selecting On-Chip Peripheral Module Request Modes with RS3 to RS0 Bits, has been revised as follows.

[Before change]

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode
RS[3:0]	MID	RID					
1000	100000	01	USB receive	EP1 FIFO full transfer request	USBEPDR1	Any	Cycle steal
		10	USB transmit	EP2 FIFO empty transfer request	Any	USBEPDR2	
	100001	10	RCAN	RM0 (RCAN receive interrupt)	MB0 to MB31	Any	Cycle steal
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	111000	11	MTU2_0	TGI0A	Any	Any	Cycle steal or burst
	111001	11	MTU2_1	TGI1A	Any	Any	
	111010	11	MTU2_2	TGI2A	Any	Any	
	111011	11	MTU2_3	TGI3A	Any	Any	
	111100	11	MTU2_4	TGI4A	Any	Any	
	111110	11	CMT_0	Compare match 0	Any	Any	Cycle steal or burst
	111111	11	CMT_1	Compare match 1	Any	Any	

[After change]

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode
RS[3:0]	MID	RID					
1000	100000	01	USB receive	EP1 FIFO full transfer request (USBRXI)	USBEPDR1	Any	Cycle steal
		10	USB transmit	EP2 FIFO empty transfer request (USBTXI)	Any	USBEPDR2	
	100001	10	RCAN_ET	RM0 (RCAN_ET receive interrupt)	MB0 to MB31	Any	Cycle steal
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	111000	11	MTU2_0	TGIA_0	Any	Any	Cycle steal or burst
	111001	11	MTU2_1	TGIA_1	Any	Any	
	111010	11	MTU2_2	TGIA_2	Any	Any	
	111011	11	MTU2_3	TGIA_3	Any	Any	
	111100	11	MTU2_4	TGIA_4	Any	Any	
	111110	11	CMT_0	Compare match transfer request 0	Any	Any	Cycle steal or burst
	111111	11	CMT_1	Compare match transfer request 1	Any	Any	

Section 11 Multi-Function Timer Pulse Unit 2 (MTU2)

- Section 11.3.9, Timer Synchronous Clear Register (TSYCR), has been revised as follows.

  [Before change]

  Section 11.3.9 Timer Synchronous Clear Register (TSYCR)

  TSYCR is an 8-bit readable/writable register that specifies conditions for clearing TCNT_3 and TCNT_4 in the MTU2S in synchronization with the MTU2. The MTU2S has one TSYCR in channel 3 but the MTU2 has no TSYCR.

  [After change]

  Section 11.3.9 Timer Synchronous Clear Register S (TSYCRS)

  TSYCRS is an 8-bit readable/writable register that specifies conditions for clearing TCNT_3 and TCNT_4 in the MTU2S in synchronization with the MTU2. The MTU2S has one TSYCRS in channel 3 but the MTU2 has no TSYCRS.

- Note has been added to section 11.3.23, Time Gate Control Register (TGCR) as follows.

  [After change]

  Do not set the FB bit to 0 when the BDC bit is set to 1 in MTU2S.

- Section 11.4.10, MTU2-MTU2S Synchronous Operation, has been revised as follows.

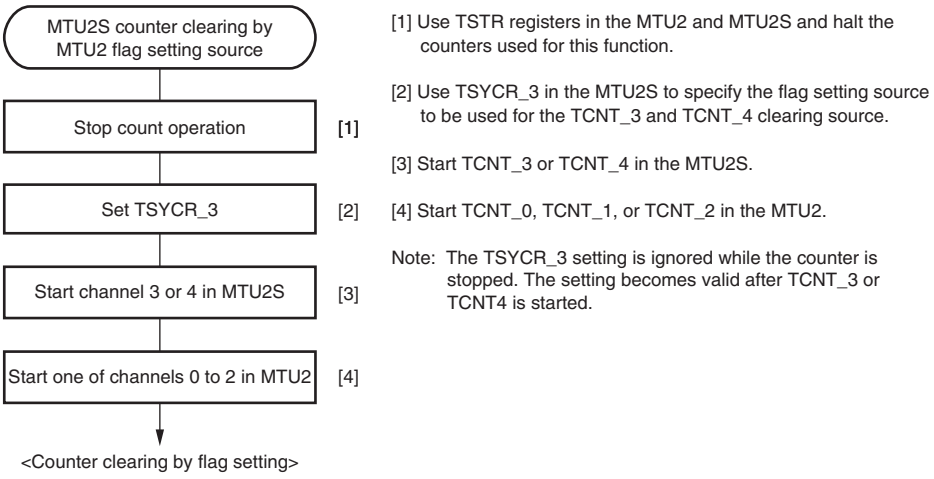
  [Before change]

  (2) MTU2S Counter Clearing Caused by MTU2 Flag Setting Source (MTU2-MTU2S Synchronous Counter Clearing)

  The MTU2S counters can be cleared by sources for setting the flags in TSR_0 to TSR_2 in the MTU2 through the TSYCR_3 settings in the MTU2S.

  (a) Example of Procedure for Specifying MTU2S Counter Clearing by MTU2 Flag Setting Source

  Figure 11.85 shows an example of procedure for specifying MTU2S counter clearing by MTU2 flag setting source.



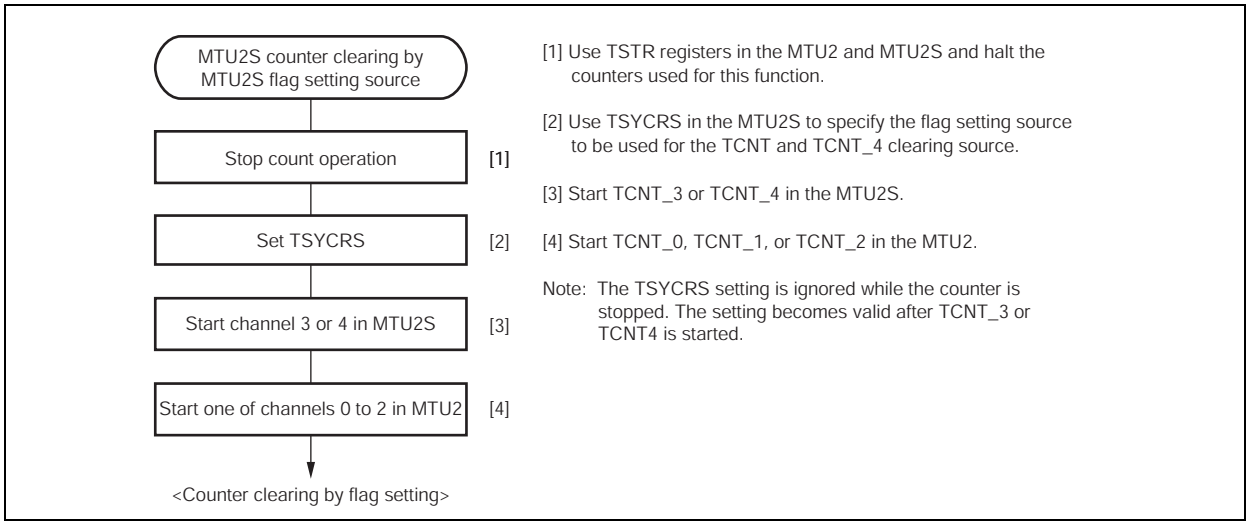
[After change]

(2) MTU2S Counter Clearing Caused by MTU2 Flag Setting Source (MTU2-MTU2S Synchronous Counter Clearing)

The MTU2S counters can be cleared by sources for setting the flags in TSR_0 to TSR_2 in the MTU2 through the TSYCRS settings in the MTU2S.

(a) Example of Procedure for Specifying MTU2S Counter Clearing by MTU2 Flag Setting Source

Figure 11.85 shows an example of procedure for specifying MTU2S counter clearing by MTU2 flag setting source.



Section 12 Multi-Function Timer Pulse Unit 2S (MTU2S)

- Table 12.3 Register Configuration in section 12.2, Register Descriptions, has been revised as follows.

[Before change]

Timer synchronous clear register S	TSYCRS	R/W	H'00	H'FFFE4A50	8

[After change]

Timer synchronous clear register S*1	TSYCRS	R/W	H'00	H'FFFE4A50	8

*1 For details on registers, refer to section 11.3.9, Timer Synchronous Clear Register (TSYCR) and figure 11.85 in section 11, Multi-Function Timer Pulse Unit 2 (MTU2).

Section 13 Port Output Enable 2 (POE2)

- Table 13.1, Pin Configuration in section 13.2, Input/Output Pins has been revised as follows.

[Before change]

Pin Name	Symbol	I/O	Function
Port output enable input pins 0 to 3	$\overline{\text{POE0}}$ to $\overline{\text{POE3}}$	Input	Input request signals to place high-current pins (PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B, PE14/TIOC4C, and PE15/TIOC4D) for MTU2 in high-impedance state
Port output enable input pins 4 to 7	$\overline{\text{POE4}}$ to $\overline{\text{POE7}}$	Input	Input request signals to place high-current pins (PE5/TIOC3BS, PE6/TIOC3DS, PE0/TIOC4AS, PE1/TIOC4BS, PE2/TIOC4CS, PE3/TIOC4DS, PD10/TIOC3BS, PD11/TIOC3DS, PD12/TIOC4AS, PD13/TIOC4BS, PD14/TIOC4CS, PD15/TIOC4DS, PD29/TIOC3BS, PD28/TIOC3DS, PD27/TIOC4AS, PD26/TIOC4BS, PD25/TIOC4CS, and PD24/TIOC4DS) for MTU2S in high-impedance state
Port output enable input pin 8	$\overline{\text{POE8}}$	Input	Inputs a request signal to place pins (PE0/TIOC0A, PE1/TIOC0B, PE2/TIOC0C, and PA3/TIOC0D) for channel 0 in MTU2 in high-impedance state

[After change]

Pin Name	Symbol	I/O	Function
Port output enable input pins 0 to 3	POE0 to POE3	Input	Input request signals to place high-current pins (PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B, PE14/TIOC4C, and PE15/TIOC4D) for MTU2 in high-impedance state
Port output enable input pins 4 to 7	POE4 to POE7	Input	Input request signals to place high-current pins (PE5/TIOC3BS, PE6/TIOC3DS, PE0/TIOC4AS, PE1/TIOC4BS, PE2/TIOC4CS, PE3/TIOC4DS, PD10/TIOC3BS, PD11/TIOC3DS, PD12/TIOC4AS, PD13/TIOC4BS, PD14/TIOC4CS, PD15/TIOC4DS, PD29/TIOC3BS, PD28/TIOC3DS, PD27/TIOC4AS, PD26/TIOC4BS, PD25/TIOC4CS, and PD24/TIOC4DS) for MTU2S in high-impedance state
Port output enable input pin 8	POE8	Input	Inputs a request signal to place pins (PE0/TIOC0A, PE1/TIOC0B, PE2/TIOC0C, and PE3/TIOC0D) for channel 0 in MTU2 in high-impedance state

Section 15 Watchdog Timer (WDT)

- The following has been added to section 15.5, Usage Note.

  [After change]

  15.5.5 $\overline{\text{WDTOVF}}$ Signal

  Leave the pin open when $\overline{\text{WDTOVF}}$ not in use. Do not pull down $\overline{\text{WDTOVF}}$.

  If pulling-down is required, use a resistance of 1MΩ or more.

Section 16 Serial Communication Interface (SCI)

- The following has been added to section 16.3.8, Serial Port Register (SCSPTR).

[Before change]

Bit:	7	6	5	4	3	2	1	0
	EIO	-	-	-	SPB1IO	SPB1DT	-	SPB0DT
Initial value:	0	0	0	0	0	-	0	1
R/W:	R/W	-	-	-	R/W	R/W	-	W

Bit	Bit Name	Initial Value	R/W	Description
:	:	:	:	:
2	SPB1DT	Undefined	R/W	Clock Port Data in Serial Port Specifies the data output through the SCK pin in the serial port. Output should be enabled by the SPB1IO bit (for details, refer to the SPB1IO bit description). When output is enabled, the SPB1DT bit value is output through the SCK pin. 0: Low level is output 1: High level is output
:	:	:	:	:

[After change]

Bit:	7	6	5	4	3	2	1	0
	EIO	-	-	-	SPB1IO	SPB1DT	-	SPB0DT
Initial value:	0	0	0	0	0	-	0	1
R/W:	R/W	-	-	-	R/W	W	-	W

Bit	Bit Name	Initial Value	R/W	Description
:	:	:	:	:
2	SPB1DT	Undefined	W	Clock Port Data in Serial Port Specifies the data output through the SCK pin in the serial port. Output should be enabled by the SPB1IO bit (for details, refer to the SPB1IO bit description). When output is enabled, the SPB1DT bit value is output through the SCK pin. 0: Low level is output 1: High level is output
:	:	:	:	:

- The following has been added to (2) of section 16.4.3, Clock Synchronous Mode.

[After change]

However, in the case of reception only, output of the clock signal will continue until an overrun error occurs or the RE bit is cleared to 0. If reception operation for n characters of data is to proceed, select an external clock as the clock source. If an internal clock has to be used, set RE = 1 and TE = 1, and then transmit n characters of dummy data while receiving the n characters of data for reception.

Section 17 Serial Communication Interface with FIFO (SCIF)

- Table 17.2, Register Configuration in section 17.3, Register Descriptions, has been revised as follows.

[Before change]

Channel	Register Name	Abbreviation	R/W	Initial Value Address	Address	Access Size
3	:	:	:	:	:	:
	Serial port register_3	SCSPTR_3	R/W	H'0050	H'FFFE9820	16
	:	:	:	:	:	:

[After change]

Channel	Register Name	Abbreviation	R/W	Initial Value Address	Address	Access Size
3	:	:	:	:	:	:
	Serial port register_3	SCSPTR_3	R/W	H'00xx	H'FFFE9820	16
	:	:	:	:	:	:

- Section 17.3.11, Serial Port Register (SCSPTR), has been revised as follows:

[Before change]

The CPU can always read and write to SCSPTR. SCSPTR is initialized to H'0050 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	SCKIO	SCKDT	SPB2IO	SPB2DT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
:	:	:	:	:
2	SCKDT	0	R/W	SCK Port Data Indicates the input/output data of the serial port SCK pin. Input/output is specified by the SCKIO bit. For output, the SCKDT bit value is output to the SCK pin. The SCK pin status is read from the SCKDT bit regardless of the SCKIO bit setting. However, SCK input/output must be set in the PFC. 0: Input/output data is low level 1: Input/output data is high level
:	:	:	:	:
0	SPB2DT	0	R/W	Serial Port Break Data Indicates the input data of the RXD pin and the outputdata of the TXD pin used as serial ports. Input/output is specified by the SPB2IO bit. When the TXD pin is set to output, the SPB2DT bit value is output to the TXD pin. The RXD pin status is read from the SPB2DT bit regardless of the SPB2IO bit setting. However, RXD input and TXD output must be set in the PFC. 0: Input/output data is low level 1: Input/output data is high level

[After change]

The CPU can always read and write to SCSPTR. SCSPTR is initialized to H'00xx by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	SCKIO	SCKDT	SPB2IO	SPB2DT
Initial value:	0	0	0	0	0	0	0	0	0	—	0	—	0	—	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	W	R/W	W

Bit	Bit Name	Initial Value	R/W	Description
:	:	:	:	:
2	SCKDT	Undefined	W	SCK Port Data Indicates the input/output data of the serial port SCK pin. Input/output is specified by the SCKIO bit. For output, the SCKDT bit value is output to the SCK pin. The SCK pin status is read from the SCKDT bit regardless of the SCKIO bit setting. However, SCK input/output must be set in the PFC. 0: Input/output data is low level 1: Input/output data is high level
:	:	:	:	:
0	SPB2DT	Undefined	W	Serial Port Break Data Indicates the input data of the RXD pin and the output data of the TXD pin used as serial ports. Input/output is specified by the SPB2IO bit. When the TXD pin is set to output, the SPB2DT bit value is output to the TXD pin. The RXD pin status is read from the SPB2DT bit regardless of the SPB2IO bit setting. However, RXD input and TXD output must be set in the PFC. 0: Input/output data is low level 1: Input/output data is high level

- Description (1) in figure 17.11, Sample of Flowchart for Transmitting Serial Data, has been revised as follows.

[Before change]

(1) SCIF status check and transmit data write:

Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR. Read 1from the TDFE and TEND flags, then clear these flags to 0.

[After change]

(1) SCIF status check and transmit data write:

Read SCFSR and check that the TDFE and TEND flags are set to 1, then write transmit data to SCFTDR. Read 1from the TDFE and TEND flags, then clear these flags to 0.

- Description (1) in figure 17.16, Sample Flowchart for Transmitting/Receiving Serial Data, has been revised as follows.

[Before change]

(1) SCIF status check and transmit data write:

Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR. Read 1 from the TDFE and TEND flags, then clear these flags to 0. The transition of the TDFE flag from 0 to 1 can also be identified by a TXI interrupt.

[After change]

(1) SCIF status check and transmit data write:

Read SCFSR and check that the TDFE and TEND flags are set to 1, then write transmit data to SCFTDR and clear the TDFE and TEND flags to 0. The transition of the TDFE flag from 0 to 1 can also be identified by a TXI interrupt.

Section 18 Synchronous Serial Communication Unit (SSU)

- Table 18.6, Communication Modes and Pin States of SSCK Pin, has been revised as follows.

[Before change]

Communication Mode	Register Setting			Pin State
	SSUMS	MSS	SCKS	SSCK
SSU communication mode	0	0	0	—
			1	Input
		1	0	—
			1	Output
Clock synchronous communication mode	1	0	0	—
			1	Input
		1	0	—
			1	Output

[After change]

Communication Mode	Register Setting		Pin State
	SSUMS	MSS	SSCK
SSU communication mode	0	0	—
			Input
		1	—
			Output
Clock synchronous communication mode	1	0	—
			Input
		1	—
			Output

Section 20 A/D Converter (ADC)

- Section 20.3.1, A/D Control Registers 0 to 2 (ADCR_0 to ADCR_2), has been revised as follows.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
7	ADST	0	R/W	A/D Start When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. When this bit is set to 1, A/D conversion is started. In single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by software, a reset, or in software standby mode or module standby mode.
:	:	:	:	:

[After change]

Bit	Bit Name	Initial Value	R/W	Description
7	ADST	0	R/W	A/D Start When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. When this bit is set to 1, A/D conversion is started. In single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by software, a reset, or in software standby mode.
:	:	:	:	:

Section 24 I/O Ports

- The following has been added to section 24, I/O Ports.

[After change]

24.7 Usage Notes

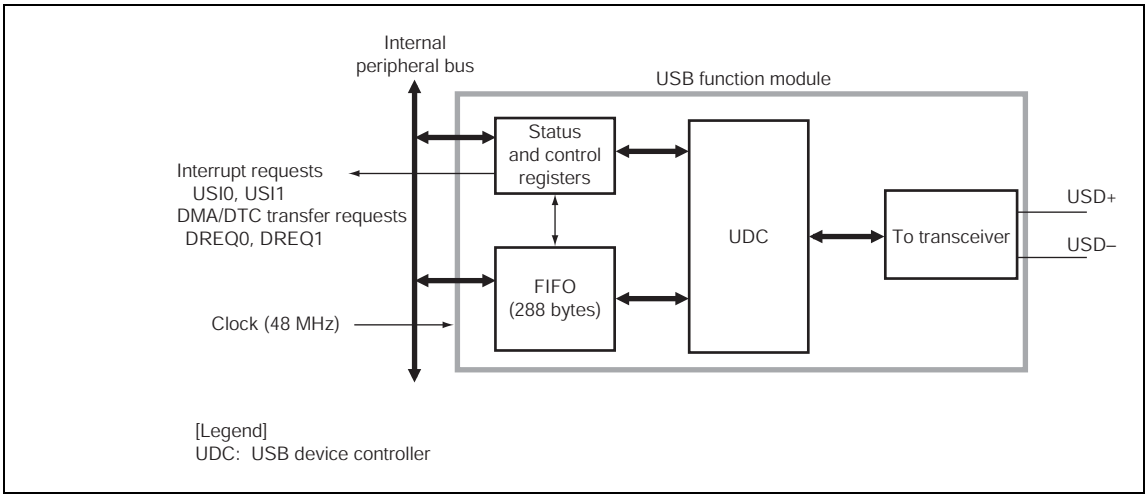
24.7.1 Handling of Unused Pins

Unused pins should be connected to Vcc or GND by resistors and fixed to the high or low level. PF0 to PF11 should be connected to Avcc or Avss by resistors. However, handling of the NMI, USD+, USD-, EXTAL, XTAL, USBXTAL, WDTOVF, TRST, TMS, TCK, TDO and TDI signals should be in accord with the descriptions for the corresponding modules.

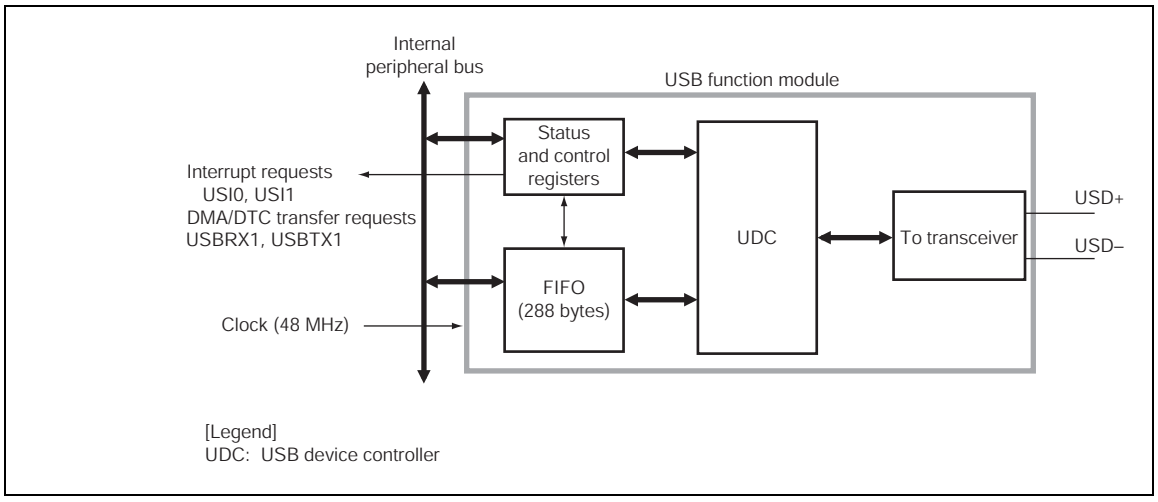
Section 25 USB Function Module

- Figure 25.1, Block Diagram of USB, has been revised as follows.

[Before change]



[After change]



- Note have been added to table 25.1, Pin Configuration and Functions, in section 25.2, Pin Configuration.

  Note: * In the case of 3.0 ≤ Vcc ≤ 3.6V, DrVcc = Vcc or 3.0 ≤ DrVcc ≤ 3.6V

  In the case of 3.6≤ Vcc ≤ 5.5V, DrVcc ≤ 3.6V < Vcc

- Notes in section 25.3.18, USBDMA Transfer Setting Register (USBDMAR), has been modified as follows.

  [Before change]

  Note: 1. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE0 bit in DTCERA to start DTC transfer.

  2. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE1 bit in DTCERA to start DTC transfer.

  [After change]

  Notes: 1. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE0 bit in DTCERA to start DTC transfer. When the DME bit in DMAOR and DTCE0 bit in DTCERA are not set, EP2-FIFO empty DTC transfer end interrupt (the TXF bit in USDTENDRR) will occur.

  2. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE1 bit in DTCERA to start DTC transfer. When the DME bit in DMAOR and DTCE1 bit in DTCERA are not set, EP1-FIFO full DTC transfer end interrupt (the RXF bit in USDTEDRR) will occur.

- Table 25.3, Interrupt Sources, has been modified as follows.

  [Before change]

Register	Bit	Transfer Type	Interrupt Source	Description	Interrupt Request Signal	DMAC/DTC Activation by USB Request
USBIFR0	7	(Status)	BRST	Bus reset	USI0 or USI1	×
	6	Bulk-OUT (EP1)	EP1FULL	EP1FIFO full	USI0 or USI1	DREQ0[*1]
	5	Bulk-IN (EP2)	EP2TR	EP2 transfer request	USI0 or USI1	×
	4		EP2EMPTY	EP2 FIFO empty	USI0 or USI1	DREQ1[*2]
	:	:	:	:	:	:
USBIFR1	:	:	:	:	:	:

  [After change]

Register	Bit	Transfer Type	Interrupt Source	Description	Interrupt Request Signal	DMAC/DTC Activation by USB Request
USBIFR0	7	(Status)	BRST	Bus reset	USI0 or USI1	×
	6	Bulk-OUT (EP1)	EP1FULL	EP1FIFO full	USI0 or USI1	USBRXI[*1]
	5	Bulk-IN (EP2)	EP2TR	EP2 transfer request	USI0 or USI1	×
	4		EP2EMPTY	EP2 FIFO empty	USI0 or USI1	USBTXI[*2]
	:	:	:	:	:	:
USBIFR1	:	:	:	:	:	:

Section 31, Electrical Characteristics

- Table 31.7, Bus Timing, has been revised as follows.

[Before change]

		Bϕ = 50 MHz*			
Item	Symbol	Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	1	20	ns	Figures 31.11 to 31.35, 31.38
Address delay time 2	t_{AD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figure 31.18
Address delay time 3	t_{AD3}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
Address setup time	t_{AS}	0	—	ns	Figures 31.11 to 31.14, 31.18
Address hold time	t_{AH}	0	—	ns	Figures 31.11 to 31.14
BS delay time	t_{BSD}	—	20	ns	Figures 31.11 to 31.32, 31.36, 31.38
CS delay time 1	t_{CSD1}	1	20	ns	Figures 31.11 to 31.35, 31.38
CS delay time 2	t_{CSD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
Read write delay time 1	t_{RWD1}	1	20	ns	Figures 31.11 to 31.35, 31.38
Read write delay time 2	t_{RWD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
Read strobe delay time	t_{RSD}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.11 to 31.15, 31.17 to 31.18, 31.38
Read data setup time 1	t_{RDS1}	$1/2t_{cyc}$ + 20	—	ns	Figures 31.11 to 31.15, 31.17, 31.38
Read data setup time 2	t_{RDS2}	20	—	ns	Figures 31.16, 31.19 to 31.22, 31.27 to 31.29
Read data setup time 3	t_{RDS3}	$1/2t_{cyc}$ + 20	—	ns	Figure 31.18
Read data setup time 4	t_{RDS4}	$1/2t_{cyc}$ + 20	—	ns	Figure 31.36
Read data hold time 1	t_{RDH1}	0	—	ns	Figures 31.11 to 31.15, 31.17, 31.38
Read data hold time 2	t_{RDH2}	5	—	ns	Figures 31.16, 31.19 to 31.22, 31.27 to 31.29
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 31.18
Read data hold time 4	t_{RDH4}	$1/2t_{cyc}$ + 5	—	ns	Figure 31.36
Write enable delay time 1	t_{WED1}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.11 to 31.15, 31.38
Write enable delay time 2	t_{WED2}	—	20	ns	Figure 31.17
Write data delay time 1	t_{WDD1}	—	20	ns	Figures 31.11 to 31.17, 31.38
Write data delay time 2	t_{WDD2}	—	20	ns	Figures 31.23 to 31.26, 31.30 to 31.32
Write data delay time 3	t_{WDD3}	—	$1/2t_{cyc}$ + 20	ns	Figure 31.36

Item	Symbol	Bϕ = 50 MHz* Min.	Max.	Unit	Figure
Write data hold time 1	t_{WDH1}	1	—	ns	Figures 31.11 to 31.17, 31.38
Write data hold time 2	t_{WDH2}	1	—	ns	Figures 31.23 to 31.26, 31.30 to 31.32
Write data hold time 3	t_{WDH3}	$1/2t_{cyc}$ + 1	—	ns	Figure 31.36
WAIT setup time	t_{WTS}	$1/2t_{cyc}$ + 20	—	ns	Figures 31.12 to 31.18
WAIT hold time	t_{WTH}	$1/2t_{cyc}$ + 10	—	ns	Figures 31.12 to 31.18
RAS delay time 1	t_{RASD1}	1	20	ns	Figures 31.19 to 31.35
RAS delay time 2	t_{RASD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
CAS delay time 1	t_{CASD1}	1	20	ns	Figures 31.19 to 31.35
CAS delay time 2	t_{CASD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
DQM delay time 1	t_{DQMD1}	1	20	ns	Figures 31.19 to 31.32
DQM delay time 2	t_{DQMD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figures 31.36, 31.37
CKE delay time 1	t_{CKED1}	1	20	ns	Figure 31.34
CKE delay time 2	t_{CKED2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figure 31.37
AH delay time	t_{AHD}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 20	ns	Figure 31.15
Multiplexed address delay time	t_{MAD}	–	20	ns	Figure 31.15
Multiplexed address hold time	t_{MAH}	1	—	ns	Figure 31.15
DACK, TEND delay time	t_{DACD}	—	Refer to peripheral modules	ns	Figures 31.10 to 31.31, 31.35, 31.37
FRAME delay time	t_{FMD}	1	20	ns	Figure 31.16

[After change]

Item	Symbol	Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	1	18	ns	Figures 31.11 to 31.35
Address delay time 2	t_{AD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figure 31.18
Address delay time 3	t_{AD3}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
Address setup time	t_{AS}	0	—	ns	Figures 31.11 to 31.14, 31.18
Address hold time	t_{AH}	0	—	ns	Figures 31.11 to 31.14
BS delay time	t_{BSD}	—	18	ns	Figures 31.11 to 31.32, 31.36
CS delay time 1	t_{CSD1}	1	18	ns	Figures 31.11 to 31.35
CS delay time 2	t_{CSD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
CS setup time	t_{CSS}	0	—	ns	31.11 to 31.14
CS hold time	t_{CSH}	0	—	ns	31.11 to 31.14
Read write delay time 1	t_{RWD1}	1	18	ns	Figures 31.11 to 31.35
Read write delay time 2	t_{RWD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
Read strobe delay time	t_{RSD}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.11 to 31.38
Read data setup time 1	t_{RDS1}	$1/2t_{cyc}$ + 14	—	ns	Figures 31.11 to 31.17
Read data setup time 2	t_{RDS2}	14	—	ns	Figures 31.19 to 31.22, 31.27 to 31.29
Read data setup time 3	t_{RDS3}	$1/2t_{cyc}$ + 14	—	ns	Figure 31.18
Read data setup time 4	t_{RDS4}	$1/2t_{cyc}$ + 14	—	ns	Figure 31.36
Read data hold time 1	t_{RDH1}	0	—	ns	Figures 31.11 to 31.15, 31.17
Read data hold time 2	t_{RDH2}	2	—	ns	Figures 31.16, 31.19 to 31.22, 31.27 to 31.29
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 31.18
Read data hold time 4	t_{RDH4}	$1/2t_{cyc}$ + 5	—	ns	Figure 31.36
Write enable delay time 1	t_{WED1}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.11 to 31.15
Write enable delay time 2	t_{WED2}	—	18	ns	Figure 31.17
Write data delay time 1	t_{WDD1}	—	18	ns	Figures 31.11 to 31.17
Write data delay time 2	t_{WDD2}	—	18	ns	Figures 31.23 to 31.26, 31.30 to 31.32
Write data delay time 3	t_{WDD3}	—	$1/2t_{cyc}$ + 18	ns	Figure 31.36

		Bϕ = 50 MHz*			
Item	Symbol	Min.	Max.	Unit	Figure
Write data hold time 1	t_{WDH1}	1	15	ns	Figures 31.11 to 31.17
Write data hold time 2	t_{WDH2}	1	—	ns	Figures 31.23 to 31.26, 31.30 to 31.32
Write data hold time 3	t_{WDH3}	$1/2t_{cyc}$ + 1	—	ns	Figure 31.36
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 31.11 to 31.14
Read data access time	t_{ACC}	Tcyc x (n+1.5) -33	—	ns	Figure 31.11 to 31.14
Access time from read strobe	t_{OE}	Tcyc x (n+1) -31		ns	Figure 31.11 to 31.14
WAIT setup time	t_{WTS}	$1/2t_{cyc}$ + 18	—	ns	Figures 31.12 to 31.18
WAIT hold time	t_{WTH}	$1/2t_{cyc}$ + 2	—	ns	Figures 31.12 to 31.18
RAS delay time 1	t_{RASD1}	1	18	ns	Figures 31.19 to 31.35
RAS delay time 2	t_{RASD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
CAS delay time 1	t_{CASD1}	1	18	ns	Figures 31.19 to 31.35
CAS delay time 2	t_{CASD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
DQM delay time 1	t_{DQMD1}	1	18	ns	Figures 31.19 to 31.32
DQM delay time 2	t_{DQMD2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figures 31.36, 31.37
CKE delay time 1	t_{CKED1}	1	18	ns	Figure 31.34
CKE delay time 2	t_{CKED2}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figure 31.37
AH delay time	t_{AHD}	$1/2t_{cyc}$ + 1	$1/2t_{cyc}$ + 18	ns	Figure 31.15
Multiplexed address delay time	t_{MAD}	–	18	ns	Figure 31.15
Multiplexed address hold time	t_{MAH}	1	—	ns	Figure 31.15
DACK, TEND delay time	t_{DACD}	—	Refer to peripheral modules	ns	Figures 31.11 to 31.32, 31.36, 31.39
FRAME delay time	t_{FMD}	1	18	ns	Figure 31.16

- Figures 31.11 to 31.14 have been added as follows.

  [After change]

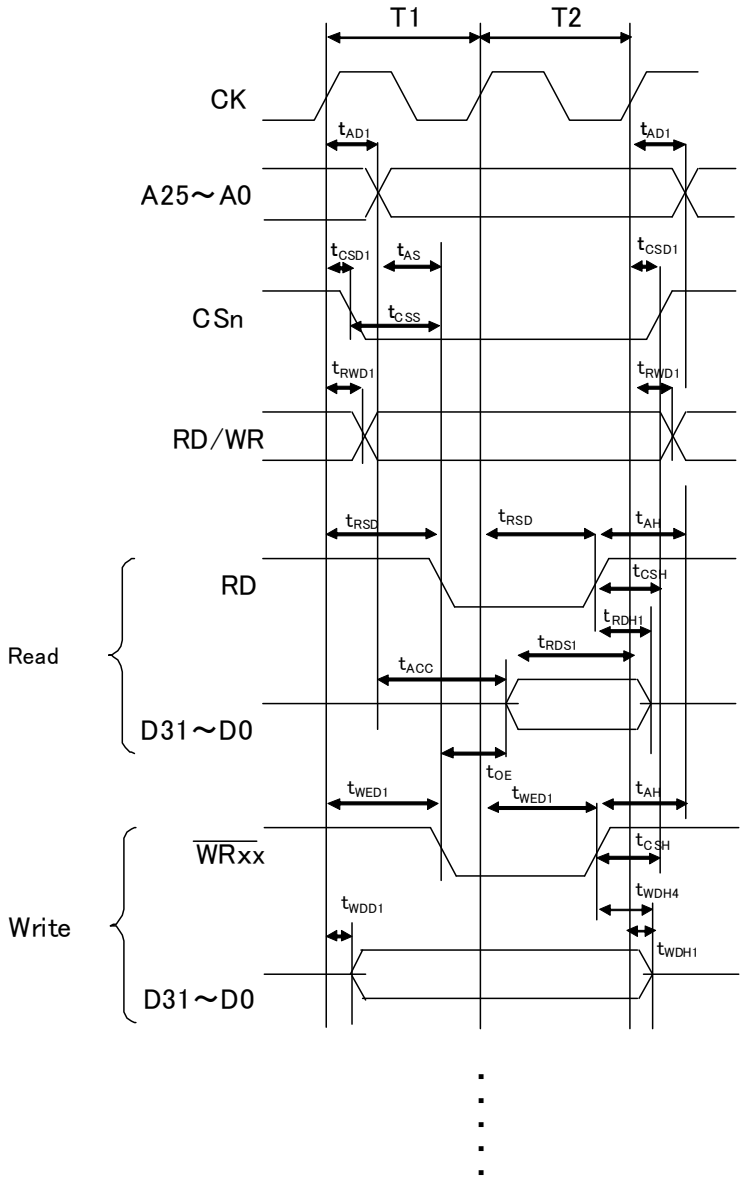


Figure 31.11 Normal Space Basic Bus Cycle (No Wait)

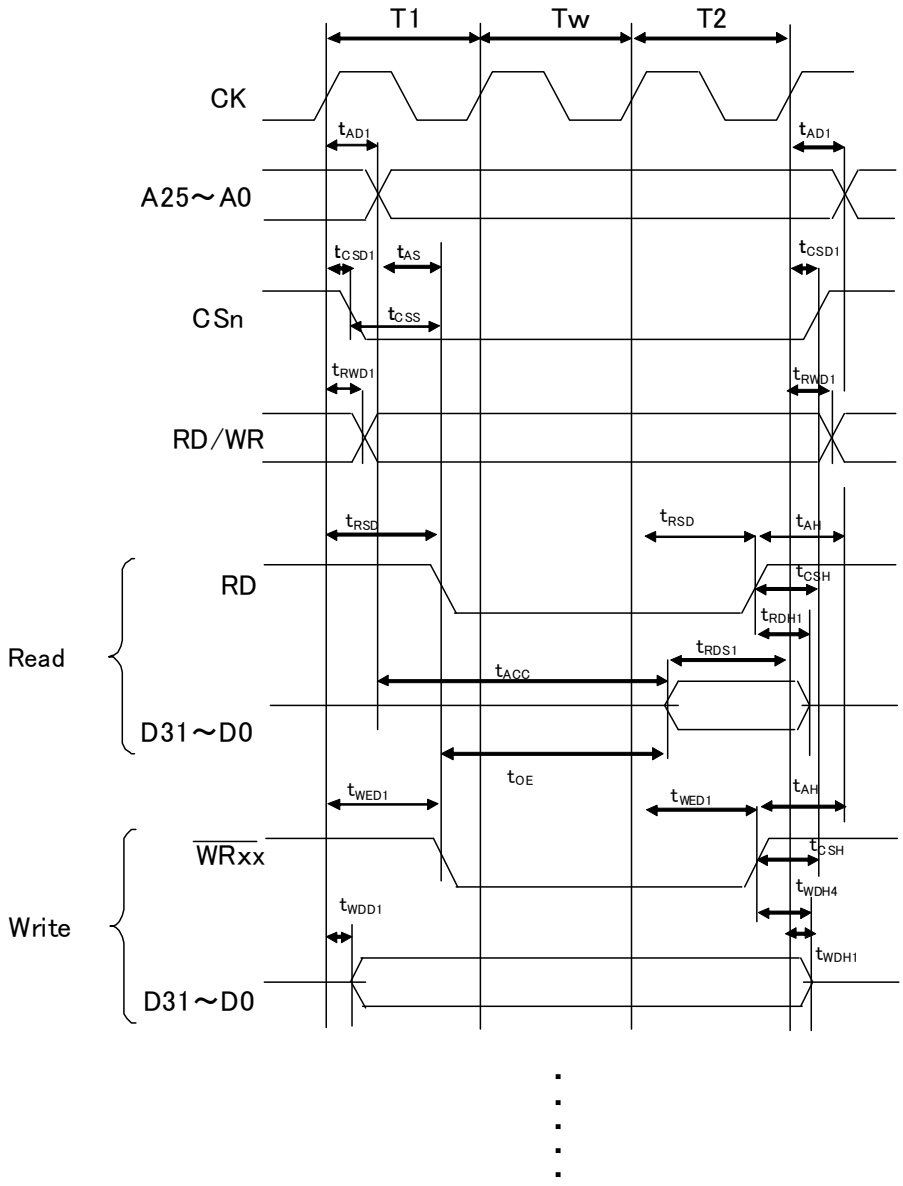


Figure 31.12 Normal Space Basic Bus Cycle (Software Wait 1)

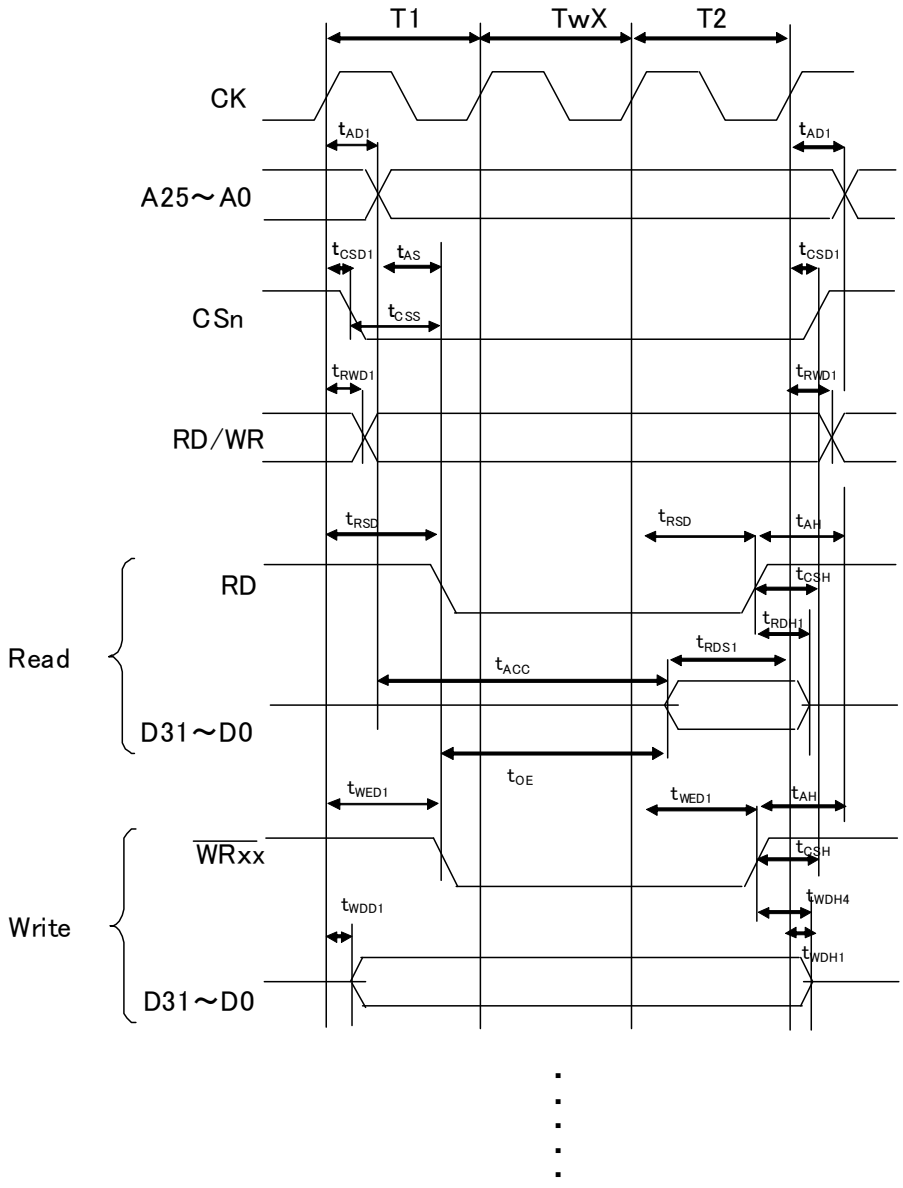


Figure 31.13 Normal Space Basic Bus Cycle (Insertion of External Wait 1)

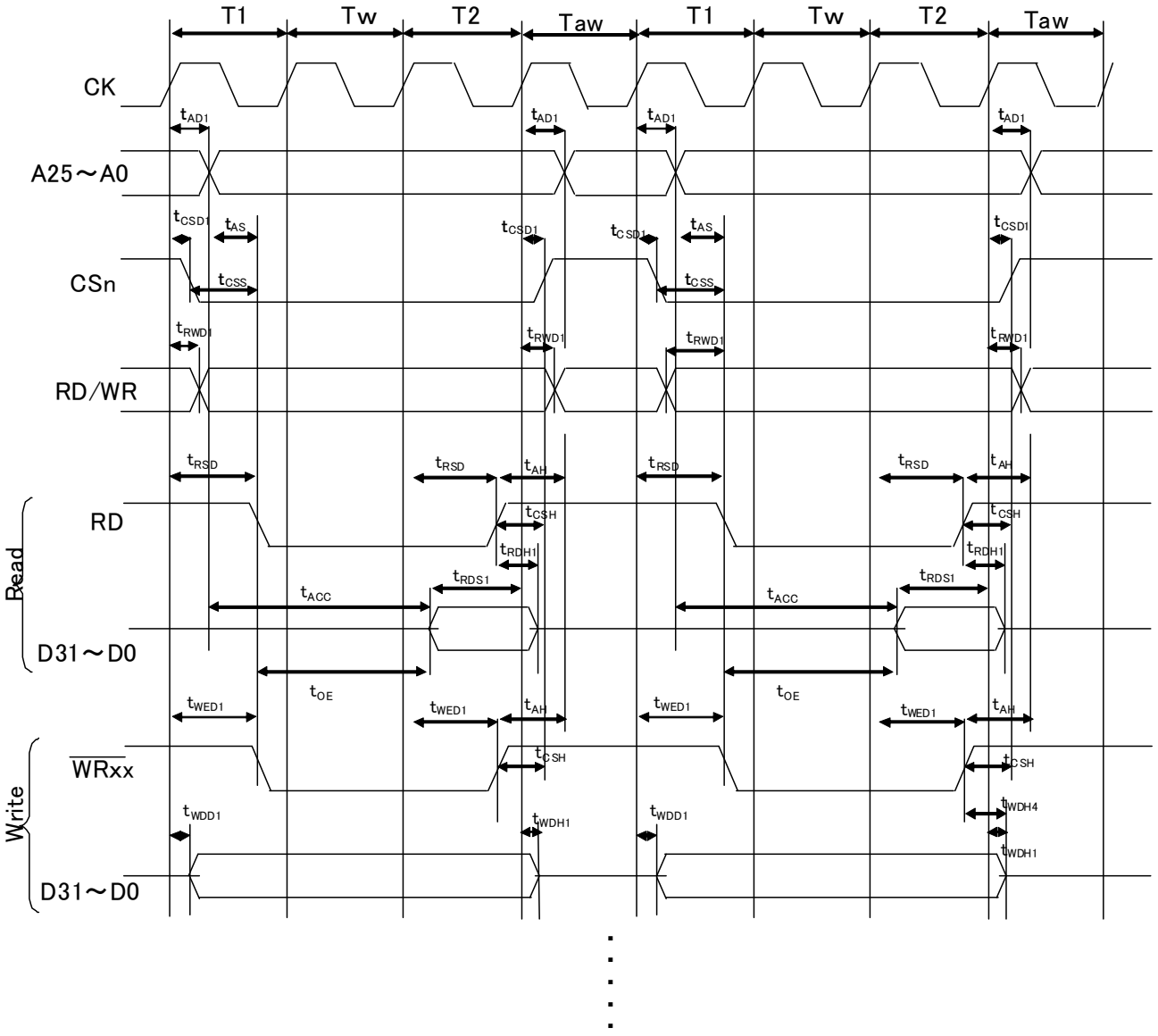


Figure 31.14 Normal Space Basic Bus Cycle
(Software Wait 1, External Wait Enabled (WM bit = 0), No Idle Cycle)

- Table 31.17, I2C Bus Interface 3 Timing in section 31.3.13, IIC3 Module Timing, has been revised as follows.

[Before change]

Item	Symbol	Test Conditions	Specifications Min.	Typ.	Max.	Unit	Figure
SCL input cycle time	t_{SCL}		12 t_{pcyc} + 600	—	—	ns	Figure 31.54
SCL input high pulse width	t_{SCLH}		3 t_{pcyc}+ 300	—	—	ns	
SCL input low pulse width	t_{SCLL}		5 t_{pcyc} + 300	—	—	ns	
SCL, SDA input rise time	t_{Sr}		—	—	300	t_{pcyc}*1	
SCL, SDA input fall time	t_{Sf}		—	—	1 t_{pcyc}	ns	
SCL, SDA input spike pulse removal time*2	t_{SP}		—	—	1 t_{pcyc}	ns	
SDA input bus free time	t_{BUF}		5	—	—	t_{pcyc}*1	
Start condition input hold time	t_{STAH}		3	—	—	t_{pcyc}*1	
Retransmit start condition input setup time	t_{STAS}		3	—	—	t_{pcyc}*1	
Stop condition input setup time	t_{STOS}		3	—	—	t_{pcyc}*1	
Data input setup time	t_{SDAS}		1 t_{pcyc} + 20	—	—	ns	
Data input hold time	t_{SDAH}		0	—	—	ns	
SCL, SDA capacitive load	Cb		0	—	400	pF	
SCL, SDA output fall time*3	t_{Sf}		20 + 0.1 cb	—	250	ns	

[After change]

Item	Symbol	Test Conditions	Specifications Min.	Typ.	Max.	Unit	Figure
SCL input cycle time	t_{SCL}		12 t_{pcyc}*1 + 600	—	—	ns	Figure 31.54
SCL input high pulse width	t_{SCLH}		3 t_{pcyc}*1+ 300	—	—	ns	
SCL input low pulse width	t_{SCLL}		5 t_{pcyc}*1 + 300	—	—	ns	
SCL, SDA input rise time	t_{Sr}		—	—	300	ns	
SCL, SDA input fall time	t_{Sf}		—	—	300	ns	
SCL, SDA input spike pulse removal time*2	t_{SP}		—	—	5 t_{pcyc}*2	t_{pcyc}*1	
SDA input bus free time	t_{BUF}		5	—	—	t_{pcyc}*1	
Start condition input hold time	t_{STAH}		3	—	—	t_{pcyc}*1	
Retransmit start condition input setup time	t_{STAS}		3	—	—	t_{pcyc}*1	
Stop condition input setup time	t_{STOS}		3	—	—	t_{pcyc}*1	
Data input setup time	t_{SDAS}		1 t_{pcyc}*1 + 20	—	—	ns	
Data input hold time	t_{SDAH}		0	—	—	ns	
SCL, SDA capacitive load	Cb		0	—	400	pF	
SCL, SDA output fall time*3	t_{Sf}		20 + 0.1 cb	—	250	ns	

- Table 31.24, Flash Memory Characteristics in section 31.7, Flash Memory Characteristics, has been revised as follows.

[Before change]

Item	Symbol	Min.	Typ.	Max.	Unit
Write time *1*2	t_P	—	1	10	ms/128 bytes
Erase time *1*3*4	t_E	—	0.6	1.5	s/byte
Number of rewrite times	N_{WEC}	—	—	100	times

[After change]

Item	Symbol	Min.	Typ.	Max.	Unit
Write time *1*2	t_P	—	2	20	ms/256 bytes
Erase time *1*3*4	t_E	—	0.6	1.5	s/byte
Number of rewrite times	N_{WEC}	—	—	100	times

- Section 31.8, Notes on Usage, has been added as follows.

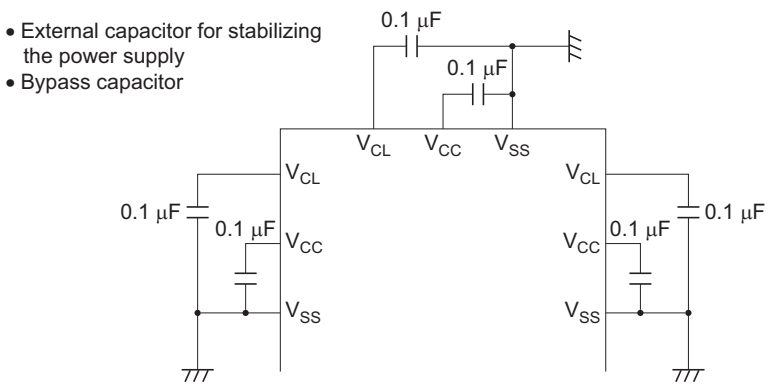
[After change]

31.8.1 Method of connecting capacitors

This LSI includes an internal voltage step-down circuit which is capable of automatically adjusting the power supply voltage downward to an optimum level. Connect a capacitor between the Vcl pin (the internally stepped-down voltage) and Vss pin to stabilize the internal voltage.

Figure 31.62 shows how the external capacitor should be connected. The external capacitor should be placed in the vicinity of the pin. Do not apply the power supply voltage to the Vcl pin.

Laminated ceramic capacitors should be connected between all pairs of Vcc and GND pins as bypass capacitors. The bypass capacitors should be placed as close to the power supply and ground pins as is possible. For crystal-oscillation related capacitors, see 4.9.1, Notes on Board Design. The values of both bypass capacitors and stabilizing capacitors for the internal voltage should be within the range from 0.02 μF to 0.33 μF.



Note: Do not apply the power supply voltage to Vcl pins.
Laminated capacitors should be used and placed as close to Vcl and Vcc pins. The capacitor value is recommnded.

Figure 31.62 Method of Connecting Capacitors