## Old Company Name in Catalogs and Other Documents

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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## HITACHI MICROCOMPUTER TECHNICAL UPDATE

20 September 2001	No.	TN-SH7-348B/E
Correction of errors on SH3, SH3-DSP hardware manualTHEME(Power on sequence)		
(Power on sequence)		
CLASSIFICATION Spec change Limitation on Use Supplementof Documents		
PRODUCTNAME SH7707,SH7709,SH7709A,SH7729		
REFERENCE       SH7707 Hardware maual Rev1.0 SH7709 Hardware manual Rev2.0 SH7709 A Hardware manual Rev4.0       SH7729 Hardware manual SH7729 Hardware manual	nual Rev3.0	3.0 Effective Date Permanent
		Lot No.: All
	Correction of errors on SH3, SH3-DSP hardw (Power on sequence) Spec change Supplementof Documents SH7707,SH7709,SH7709A,SH7729 SH7707 Hardware maual Rev1.0 SH7709 Hardware manual Rev2.0 SH7709A Hardware manual Rev4.0	Correction of errors on SH3, SH3-DSP hardware ma (Power on sequence)  Spec change Limi Supplementof Documents SH7707,SH7709,SH7709A,SH7729 SH7707 Hardware manual Rev1.0 SH7709 Hardware manual Rev2.0 SH7709 Hardware manual Rev2.0

This technical update is the revised version of 'TN-SH7-348A/E'.

1. SH7709A ADE-602-187C Rev.4.0: p.673 SH7729 ADE-602-157B Rev.3.0: p.731

"Caution" in "Electrical Characteristics" "Absolute Maximum Ratings" is corrected as follows.

1-1 description about undefined pin states

[Error]

2. Until Voltage is applied to all power supplies and a low level is input at the RESETP pin, internal circuits remain unsettled, and so pin states are also undefined. The system design must ensure that these undefined states do not cause erroneous system operation.

[Correction]

2. Until Voltage is applied to all power supplies, a high level is input at the CA pin, a low level is input at the RESETP pin, and CKIO clock operates in  $\underline{\max 4 \text{ cycles}}$ , internal circuits remain unsettled, and so pin states are also undefined.

The system design must ensure that these undefined states do not cause erroneous system operation.

When a low level is input at the CA pin, a low level input at the RESETP pin is not accepted.

1-2 description about interval of 3.3V powers and 1.8/1.9V powers turning on/off  $\left[ \text{Error} \right]$ 

100µs

[Correction] 1 ms 2. SH7707 ADE-602-137 Rev.1.0: p.685

The following sentences are added to "Caution" in "Electrical Characteristics" "Absolute Maximum Ratings".

Until Voltage is applied to all power supplies and a low level is input at the RESET pin and CKIO clock operates in <u>max 4 cycles</u>, internal circuits remain unsettled, and so pin states are also undefined. The system design must ensure that these undefined states do not cause erroneous system operation.

3. SH7709 ADE-602-123B Rev.2.0: p.595

The following sentences are added to "Caution" in "Electrical Characteristics" "Absolute Maximum Ratings".

Until Voltage is applied to all power supplies, a high level is input at the CA pin, a low level is input at the RESETP pin, and CKIO clock operates in <u>max 4 cycles</u>, internal circuits remain unsettled, and so pin states are also undefined.

The system design must ensure that these undefined states do not cause erroneous system operation.

When a low level is input at the CA pin, a low level input at the RESETP pin is not accepted.