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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A339A/E	Rev.	1.00
Title	Changes to the DMAC Activation by Peripheral Module Interrupt in the H8SX		Information Category	Technical Notification		
Applicable Product	H8SX/1657 Group	Lot No. All lots	Reference Document	See below.		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the following changes on the DMAC activation by the peripheral module interrupt in the H8SX/1657 Group Hardware Manual.

1. Modification in the DMA Controller Register

[Before change]

7.3 Register Descriptions
7.3.6 DMA Mode Control Register (DMDR)

Bit	Bit Name	Initial Value	R/W	Description
5	DTA	0	R/W	Data Transfer Acknowledge When the on-chip module interrupt is selected as a DMAC activation source, this bit must be set to 1.

[After change]

7.3 Register Descriptions
7.3.6 DMA Mode Control Register (DMDR)

Bit	Bit Name	Initial Value	R/W	Description
5	DTA	0	R/W	Data Transfer Acknowledge This bit is valid while the DMA transfer is performed by the on-chip module interrupt. This bit decides whether the source flag selected by DMRSR is cleared or not. 0: The source flag is not cleared while the DMA transfer is performed by the on-chip module interrupt. Since the source flag is not cleared by the DMA transfer, it should be cleared by the CPU or DTC transfer. 1: The source flag is cleared while the DMA transfer is performed by the on-chip module interrupt. Since the source flag is cleared by the DMA transfer, there is no need to request an interrupt to the CPU or DTC.

2. Modification in the DMA Controller Activation Source

[Before change]

7.5.3 Activation Sources

(2) Activation by On-Chip Module Interrupt

An interrupt request from an on-chip peripheral module (on-chip peripheral module interrupt) is used as a transfer request. When a DMA transfer is enabled (DTE = 1), the DMA transfer is started by an on-chip module interrupt.

The activation source of the on-chip module interrupt is selected by the DMA module request select register (DMRSR). The activation sources are specified to the individual channels. Table 7.5 is a list of on-chip module interrupts for the DMAC.

The DMAC receives interrupt requests by on-chip peripheral modules independent of the interrupt controller. Therefore, the DMAC is not affected by priority given in the interrupt controller.

When the DMAC is activated by the activation source which is selected while DTE = 1, the interrupt request flag is automatically cleared by a DMA transfer. If multiple channels use a single transfer request as an activation source, when the channel having priority is activated, the interrupt request flag is cleared. In this case, other channels may not be activated because the transfer request is not held in the DMAC.

When an activation source is selected while DTE = 0, the activation source does not request a transfer to the DMAC. It requests an interrupt to the CPU or DTC.

In addition, make sure that an interrupt request flag as an on-chip module interrupt source is cleared to 0 before writing 1 to the DTE bit.

[After change]

7.5.3 Activation Sources

(2) Activation by On-Chip Module Interrupt

An interrupt request from an on-chip peripheral module (on-chip peripheral module interrupt) is used as a transfer request. When a DMA transfer is enabled (DTE = 1), the DMA transfer is started by an on-chip module interrupt.

The activation source of the on-chip module interrupt is selected by the DMA module request select register (DMRSR). The activation sources are specified to the individual channels. Table 7.5 is a list of on-chip module interrupts for the DMAC.

The interrupt request selected as an activation source can simultaneously generate interrupt requests to the CPU or DTC. For details, see section 5, Interrupt Controller.

The DMAC receives interrupt requests by on-chip peripheral modules independent of the interrupt controller. Therefore, the DMAC is not affected by priority given in the interrupt controller.

When the DMAC is activated with DTA = 1, the interrupt request flag is automatically cleared by a DMA transfer. If multiple channels use a single transfer request as an activation source, when the channel having priority is activated, the interrupt request flag is cleared. In this case, other channels may not be activated because the transfer request is not held in the DMAC.

When the DMAC is activated with DTA = 0, the interrupt request flag is not cleared by the DMAC. It should be cleared by the CPU or DTC transfer.

When an activation source is selected while DTE = 0, the activation source does not request a transfer to the DMAC. It requests an interrupt to the CPU or DTC.

In addition, make sure that an interrupt request flag as an on-chip module interrupt source is cleared to 0 before writing 1 to the DTE bit.

3. Modification in the DTC and DMAC Activation by the Interrupt Controller

[Before change]

5.6.5 DTC and DMAC Activation by Interrupt

Selection of Interrupt Sources: The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTA = 1 in DMDR) and the DTE bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

Specifying the DISEL bit in MRB of the DTC generates an interrupt request to the CPU by clearing the DTCE bit to 0 after the individual DTC data transfer.

Note that when the DTC performs a predetermined number of data transfers and the transfer counter indicates 0, an interrupt request is made to the CPU by clearing the DTCE bit to 0 after the DTC data transfer.

When the same interrupt source is set as both the DTC activation source and CPU interrupt source, the DTC must be given priority over the CPU. If the IPSETE bit in CPUPCR is set to 1, the priority is determined according to the IPR setting. Therefore, the CPUP setting or the IPR setting corresponding to the interrupt source must be set to lower than or equal to the DTCP setting. If the CPU is given priority over the DTC, the DTC may not be activated, and the data transfer may not be performed.

Priority Determination: Omitted (No changes)

Operation Order: If the same interrupt is selected as both the DTC activation source and CPU interrupt source, the CPU interrupt exception handling is performed after the DTC data transfer. If the same interrupt is selected as the DTC or DMAC activation source or CPU interrupt source, respective operations are performed independently.

Table 5.6 lists the selection of DMAC activation sources and the selection of interrupt sources and interrupt source clear control by means of the setting of the DTCE bit in DTCERA to DTCERH of the DTC and the DISEL bit in MRB of the DTC.

Table 5.6 Interrupt Source Selection and Clear Control

DMAC Setting	DTC Setting		Interrupt Source Selection/Clear Control		
DTE	**DTCE**	**DISEL**	**DMAC**	**DTC**	**CPU**
0	0	*	X	X	√
	1	0	X	√	X
		1	X	O	O
1	*	*	√	X	X

[Legend]

√: The corresponding interrupt is used. The interrupt source is cleared.

(The interrupt source flag must be cleared in the CPU interrupt handling routine.)

O: The corresponding interrupt is used. The interrupt source is not cleared.

X: The corresponding interrupt is not available.

*: Don't care.

Usage Note: The interrupt sources of the SCI and A/D converter are cleared according to the setting shown in table 5.6, when the DTC or DMAC reads/writes the prescribed register.

To initiate multiple channels for the DTC with the same interrupt, the same priority should be assigned.

[After change]

5.6.5 DTC and DMAC Activation by Interrupt

Selection of Interrupt Sources: The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

Specifying the DISEL bit in MRB of the DTC generates an interrupt request to the CPU by clearing the DTCE bit to 0 after the individual DTC data transfer.

Note that when the DTC performs a predetermined number of data transfers and the transfer counter indicates 0, an interrupt request is made to the CPU by clearing the DTCE bit to 0 after the DTC or DMAC data transfer.

When the same interrupt source is set as both the DTC or DMAC activation source and CPU interrupt source, the DTC must be given priority over the CPU. If the IPSETE bit in CPUPCR is set to 1, the priority is determined according to the IPR setting. Therefore, the CPUP setting or the IPR setting corresponding to the interrupt source must be set to lower than or equal to the DTCP or DMAP setting. If the CPU is given priority over the DTC or DMAC, the DTC or DMAC may not be activated, and the data transfer may not be performed.

Priority Determination:

Omitted (No changes)

Operation Order: If the same interrupt is selected as both the DTC activation source and CPU interrupt source, the CPU interrupt exception handling is performed after the DTC data transfer. If the same interrupt is selected as the DTC or DMAC activation source or CPU interrupt source, respective operations are performed independently. Table 5.6 lists the selection of interrupt sources and interrupt source clear control by means of the setting of the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC and the DISEL bit in MRB of the DTC.

Table 5.6 Interrupt Source Selection and Clear Control

DMAC Setting	DTC Setting		Interrupt Source Selection/Clear Control		
DTA	DTCE	DISEL	DMAC	DTC	CPU
0	0	*	O	X	√
	1	0	O	√	X
		1	O	O	√
1	*	*	√	X	X

[Legend]

√: The corresponding interrupt is used. The interrupt source is cleared.

(The interrupt source flag must be cleared in the CPU interrupt handling routine.)

O: The corresponding interrupt is used. The interrupt source is not cleared.

X: The corresponding interrupt is not available.

*: Don't care.

Usage Note: The interrupt sources of the SCI and A/D converter are cleared according to the setting shown in table 5.6, when the DTC or DMAC reads/writes the prescribed register.

To initiate multiple channels for the DTC with the same interrupt, the same priority (DTCP = DMAP) should be assigned.

4. Target Product

Reference Document: H8SX/1657 Group Hardware Manual (Rev. 1.00 REJ09B0106-0100Z)