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# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	25 May 2000	No.		TN-H8*-171A/E		
THEME	Attention on use Timer F					
CLASSIFICATION	<ul> <li>Spec. change</li> <li>Limitation on</li> <li>Supplement of Documents</li> </ul>					
	H8/3887 series, H8/3847 series, H8/3867 series,			Lot No. etc.		
PRODUCT NAME	H8/3827 series, H8/3847R series,					
	H8/3827R series, H8/3802 series			All Lot		
	H8/3887 series, H8/3847 series Hardware Manua	al Rev. 2	2.0	Effective Date		
REFERENCE DOCUMENTS	H8/3867 series, H8/3827 series Hardware Manua	al Rev. 3	.0	Eternal		
	H8/3847R series, H8/3827R series, H8/3802 series			From		
	Hardware Manual Rev. 1.0					

We appreciate your selection of Hitachi microcomputers.

We inform you of additional information for Hitachi single chip

microcomputer H8/3887/47/67/27/47R/27R series, H8/3802 series Hardware Manual.

<Additional contents>

9.4 Timer F ----(For H8/3887/47 series, in section 9.4 on P 197. For H8/3867/27 series, in section 9.4 on P 194. For H8/3827R series, in section 9.4 on P 193. For H8/3847R series, in section 9.4 on P203. For H8/3802 series, in section 9.3 on P 174)

9.4.5 Application Notes ----(For H8/3887/47 series, in section 9.4.5 on P 214. For H8/3867/27 series, in section 9.4.5 on P 212. For H8/3827R series, in section 9.4.5 on P 210. For H8/3847R series, in section 9.4.5 on P 220. For H8/3802 series, in section 9.3.5 on P192)

(3) Clear timer FH, timer FL interrupt request flags (IRRTFH, IRRTFL), timer overflow flags H, L (OVFH, OVFL) and compare match flags H, L (CMFH, CMFL)

When  $\phi$  w/4 is selected as the internal clock, "Interrupt factor generation signal" will be operated with  $\phi$  w and the signal will be outputted with  $\phi$  w width.

And, "Overflow signal" and "Compare match signal" are controlled with 2 cycles of  $\phi$  w signals. Those signals are outputted with 2 cycles width of  $\phi$  w. (Figure 1)

In active (high-speed, medium-speed) mode, even if you cleared interrupt request flag during the term of validity of "Interrupt factor generation signal", same interrupt request flag is set. (Figure 1-1). And, you cannot be cleared timer overflow flag and compare match flag during the term of validity of "Overflow signal" and "Compare match signal".

For interrupt request flag is set right after interrupt request is cleared, interrupt process to one time timer FH, timer FL interrupt might be repeated. (Figure1-2)

Therefore, to definitely clear interrupt request flag in active (high-speed, medium-speed) mode, clear should be processed after the time that calculated with below (1) formula. And, to definitely clear timer overflow flag and compare match flag, clear should be processed after read timer control status register F(TCSRF) after the time that calculated with below (1) formula.

For ST of (1) formula, please substitute the longest number of execution states in used instruction.

(10 states of RTE instruction when MULXU, DIVXU instruction is not used, 14 states when MULXU, DIVXU instruction is used)

In subactive mode, there are no limitation for interrupt request flag, timer overflow flag, and compare match flag clear.

The term of validity of "Interrupt factor generation signal"

=1 cycle of  $\phi$  w + waiting time for completion of executing instruction + interrupt time synchronized with  $\phi$ 

 $=1/\phi \text{ w }+\text{ST}\times(1/\phi)+(2/\phi) \text{ (second)}\cdots(1)$ 

ST: Executing number of execution states

Method 1 is recommended to operate for time efficiency.

(Method1)

1. Prohibit interrupt in interrupt handling routine (set IENFH, IENFL to "0").

- 2.After program process returned normal handling, clear interrupt request flags (IRRTFH, IRRTFL) after more than time that calculated with (1) formula.
- 3.After read timer control status register F (TCSRF), clear timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).

4.Operate interrupt permission (set IENFH, IENFL to "1").

(Method2)

1.Set interrupt handling routine time to more than time that calculated with (1) formula.

- 2.Clear interrupt request flags (IRRTFH, IRRTFL) at the end of interrupt handling routine.
- 3.After read timer control status register F (TCSRF), clear timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).

All above attentions are also applied in 16bit mode and 8bit mode.

	Interrupt request flag clear Interrupt request flag clear I
Program process	Interrupt   Interrupt   Normal
φ W	
Interrupt factor	
(Internal signal, nega-acitve)	
Overflow signal,	
Compare match signal	
(Internal signal, nega-acitve)	
Interrupt request flag	
(IRRTFH,IRRTFL)	 1

Figure 1 Clear interrupt request flag when interrupt factor generation signal is valid

#### (4) Timer counter (TCF) read/write

When  $\phi$  w/4 is selected as the internal clock in active(high-speed, medium-speed) mode, write on TCF is impossible. And, when read TCF, as the system clock and internal clock are mutually asynchronous, TCF synchronizes with synchronization circuit.

This results in a maximum TCF read value error of  $\pm 1$ .

When read/write TCF in active(high-speed, medium-speed) mode is needed, please select internal clock except for  $\phi$  w/4 before read/write.

In subactive mode, even  $\phi$  w/4 is selected as the internal clock, normal read/write TCF is possible.

## **HITACHI SEMICONDUCTOR TECHNICAL**

DATE	14 September 2000No.	TN-H8*-186A/E
THEME	DC characteristics of the port 9	
CLASSIFICATION	Spec. change Limi	itation on Use
PRODUCT NAME	HD6473802,HD6433802,HD6433801,HD6433800	Lot No.etc. All lots
REFERENCE DOCUMENTS	H8/3802 Series Hardware Manual (ADE-602-203)	Effective Date Eternal From Now

The DC characteristics of the port 9 are changed in Hitachi single chip microcomputer H8/3802 series hardware manual. We want it understood and approved.

Section 14 Electrical Characteristics

14.2 H8/3802 Series Electrical Characteristics

14.2.2 DC Characteristics

Table 14.2 DC Characteristics•••(P312)

(Incorrect)

				Value	8			
Item	Symbol	Applicable Pins	Min	Тур	Max	Unit	Test Condition	Notes
Output low	Vol	P90 to P92	-	-	0.5	-	Iol=25mA	
voltage		P93 to P95		_	0.5		Iol=10mA	

(Correct)

				Value	8		•	
Item	Symbol	Applicable Pins	Min	Тур	Max	Unit	Test Condition	Notes
Output low	Vol	P90 to P92	-	-	0.5	<u>V</u>	<u>Vcc=2.2 to 5.5V</u>	<u>*5</u>
voltage							IoL=25mA	
		· · ·					Iol=15mA	
		P93 to P95		-	0.5	V	Iol=10mA	

### **HITACHI SEMICONDUCTOR TECHNICAL**

DATE	14 September 2000 N	Io. TN-H <b>8*-</b> 187A/E
THEME	Error Correction of H8/3802 Series Hardware M	anual
CLASSIFICATION	□ Spec. change □ L ■ Supplement of Documents	imitation on Use
PRODUCT NAME	HD6473802,HD6433802,HD6433801,HD64338	00 Lot No.etc. All lots
REFERENCE	H8/3802 Series Hardware Manual	Effective Date Eternal
DOCUMENTS	(ADE-602-203)	From Now

The error corrections in Hitachi single chip microcomputer H8/3802 series hardware manual are given below. We want it understood and approved.

Section 3 Exception Handling 3.3 Interrupts 3.3.2 Interrupt Control Registers

 Table 3.3
 Interrupt Control Registers
 ······(P61)

#### (Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
IRQ edge select register	IEGR	R/W	<u>H'FC</u>	H'FFF2
Interrupt enable register 1	IENR1	R/W	<u>H'58</u>	H'FFF3
Interrupt enable register 2	IENR2	R/W	<u>H'32</u>	H'FFF4
Interrupt request register 1	IRR1	R/W*	<u>H'78</u>	H'FFF6
Interrupt request register 2	IRR2	R/W*	<u>H'32</u>	H'FFF7
Wakeup interrupt request register	IWPR	R/W*	H'00	H'FFF9
Wakeup edge select register	WEGR	R/W	H'00	H'FF90

(Correct)

Name	Abbrev.	R/W	Inițial Value	Address
IRQ edge select register	IEGR	R/W		H'FFF2
Interrupt enable register 1	IENR1	R/W	_	H'FFF3
Interrupt enable register 2	IENR2	R/W		H'FFF4
Interrupt request register 1	IRR1	R/W*		H'FFF6
Interrupt request register 2	IRR2	R/W*		H'FFF7
Wakeup interrupt request register	IWPR	R/W*	H'00	H'FFF9
Wakeup edge select register	WEGR	R/W	H'00	H'FF90

Section 3 Exception Handling **3.3 Interrupts** 3.3.2 Interrupt Control Registers 1. IRQ edge select register (IEGR) ·····(P61) (Incorrect) Bit 7 6 4 3 2 0 5 1 \_ IEG1 IEG0 1. Initial value 1 0 1 1. 1 0 1 **Read/Write** R/W R/W IEGR is an 8-bit read/write register used to designate whether pins IRQ1 and IRQ0 are set to rising edge sensing or falling edge sensing. Bits 7 to 2: Reserved bits Bits 7 to 2 are reserved; they are always read as 1 and cannot be modified. (Correct) Bit 7 6 5 3 2 1 0 IEG1 IEG0 Initial value 1 1 1、 0 0 **Read/Write** — R/W R/W ÷ IEGR is an 8-bit read/write register used to designate whether pins IRQ1 and IRQ0 are set to rising edge sensing or falling edge sensing. Bits 7 to 5: Reserved bits Bits 7 to 5 are reserved; they are always read as 1 and cannot be modified. Bits 4 to 2: Reserved bits . Bits 4 to 2 are reserved bits. Section 3 Exception Handling **3.3 Interrupts 3.3.2 Interrupt Control Registers** 2. Interrupt enable register 1 (IENR1)  $\cdots \cdot (P62 \text{ to } P63)$ (Incorrect) Bit  $\mathbf{7}$ 6 5 2 4 3 0 1 IENTA **IENWP** . IENEC2 İEN1 IEN0 Initial value 0 . 0 1, 0 1 1 0 0 **Read/Write** R/W R/W R/W R/W R/W Bit 6: Reserved bit Bit 6 is reserved; it is always read as 1 and cannot be modified. Bits 4 and 3: Reserved bits Bits 4 and 3 are reserved; they are always read as 1 and cannot be modified.

Bit	7	6	5	4	3	2	1	0
	IENTA		IENWP			IENEC2	IEN1	IENQ
Initial value	0、	Ξ,	0	Ξ.	<u> </u>	0	Q.	0
Read/Write	R/W	·	R/W		-·.	<b>R/W</b> .	R/W	R/W .
Bit 6: Reserved b	<u>vit</u>							
Bit 6 is reserved b	<u>it.</u> •							
Bits 4 and 3: Rea	served bits							
Bits 4 and 3 are re	eserved bits.							
Section 3 I	Exception Ha	ndling						
3.3 Interru	-	0						
	rupt Control	0		(-				
	ot enable regi	ster 2 (IE	NR2)	•••••(1	263 to P64	1)		
(Incorrect)	_	~	_		-	_	-	_
Bit		6	5	4	3	2	1	0
<b></b>		IENAD,	,	- 1	IENTFH	IENTFL	_ ,	IENEC
Initial value	0,	0,	<u>1</u> ,	1	0	0	<u>1</u> ,	0
Read/Write	R/W	R/W	Ξ.	Ξ,	R/W ,	R/W ,	Ξ.	R/W
Bits 5 and 4: Res								
Bits 5 and 4 are re		<u>hey are a</u>	lways read	<u>as 1 and</u>	<u>cannot be</u>	modified.		
Bit 1: Reserved b Bit 1 is reserved; i	_	ad as 1 a			J			
<u>Dit i is reserved</u> , i	t is always re	auasia	na cannot b	<u>e moarrie</u>	<u>a.</u>			
(Correct)								
()								
Bit	7	6	5	4	3	2	1	n
Bit	7 IENDT	6 IENAD	5	4	3	2 IENTEL	1	0 IENEC
	7 IENDT,	IENAD	5	4	IENTĘH	IENTĘL	1	IENEC
Initial value	0	IENAD 0	= .	4 —   = w	IENTĘH 0	IENTFL	1 — — — —	IENEC 0
Initial value Read/Write	0 R/W	IENAD	5 —	4 — , — — 	IENTĘH	IENTĘL		IENEC
Initial value Read/Write <u>Bits 5 and 4: Rese</u>	0 R/W	IENAD 0 R/W	— — 		IENTĘH 0	IENTFL		IENEC 0
Initial value Read/Write <u>Bits 5 and 4: Rese</u> Bits 5 and 4 are re	0 R/W erved bits served; only a	IENAD 0 R/W	— — 		IENTĘH 0	IENTFL		IENEC 0
Initial value Read/Write <b>Bits 5 and 4: Rese</b> <u>Bits 5 and 4 are re</u> <b>Bit 1: Reserved bi</b>	0 R/W erved bits served; only :	IENAD 0 R/W a write of	U is possible		IENTĘH 0	IENTFL	1 — — — 	IENEC 0
Initial value Read/Write <u>Bits 5 and 4: Rese</u> <u>Bits 5 and 4 are re</u> <u>Bit 1: Reserved bi</u> <u>Bit 1 is reserved; o</u>	0 R/W erved bits eserved; only a t enly a write o	IENAD 0 R/W a write of f 0 is poss	U is possible		IENTĘH 0	IENTFL	1 — — — 	IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved bi Bit 1 is reserved; o Section 3 B	0 R/W erved bits eserved; only a t only a write only Exception Har	IENAD 0 R/W a write of f 0 is poss	U is possible		IENTĘH 0	IENTFL		IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved bi Bit 1 is reserved; o Section 3 H 3.3 Interry	0 R/W erved bits eserved; only a served; only a conly a write of Exception Ham	IENAD 0 R/W a write of f 0 is poss	U is possible		IENTĘH 0	IENTFL	1 — — — 	IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved bit Bit 1 is reserved; o Section 3 H 3.3 Interru 3.3.2 Inter	0 R/W erved bits eserved; only a t only a write only Exception Har	IENAD 0 R/W a write of f 0 is poss ndling Registers	U is possible		IENTFH 0 R/W	IENTFL		IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved bi Bit 1 is reserved; o Section 3 H 3.3 Interru 3.3.2 Inter- 4. Interrup	0 R/W erved bits eserved; only a served; only a served; only a entry a write of Exception Han upts rupt Control	IENAD 0 R/W a write of f 0 is poss ndling Registers	U is possible	<u>e.</u> .	IENTFH 0 R/W	IENTFL		IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved bi Bit 1 is reserved; o Section 3 H 3.3 Interru 3.3.2 Inter- 4. Interrup	0 R/W erved bits eserved; only a served; only a served; only a entry a write of Exception Han upts rupt Control	IENAD 0 R/W a write of f 0 is poss ndling Registers	U is possible	<u>e.</u> .	IENTFH 0 R/W	IENTFL		IENEC 0
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are rea Bit 1: Reserved bit Bit 1 is reserved: o Section 3 H 3.3 Interrue 3.3.2 Interrue 4. Interrup (Incorrect)	0 R/W erved bits eserved; only : eserved; only : t only a write or Exception Han pts rupt Control of request reg	IENAD 0 R/W a write of f 0 is poss ndling Registers ister 1 (II	U is possible	<u>e.</u> .	IENTFH 0 R/W	IENTĘL .0 R/W		IENEC 0 R/W
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are rea Bit 1: Reserved bit Bit 1 is reserved: o Section 3 H 3.3 Interrue 3.3.2 Interrue 4. Interrup (Incorrect)	0 R/W erved bits eserved; only a served; only a enly a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of the only a write of th	IENAD 0 R/W a write of f 0 is poss ndling Registers ister 1 (II	U is possible	e (F 4 _	IENTFH 0 R/W 265) 3 	IENTĘL .0 R/W 2 IRREC2		IENEC 0 R/W
Initial value Read/Write Bits 5 and 4: Rese Bits 5 and 4 are re Bit 1: Reserved big Bit 1 is reserved; o Section 3 H 3.3 Interru 3.3.2 Interru 4. Interrup (Incorrect) Bit	0 R/W erved bits eserved; only a served; only a ser	IENAD 0 R/W a write of f 0 is poss ndling Registers ister 1 (II 6 — .		<u>e.</u> .	IENTFH 0 R/W	IENTFL .0 R/W	1 IRRI1	IENEC 0 R/W 0 IRRIQ

### Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved: they are always read as 1 and cannot be modified.

Bit	7	6	5	4	3	2	1	0
	IRRTA .		_	_	· <u> </u>	IRREC2	IRRI1	IRRIO
Initial value	0	<b>—</b> .	 1 _	<u> </u>	· _	0	0	0
Read/Write	R/W* .	<u> </u>	- ·	· — .	— , —	R/W*.	R/W*	R/W*
Bits 6 and 4,3: Res		• -	• •		• -	10,11		10/11
Bits 6 and 4,3 are 1								
Bit 5: Reserved bit		<u>~</u>						
Bit 5 is reserved; it		ad as 1 ar	id cannot '	be modifie	ed.			
	·····							
Section 3 E	xception Ha	ndling						
3.3 Interru	-							
	rupt Control t request reg		נפסי		P67, P68)			
(Incorrect)	t lequest leg	(15ter 2 (11)	(1(2)	. (	107, 100)			
Bit	7	6	5	4	3	2	1	0
Dit	IRRDT	IRRAD		Ŧ	IRRTFH	IRRTFL	1	IRREC
	110001,	minab		,	111111111		<u>1</u>	Innac
Initial value		0	1	1	Δ	0	1	^
Initial value	0	0	<u>1</u>	<u> </u>	0	0 . D <i>(</i> 11)*	<u>1</u> ,	0
Read/Write	R/W*	0 R/W*	1 `	1 `,	0 R/W*	0 . . R/W*.	<u>1</u> 	0 R/W*
Read/Write Bits 5 and 4: Rese	R/W*	R/W*	=`.	`,	R/W*	<b>R/W*</b> .	1 —	,
Read/Write Bits 5 and 4: Rese Bits 5 and 4 are res	R/W* rved bits served; they	R/W*	=`.	`,	R/W*	<b>R/W*</b> .	<u>1</u> 	,
Read/Write Bits 5 and 4: Reser <u>Bits 5 and 4 are res</u> Bit 1: Reserved bit	R/W* rved bits served: they	R/W* are alway	=`. s read as 1	=	R/W*	<b>R/W*</b> .	1	,
	R/W* rved bits served: they	R/W* are alway	=`. s read as 1	=	R/W*	<b>R/W*</b> .	<u>1</u> —	,
Read/Write Bits 5 and 4: Reset Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it	R/W* rved bits served: they	R/W* are alway	=`. s read as 1	=	R/W*	<b>R/W*</b> .	1	,
Read/Write Bits 5 and 4: Reser Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it (Correct)	R/W* rved bit <u>s</u> served; they is always re	R/W* are alway: ead as 1 ar	=`. s read as 1 ud cannot 1	` L and cann be modifie	R/W <sup>*</sup>	R/W*	=	R/W*
Read/Write Bits 5 and 4: Reset Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it	R/W* rved bits served; they is always re	R/W* are always ead as 1 ar	=`. s read as 1	=	R/W*	R/W* ified. 2		R/W* 0
Read/Write Bits 5 and 4: Reset Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it (Correct) Bit	R/W* rved bits served; they is always re 7 IRRDT	R/W* are always ead as 1 ar 6 IRRAD	=`. s read as 1 ud cannot 1	` L and cann be modifie	R/W* not be mod ed. 3 IRRTFH	R/W* ified. 2 IRRTFL	=	R/W*
Read/Write Bits 5 and 4: Reser Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it (Correct) Bit Initial value	R/W* rved bits served; they is always re 7 IRRDT 0	R/W* are alway: ead as 1 ar 6 IRRAD 0	= ` s read as 1 id cannot 1 5 	` <u>L and cann</u> be modifie <u>4</u> 	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; it</u> (Correct) Bit Initial value Read/Write	R/W* rved bits served: they is always re 7 IRRDT 0 R/W*	R/W* are always ead as 1 ar 6 IRRAD	=`. s read as 1 ud cannot 1	` L and cann be modifie 4 	R/W* not be mod ed. 3 IRRTFH	R/W* ified. 2 IRRTFL	=	R/W*
Read/Write <u>Bits 5 and 4: Reserved</u> <u>Bits 5 and 4 are readed</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; it</u> (Correct) Bit Initial value Read/Write <u>Bits 5 and 4: Reserved</u>	R/W* rved bits served; they is always re 7 IRRDT 0 R/W* rved bits	R/W* are always ead as 1 ar 6 IRRAD 0 R/W*	= s read as 1 nd cannot 5  = <u>W</u>	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved: it</u> (Correct) Bit Initial value Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u>	R/W* rved bits served: they is always re 7 IRRDT 0 R/W* rved bits served: only	R/W* are always ead as 1 ar 6 IRRAD 0 R/W*	= s read as 1 nd cannot 5  = <u>W</u>	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write <u>Bits 5 and 4: Reserved</u> <u>Bits 5 and 4 are readed</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; it</u> (Correct) Bit Initial value Read/Write <u>Bits 5 and 4: Reserved</u>	R/W* rved bits served: they is always re 7 IRRDT 0 R/W* rved bits served: only	R/W* are always ead as 1 ar 6 IRRAD 0 R/W*	= s read as 1 nd cannot 5  = <u>W</u>	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; it</u> (Correct) Bit Initial value Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 1: Reserved bit</u>	R/W* rved bits served; they is always re 7 IRRDT 0 R/W* rved bits served; only	R/W* are always ead as 1 ar 6 IRRAD 0 R/W* a write of	= s read as 1 id cannot 5   W 0 is possib	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write Bits 5 and 4: Reser Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; it (Correct) Bit Initial value Read/Write Bits 5 and 4: Reser Bits 5 and 4 are res Bit 1: Reserved bit Bit 1 is reserved; or	R/W* rved bits served; they is always re 7 IRRDT 0 R/W* rved bits served; only nly a write o	R/W* are always ead as 1 ar 6 IRRAD 0 R/W* a write of	= s read as 1 id cannot 5   W 0 is possib	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; it</u> (Correct) Bit Initial value Read/Write <u>Bits 5 and 4: Reser</u> <u>Bits 5 and 4 are res</u> <u>Bit 1: Reserved bit</u> <u>Bit 1 is reserved; or</u> Section 8 I/	R/W* rved bits served; they is always re 7 IRRDT 0 R/W* rved bits served; only nly a write o	R/W* are always ead as 1 ar 6 IRRAD 0 R/W* a write of	= s read as 1 id cannot 5   W 0 is possib	` <u>L and cann</u> be modifie <u>4</u>  <u>—</u> <u>W</u>	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*
Read/Write Bits 5 and 4: Reserved Bits 5 and 4 are reserved bit Bit 1: Reserved bit Bit 1 is reserved: it (Correct) Bit Initial value Read/Write Bits 5 and 4: Reserved Bit 1: Reserved bit Bit 1: Reserved bit Bit 1 is reserved; or Section 8 I/ 8.2 Port 3	R/W* rved bits served; they is always re 7 IRRDT 0 R/W* rved bits served; only nly a write o	R/W* are always ead as 1 ar 6 IRRAD 0 R/W* a write of f 0 is possi	= s read as 1 ad cannot 5 — — W 0 is possib ble.	` L and cann be modifie 4   W ble.	R/W* not be mod ed. 3 IRRTFH 0	R/W* ified. 2 IRRTFL 0		R/W*

(Incorrect)			
Name ·	Abbrev.	R/W Initial Value	Address
Port data register 3	PDR3,	R/W. <u>H'01</u> .	H'FFD6
Port control register 3	PCR3	W . <u>H'01</u> .	H'FFE6
Port pull-up control register 3	PUCR3	R/W <u>H'01</u>	H'FFE1
Port mode register 3	PMR3 .	R/W · <u>H'39</u>	H'FFCA

(Correct)

Name ,	Abbrev. ,	<b>R/W</b> .	Initial Value	Address .
Port data register 3 ,	PDR3 .	R/W ⋅	<u> </u>	H'FFD6 .
Port control register 3	PCR3	W .	<u> </u>	H'FFE6 .
Port pull-up control register 3	PUCR3 ·	R/W	<u> </u>	H'FFE1
Port mode register 3	PMR3 .	R/W.	<u> </u>	H'FFCA .

Section 8 I/O Ports ·

8.2 Port 3 ·

8.2.2 Register Configuration and Description'

1. Port data register 3 (PDR3) · · · · · · · (P130) ·

#### (Incorrect)

Bit .	7.	6.	5 .	4 ·	3.	2	1.	
	P37	P36 ·	P35	P34,	P33 ·	P32 ·	P31.	<u> </u>
Initial value ,	Ο.	0.	0 ·	0 -	Ο.	0.	0.	. 1
Read/Write '	R/W.	R/W	R/W ·	R/W	R/W	R/W	R/W ·	<b>—</b> .
PDR3 is an 8-bit reg	gister that s	stores data	1 for port 3	pins P37 t	o P31. If p	ort 3 is re	ad while P	CR3

bits are set to 1, the values stored in PDR3 are read, regardless of the actual pin states. If port 3 is read while PCR3 bits are cleared to 0, the pin states are read.

Upon reset; PDR3 is initialized to H'01.

#### (Correct)

Bit	7.	6 ·	5 ·	4 ·	3 ·	2 ,	1 .	0 .
	P37	P36	P35 ·	P34 ·	P33 ,	P32.	P31	—.
Initial value	0,	0,.	0.	0.	, Ο,	, O ·	, 0.,	Ξ.
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	, — ,

PDR3 is an 8-bit register that stores data for port 3 pins P37 to P31. If port 3 is read while PCR3 bits are set to 1, the values stored in PDR3 are read, regardless of the actual pin states. If port 3 is read while PCR3 bits are cleared to 0, the pin states are read.

Section 8 I/O Ports 8.2 Port 3 8.2.2 Register Configuration and Description -2. Port control register 3 (PCR3) ·····(P130) .

(Incorrect)								
Bit	7 .	6.	5.	<u>4 ·</u>	3 ·	2	1.	0
	PCR37	PCR36	PCR35	PCR34 ·	PCR33	PCR32	PCR31 .	
Initial value	0	0.	0.	0 -	0	0 -	0,	1.
Read/Write .	w .	W	w۰	w ·	W.	W.	W	_
	· . · . · ·		1 .1 . `	1 0.1		<b>D</b> O 1 DO		•

PCR3 is an 8-bit register for controlling whether each of the port 3 pins P37 to P31 functions as an input pin or output pin. Setting a PCR3 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR3 and in PDR3 are valid only when the corresponding pin is designated in PMR3 as a general I/O pin.

Upon reset, PCR3 is initialized to H'01.

PCR3 is a write only register, which is always read as all 1s.

#### (Correct)

Bit	7.	<u>6 ·</u>	5	4 .	3.	2 .	1 .	0
	PCR37·	PCR36	PCR35	PCR34	PCR33 ·	PCR32	PCR31	<u> </u>
Initial value .	0.	Ο.,	0.	0 -	0 -	0.	0	
Read/Write	W .	<b>W</b> ∗ .	W	W ·	W :	Ŵ-	W,	W

PCR3 is an 8-bit register for controlling whether each of the port 3 pins P37 to P31 functions as an input pin or output pin. Setting a PCR3 bit to 1 makes the corresponding pin an output pin, while . clearing the bit to 0 makes the pin an input pin. The settings in PCR3 and in PDR3 are valid only when the corresponding pin is designated in PMR3 as a general I/O pin.

PCR3 is a write-only register, and the bits 7 to 1 are read as all 1s.

Bit 0 is reserved; only a write of 0 is possible.

Section 8 I/O Ports . 8.2 Port 3 . 8.2.2 Register Configuration and Description 3, Port pull-up control register 3 (PUCR3) .....(P130),

#### (Incorrect)

Bit .	7.	6,	5.	4	3.	2 .	<u> </u>	0
	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	_
Initial value	ο.	ο.	0	0 .	0	• •	0 .	1
Read/Write	R/W .	R/W .	R/W·	R/W	R/W ·	R/W	<b>R/W</b> .	Ξ.
PUCR3 controls whe	ther the N	IOS pull-u	p of the p	ort 3 pins ]	P37 to P31	is on or of	f. When	
a PCR3 bit is cleared	l țo 0, setti	ing the cor	respondin	g PUCR3	bit to 1 tur	ns on the	MOS pull-	up for
the corresponding pi	n, while cl	earing the	bit to 0 ti	urns off the	e MOS pul	l-up.		
<u>Upon reset, PUCR3</u>	is initializ	ed to H'01.	Ł					
(Correct)								

#### Bit 7 -3 6 5 4 2 0. PUĈR37 PUCR35 PUCR36 PUCR34 PUCR33 PUCŔ32 PUCR31 Initial value, 0 0. 0 . 0 0 . 0 0 Ξ., **Read/Write** R/W R/W R/W R/W R/W R/W R/W <u>w</u>

PUCR3 controls whether the MOS pull-up of the port 3 pins P37 to P31 is on or off. Whena PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up. <u>Bit 0 is reserved</u>; only a write of 0 is possible.

#### (Incorrect) .

Bit +	7	6.	5	4	3,	2	1 •	0
	AEVL	AEVH ;	— "	-,	_,	TMOFH	TMOFL	,
Initial value	0 ·	0	1	1	1	0,	0.,	1
Read/Write	R/W	R/W	=.	<u> </u>	<u> </u>	R/W	R/W , ∙	_
PMR3 is an 8-bit re	ad/write re	gister, cont	rolling th	e selection	of pin fu	nctions for	port 3 pins	
Upon reset, PMR3'i	is initialized	ł to H'39.						

Bits 5 to 3: Reserved bits '

These bits are reserved; they are always read as 1 and cannot be modified.

Bit 0; Reserved bit

This bit is reserved; it is always read as 1 and cannot be modified.

#### (Correct)

Bit	7 ·	6 '	5	4	3	2 ·	1	0
•	AEVL ·	AEVH	<u> </u>	,	_ ,	TMOFH	TMOFL	
Initial value.	0,	0	=`·	=,	Ξ,	0 、	0 · .	= ,
Read/Write,	R/W	R/W	<u>W</u> .	W	<u>w</u> .	R/W	R/W	<u>w</u> .
PMR3 is an 8-bit re	ad/write re	gister, conti	rolling the	selection	ı of pin fu	inctions for p	ort 3 pins.	•
Bits 5 to 3: Reser	ved bits '							
<u>These bits are reser</u>	rved; only-a	write of 0 i	<u>s possible.</u>	•				
Bit 0: Reserved bit.								
This bit is reserved	<u>; only a wri</u>	te of 0 is po	<u>ssible:</u>					
Section 8 I/	O Ports <sup>.</sup>							
8.3 Port 4 ·								
8.3.2 Regist	er, Configur	ation and I	-					
Tabla 2 5 D	ort 4 Regist	ers	····(P	135)				
(incorrect)		`						
(Incorrect)		•	Abbrev.		R/W	Initial Value	e Ad	dress
(Incorrect) Name		•	Abbrev. PDR4+		<b>R/W</b> R/W	Initial Value		dress FD7-
		· · · · · · · · · · · · · · · · · · ·					H'F	<u>.</u>

			• • · · · · · · · · · · · · · · · · · ·				·
Name			Abbrev.		R/W	Initial Value	Address
Port data register 4			PDR4,		R/W .,	H'F8··	H'FFD7 ;
Port control register			PCR4 .		W .	H'F8	H'FFE7
Port mode register 2			PMR2	•	R/W .	<i>i</i>	H'FFC9
			Description ·····(F				
(Incorrect)		•					
Bit .	7、	6 ·	5	4.	3.	2、	1 0,
	<b>—</b> , <b>, (</b>	<b>—</b> ,.	POF1	- <u>,</u>	— <u>,</u>		IRQ0
Initial value ,	1,	1	0 +	1,.	1.,	1	1 0.
Read/Write		_	R/W,	<u> </u>	<b>—</b> .	<i>—</i> .	
PMR2 is an 8-bit re	ad/write reg	ister cont		selection	of the P4	3/IRQ0 pin fund	•
PMOS on/off state i			-				the and the
Bits 7, 6; and 4 to	•		pon room r				
Bits 7, 6, and 4 to 1			e always re	ad as 1 a	nd canno	t he modified	
Bit -	<u> </u>	<u>6</u> ·	5 · POF1 ·	<u>4</u> ·	3		$\frac{1}{-1}$ 0
Initial value	1 .	1.	0	1 .	1		<u> </u>
Initial value Read/Write	1 · ·	1 . — .	0 R/W	1 .	1 .	<u> </u>	
		<u> </u>	R/W	1  selectiofi			<u> </u>
Read/Write	ad/write regi	 ister contr	R/W	1 selectiofi			<u> </u>
Read/Write PMR2 is an 8-bit re	ad/write regi for the <u>P35</u> pi	– ister contr n.	R/W	1 .			<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f	ad/write regi for the <u>P35</u> pi 3: Reserved b	ister contr n. <u>its</u>	R/W		_ of the P4	3/IRQ0 pin func	<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f <u>Bits 7, 6, and 4, 3</u>	ead/write regi for the <u>P35</u> pi <u>3: Reserved b</u> re reserved; t	ister contr n. <u>its</u>	R/W		_ of the P4	3/IRQ0 pin func	<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f <u>Bits 7, 6, and 4, 3</u> <u>Bits 7, 6, and 4, 3 a</u>	ead/write regi for the <u>P35</u> pi 3: Reserved b re reserved; bits	 n. <u>its</u> they are a	R/W rolling the s always read		_ of the P4	3/IRQ0 pin func	<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f Bits 7, 6, and 4, 3 Bits 7, 6, and 4, 3 a Bits 2, 1: Reserved These bits are reserved Section 8 I/( 8.7 Port 8, 8.7.2 Regist	ead/write regi for the <u>P35</u> pi <u>3: Reserved b</u> <u>re reserved; to bits</u> <u>rved; only a v</u> O Ports	— ister contr n. <u>its</u> they are a vrite of 0 ; tion and 1	R/W rolling the s always read is possible.	<u>as 1 and</u>	_ of the P4	3/IRQ0 pin func	$\underline{-} \cdot \cdot 0 \cdot \underline{W} \cdot R/W$
Read/Write PMR2 is an 8-bit re PMOS on/off state f Bits 7, 6, and 4, 3 Bits 7, 6, and 4, 3 a Bits 2, 1: Reserved These bits are reser Section 8 I/( 8.7 Port 8, 8.7.2 Regist	ead/write regi for the <u>P35</u> pi <u>3: Reserved b</u> <u>re reserved; to bits</u> <u>rved; only a v</u> O Ports er Configura	— ister contr n. <u>its</u> they are a vrite of 0 ; tion and 1	R/W rolling the s always read is possible.	<u>as 1 and</u>	_ of the P4	3/IRQ0 pin func	<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f <u>Bits 7, 6, and 4, 3</u> <u>Bits 7, 6, and 4, 3 a</u> <u>Bits 2, 1: Reserved</u> <u>These bits are reser</u> Section 8 I/C 8.7 Port 8, 8.7.2 Regist Table 8.17 F (Incorrect). Name	ead/write regi for the <u>P35</u> pi <u>3: Reserved b</u> <u>re reserved; n</u> <u>bits</u> <u>rved; only a v</u> O Ports O Ports er Configura Port 8 Regist	— ister contr n. <u>its</u> they are a vrite of 0 ; tion and 1	R/W rolling the s always read is possible.	<u>as 1 and</u> 151) .	_ of the P4	3/IRQ0 pin func	<u> </u>
Read/Write PMR2 is an 8-bit re PMOS on/off state f <u>Bits 7, 6, and 4, 3</u> <u>Bits 7, 6, and 4, 3 a</u> <u>Bits 2, 1: Reserved</u> <u>These bits are reserved</u> Section 8 I/0 8.7 Port 8, 8.7.2 Regist Table 8.17 F	ead/write regi for the <u>P35</u> pi <u>3: Reserved b</u> <u>re reserved; n</u> <u>bits</u> <u>rved; only a v</u> O Ports O Ports er Configura Port 8 Regist	— ister contr n. <u>its</u> they are a vrite of 0 ; tion and 1	R/W rolling the s always read is possible. Description (P	<u>as 1 and</u> 151) .	 of the P4 Leannot I	3/IRQ0 pin fund	$=$ 0 $\cdot$ <u>W</u> R/W to $\cdot$

Name		Abbrev.	R/W	Initial Value	Address
Port data register 8	•	PDR8 ,	R/W.	<u> </u>	<sub>'</sub> H'FFDB
Port control register 8	3,	PCR8	W	•	H'FFEB
	) Ports er Configuration a register 8 (PDR8)		2)		
(Incorrect)					
Bit .	7, 6	. 5 .	4. 3	2	1 0
		· . —, _, _	_ ·   <u>, _</u>		- P80
Initial value	. <u>1</u> <u>1</u>	· <u>1</u> · · ·	<u>1</u> . <u>1</u>	• <u>1</u> •••	<u>1</u> 0,
Read/Write	<u> </u>	<u> </u>	-'		— . R/W
PDR8 is an 8-bit reg	ister that stores (	datá for port 8 pin	P80. If port	8 is read while I	PCR8 bits are
set to 1, the values s	tored in PDR8 ar	e read, regardless	of the actua	l pin states. If p	ort 8 is read
while PCR8 bits are	cleared to 0, the	pin states are read	<b>l</b> .		,
<u>Upon reset, PDR8 is</u>	<u>s'initialized to`H'</u>	<u>FE.</u> -			, ,
(Correct)					
Bit	7.6	5	4 - 3	. 2 -	1 0
			- · .   -		- P80.
Initial value	<u> </u>		<u>_·</u> _	· <u>-</u> ·	<u> </u>
Read/Write	— <u> </u>	. –	-'	·	—
PDR8 is an 8-bit regi	ister that stores o	lata for port 8 pin	P80. If port	8 is read while I	
		e read, regardless			
			-	- · · -	•••••••
while PCR8 bits are					
while PCR8 bits are Section 8 I/O					
while PCR8 bits are Section 8 I/O 8.7 Port 8	Ports.	and Description			
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Register		• –	2),	·	
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Register	) Ports. y Configuration a	• –	2),		
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro	) Ports. y Configuration a	• –	2),	2	1 0
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect)	) Ports. y Configuration a	• –	2), 4 <u>3</u> - –	2	1 0 — PCR86
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect)	) Ports. y Configuration a	28) ····· (P152	2), 4 . 3  1 1	<u> </u>	
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Register 2. Port contro (Incorrect) Bit	Ports. Configuration.a of register 8 (PCF 7 6 	28) ····· (P152	<u>4 . 3</u> 	<u> </u>	- · PCR80
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect) Bit Initial value Read/Write	Ports. Configuration.a of register 8 (PCF 7 6 7 6 1 1 = =	$ \begin{array}{c} 5 \\ - \\ - \\ 1 \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ -$	4 . <u>3</u> - , – 1 · 1 = · _	. <u> </u>	$ \begin{array}{c c} \hline - & PCR86 \\ \hline 1 & 0 \\ \hline - & W \end{array} $
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect) Bit Initial value Read/Write PCR8 is an 8-bit regi	Ports. Ports. Configuration a ol register 8 (PCF 7 6 7 6 1 1 1 1 = =	5         5         1         1         ag whether the port	4 . 3  1 1  it 8 pin P80	. <u> </u>	─ PCR80 1 0 · □ W input or output
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect) Bit Initial value Read/Write PCR8 is an 8-bit regi pin. Setting a PCR8 I	Ports. Ports. Configuration a ol register 8 (PCF 7 6 7 6 1 1 1 1 = = ister for controllin bit to 1 makes the	5         5         1         1         and whether the point         e corresponding pi	4 . 3 – 1 1 = – – t 8 pin P80 n an output	functions as an i pin, while clear	$\begin{array}{c c} - & PCR86 \\ 1 & 0 \\ - & W \\ \hline \\ \text{input or output} \\ \text{ing the bit to } 0 \end{array}$
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (Incorrect) Bit Initial value Read/Write PCR8 is an 8-bit regi	Ports. Ports. Configuration a ol register 8 (PCF 7 6 7 6 1 1 = = istêr for controllin bit to 1 makes the out pin. PCR8 and	5         1         1         ag whether the pore         corresponding pi         PDR8 settings and	4 . 3 – 1 1 = – – t 8 pin P80 n an output re valid whe	 functions as an i pin, while clear n the correspond	$\begin{array}{c c} - & PCR86 \\ 1 & 0 \\ - & W \\ \hline \\ \text{input or output} \\ \text{ing the bit to } 0 \end{array}$
while PCR8 bits are Section 8 I/O 8.7 Port 8 8.7.2 Registe 2. Port contro (incorrect) Bit Initial value Read/Write PCR8 is an 8-bit regi pin. Setting a PCR8 I makes the pin an inp	Ports. Configuration a of register 8 (PCF 7 6 7 6 1 1 1 1 = = ister for controllin bit to 1 makes the out pin. PCR8 and af-purpose input/	5         1         1         ag whether the porce         corresponding pi         1 PDR8 settings and         output by bits SG8	4 . 3 – 1 1 = – – t 8 pin P80 n an output re valid whe	 functions as an i pin, while clear n the correspond	$\begin{array}{c c} - & PCR86 \\ 1 & 0 \\ - & W \\ \hline \\ \text{input or output} \\ \text{ing the bit to } 0 \end{array}$

(Correct)								
Bit	7	6	5	4	3	2	1	0
		—	—		· _			PCR80
Initial value	_		=	=	=	<u> </u>	=	• 0
Read/Write	W	W	W	W	W	W	W	W
PCR8 is an 8-bit re							=	-
pin. Setting a PCR							-	
makes the pin an i						-	onding pi	ins are
designated for gene					SGS0 in I	LPCR.		
PCR8 is a write-on	<u>ly register, a</u>	nd the bi	<u>t 0 is read</u>	<u>as 1.</u>				
Bits 7 to 1 are rese	rved; only a	<u>write of 0</u>	is possibl	<u>e.</u>				
Section 8 I/ 8.8 Port 9	O Ports							
	ter Configura	ation and	Descriptio	on				
Table 8.20	Port 9 Regist	ters	• • • • • •	(P154)				
(incorrect)								
Name			Abbre	v.	R/W	Initial Va	lue	Address
Port data register 9			PDR9		R/W	H'FF		H'FFDC
	)		PDR9 PMR9		R/W R/W	H'FF <u>H'F4</u>		H'FFDC H'FFEC
Port mode register 9 (Correct) Name	)		PMR9		R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC
Port mode register 9 (Correct) Name Port data register 9			PMR9 Abbre PDR9	v.	R/W R/W R/W	<u>H'F4</u>	lue	H'FFEC Address H'FFDC
Port mode register 9 (Correct) Name Port data register 9			PMR9	v.	R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9		· · · · · · · · · · · · · · · · · · ·	PMR9 Abbre PDR9	v.	R/W R/W R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC Address H'FFDC
Port mode register 9 (Correct) Name Port data register 9			PMR9 Abbre PDR9	v.	R/W R/W R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC Address H'FFDC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Register	O Ports ter Configura		PMR9 Abbre PDR9 PMR9 Descriptio	v	R/W R/W R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC Address H'FFDC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regiss 2. Port mod	O Ports		PMR9 Abbre PDR9 PMR9	v	R/W R/W R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC Address H'FFDC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mode (Incorrect)	O Ports ter Configura	(PMR9)	PMR9 Abbre PDR9 PMR9	v. on (P155)	R/W R/W R/W	H'F4 Inifial Va H'FF =	lue	H'FFEC Address H'FFDC H'FFEC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regiss 2. Port mod	O Ports ter Configura		PMR9 Abbre PDR9 PMR9 Descriptio	v	R/W R/W R/W	<u>H'F4</u> Inifial Va	lue	H'FFEC Address H'FFDC H'FFEC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 	PMR9 Abbre PDR9 PMR9 Descriptio	v. on (P155) 4 	R/W R/W R/W 3 PIOFF	H'F4 Inifial Va H'FF =	lue	H'FFEC Address H'FFDC H'FFEC
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value	O Ports ter Configura	(PMR9)	PMR9 Abbre PDR9 PMR9	v. on (P155)	R/W R/W R/W 3 PIOFF 0	H'F4 Inifial Va H'FF =	1 1 PWM2 0	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0
Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regis 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W
Port mode register 9 (Correct) Name Port data register 9 Port mode register 9 Section 8 I/ 8.8 Port 9 8.8.2 Regist 2. Port mod (Incorrect) Bit Initial value Read/Write	O Ports ter Configura le register 9 ( 7 	(PMR9) 6 — 1 —	PMR9 Abbre PDR9 PMR9 Descriptio	v. (P155) 4 1 -	R/W R/W R/W 3 PIOFF 0 R/W	<u>H'F4</u> Initial Va H'FF = 2 1  1	lue 1 PWM2 0 R/W	H'FFEC Address H'FFDC H'FFEC 0 PWM1 0 R/W

(Correct)Bit $\overline{7}$ $\overline{6}$ $\overline{5}$ $4$ $3$ $2$ $1$ $0$ Initial value1111 $0$ $\equiv$ $0$ $0$ Read/Write $1$ 111 $0$ $\equiv$ $0$ $0$ Read/Write $   -$	<u></u>									
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	(Correct)									
Initial value1110 $\equiv$ 00Read/WriteR/WWR/WR/WPMR9 is an 8-bit read/write register controlling the selection of the P30 and P32 pin functions.Bit 2: Reserved bitThis bit is reserved: only a write of 0 is possible.Section 8 I/O Ports8.11 Input/Output Data Inversion Function8.11 Input/Output Data Inversion Function8.11 Register ConfigurationTable 8.28 Register Configuration	Bit	7	6	5	4	. 3	2		0	
Read/WriteR/WWR/WR/WPMR9 is an 8-bit read/write register controlling the selection of the P90 and P32 pin functions.Bit 2: Reserved bitThis bit is reserved: only a write of 0 is possible.Section 8 I/O Ports8.11 Input/Output Data Inversion Function8.112 Register Configuration and DescriptionTable 5.28 Register ConfigurationTable 5.28 Register Configuration(P164, P165)(Incorrect)Bit76547678.112 Register Configuration9.11<		<u> </u>	<u> </u>	<b>—</b> .	<u> </u>	PIOFF	·_!	PWM2	PWM1	
PMR9 is an 8-bit read/write register controlling the selection of the P90 and P92 pin functions.         Bit 2: Reserved bit         This bit is reserved: only a write of 0 is possible.         Section 8 I/O Ports         8.11 Input/Output Data Inversion Function         8.11 Input/Output Data Inversion Function         8.11 Input/Output Data Inversion Function         8.11 Register Configuration and Description         Table 8.28 Register Configuration         Incorect)         Bit       7         6       5       4       3       2       1       0         Initial value       1       0       1       0       0       1       1         Read/Write       -       -       R/W       R/W       =       =       SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data         inversion switching.       SPCR is an 8-bit readable/writable register data 1 and cannot be modified.       Bit 4 is reserved bits         Bit 1 and 0: Reserved bits       Bit 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)       Bit       7       6       5       4       3       2       1       0         Bit 1 and 0: Reserved bits       Bit 1 and 0 are reserved: tha performs RXD32 and TXD32 pin input/output	Initial value	1	1 、	1	1	0	<b>—</b> ,	0	0	
Bit 2: Reserved bit         This bit is reserved: only a write of 0 is possible.         Section 8 I/O Ports         8.11 Input/Output Data Inversion Function         Sili Input/Output Data Inversion Function         Sili Input/Output Data Inversion Function         Sili Provide State Configuration and Description         Table 8.28 Register Configuration         Table 8.28 Register Configuration         This all 2 on 0         Table 8.28 Register Configuration         SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data         inversion switching. SPCR is an 8-bit readable/writable register can be modified.         Bit 1 and 0. Reserved bits         Bit 1 and 0 are reserved: they are always read as 1 and cannot be modified.         Correct)         Bit 1 1 0 = 0 0 = =         R/W W R/W R/W W W <th cols<="" td=""><td>Read/Write</td><td></td><td><u> </u></td><td></td><td></td><td>R/W</td><td>W</td><td>R/W</td><td>R/W</td></th>	<td>Read/Write</td> <td></td> <td><u> </u></td> <td></td> <td></td> <td>R/W</td> <td>W</td> <td>R/W</td> <td>R/W</td>	Read/Write		<u> </u>			R/W	W	R/W	R/W
This bit is reserved: only a write of 0 is possible Section 8 I/O Ports 8.11 Input/Output Data Inversion Function 8.11.2 Register Configuration and Description Table 8.28 Register Configuration $\cdots (P164, P165)$ (Incorrect) Bit 7 6 7 6 5 4 3 2 1 0 1 Read/Write 7 7 7 7 8 7 7 7 7 7 8 7 8 7 8 7 8 8 7 7 7 8 8 7 8 8 7 8	PMR9 is an 8-bit rea	ad/write reg	<u>gister con</u> f	trolling the	selectior	<u>n of the P9(</u>	<u>o and P92 r</u>	<u>oin functio</u>	<u>ons.</u>	
Section 8 I/O Ports 8.11 Input/Output Data Inversion Function 8.112 Register Configuration and Description Table 8.28 Register Configuration $\cdots$ (P164, P165) (Incorrect) Bit $7$ 6 5 4 3 2 1 0 - SPC32 - SCINV3 SCINV2 Initial value 1 1 0 1 0 0 1 1 Read/Write R/W = R/W R/W = - SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset. Bit 4: Reserved bit Bit 4 is reserved: this is always read as 1 and cannot be modified. Bits 1 and 0: Reserved bits Bits 1 and 0: Reserved bits Bit 7 6 5 4 3 2 1 0 - - SPC32 - SCINV3 SCINV2 Initial value 1 1 0 = 0 0 = = Read/Write R/W W R/W W W W SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset. Bit 4 is reserved: they are always read as 1 and cannot be modified. Eits 1 and 0: Reserved bits Bits 1 and 0: Reserved bits Bit 1 and 0 are reserved: they are always read as 1 and cannot be modified. SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. Bit 4 is reserved int Bit 1 and 0: Reserved bits Bits 1 and 0 are reserved: only a write of 0 is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration	Bit 2: Reserved bit									
8.11 Input/Output Data Inversion Function 8.11.2 Register Configuration and Description Table 8.28 Register Configuration $\cdots (P164, P165)$ (Incorrect) Bit $7 6 5 4 3 2 1 0$ SPC32 SCINV3 SCINV2 Initial value 1 1 0 1 0 0 1 1 0 0 1 1 ReadWrite $ RW - RW - RW$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to HTD3 by a reset. Bit 4: Reserved bit Bit 4 is reserved: this is always read as 1 and cannot be modified. Bits 1 and 0: Reserved bits Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified. (Correct) Bit $7 6 5 4 3 2 1 0$ SPC32 - SCINV3 SCINV2 Initial value 1 1 0 $= 0 0 0 = -$ ReadWrite $ RW W RW RW W W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching Bit 4 is reserved: they are always read as 1 and cannot be modified. Elis 1 and 0 are reserved: they are always read as 1 and cannot be modified. Bit 7 6 5 4 3 2 1 0 RW W RW RW W W SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching Bit 4 is reserved. bit Bit 4 is reserved. In 1 0 $= 0 0 0 = -$ ReadWrite $ RW W RW RW W W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching Bit 4 Reserved bit Bit 4 is reserved. In 1 $0$ is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration	This bit is reserved;	<u>only a writ</u>	<u>æ of 0 is p</u>	ossible.						
Bit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ Initial value11010011Read/Write $  RW$ $RW$ $RW$ $=$ $=$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output datainversion switching. SPCR is initialized to H'D3 by a reset.Bit 4: Reserved bitBit 4 is reserved: this is always read as 1 and cannot be modified.Bits 1 and 0: Reserved bitsBits 1 and 0 are reserved: they are always read as 1 and cannot be modified.(Correct)Bit $7$ $6$ $5$ $4$ $3$ $2$ $0$ Initial value11 $0$ $=$ $0$ $0$ $=$ $=$ Initial value11 $0$ $=$ $0$ $0$ $=$ $=$ Read/Write $  R/W$ $W$ $R/W$ $W$ $W$ $W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output datainversion switching.Bit 4 is reserved bitBit 4 is reserved bitBit 4 is reserved bitsBits 1 and 0: Reserved bitsBits 1 and 0: Reserved bitsBits 1 and 0: Reserved bitsSection 9 Timers9.2 Timer A9.2.1 Overview3. Register configuration	8.11 Input/O 8.11.2 Regist Table 8.28 R	Output Data Iter Configu	ration and	d Descriptio	on	65)	,			
$  SPC32$ $ SCINV3$ $SCINV2$ $ -$ Initial value11010011Read/Write $  R/W$ $\equiv$ $R/W$ $\equiv$ $\equiv$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output datainversion switching. SPCR is initialized to H'D3 by a reset.Bit 4: Reserved bitBit 4 is reserved: this is always read as 1 and cannot be modified.Bits 1 and 0: Reserved bitsBit 1 and 0: Reserved bitsBit $7$ $6$ $5$ $4$ $3$ $2$ $0$ $  SPC32$ $ SCINV3$ $SCINV2$ $ -$ Initial value11 $0$ $=$ $0$ $0$ $=$ $=$ Read/Write $  R/W$ $W$ $R/W$ $W$ $W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output datainversion switching. $Bit 4$ is reserved bitBit 4 is reserved bit $Bit 4$ is reserved bitBit 4 is reserved bitBit 1 and 0: Reserved bitsBits 1 and 0: Reserved bitsBits 1 and 0 are reserved only a write of 0 is possible.Section 9 Timers9.2 Timer A9.2.1 Overview3. Register configuration	(Incorrect)									
Initial value11010011Read/WriteR/W-R/WSPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to HTD3 by a resetBit 4 Reserved bit	Bit	7	6	5	4	3	2	1	0	
Read/Write       -       -       R/W       =       R/W       R/W       =       =         SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset.       Bit 4: Reserved bit         Bit 4: Reserved bit       Bit 4 is reserved: this is always read as 1 and cannot be modified.       Bits 1 and 0: Reserved bits         Bit 1 and 0: Reserved: they are always read as 1 and cannot be modified.       (Correct)         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       0       =       0       0       =       =         Initial value       1       1       0       =       0       0       =       =         Initial value       1       1       0       =       0       0       =       =         Read/Write       -       -       R/W       W       W       W       SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching.       Bit 4 is reserved bit       Eit 4 is reserved bit       Eit 1 and 0: Reserved bits         Bits 1 and 0 are reserved: only a write of 0 is possible.       Section 9 Timers       9.2 Timer A       9.2.1 Overview       3. R		—,		SPC32	,	SCINV3	SCINV2	<u> </u>		
SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data         inversion switching. SPCR is initialized to HD3 by a reset.         Bit 4: Reserved bit         Bit 4 is reserved: this is always read as 1 and cannot be modified.         Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       0 $=$ 0 $=$ $=$ Initial value       1       1       0 $=$ 0       0 $=$ $=$ Read/Write $=$ $=$ $R/W$ $W$ $W$ $W$ $W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data       inversion switching. $W$ $W$ Bit 4: Reserved bit $B$	Initial value	1	1	0.	<u>1</u> ,	0,	0	1	<u>1</u> ·	
inversion switching. SPCR is initialized to HD3 by a reset. Bit 4: Reserved bit Bit 4 is reserved: this is always read as 1 and cannot be modified. Bits 1 and 0: Reserved bits Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified. (Correct) Bit $7   6   5   4   3   2   1   0$ $\overline{-}     SPC32   -   SCINV3   SCINV2    }$ Initial value 1 1 0 $\equiv   0   0   =   =.$ Read/Write $-     R/W   W   R/W   R/W   W   W$ SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. Bit 4: Reserved bit Bit 4: Reserved bit Bits 1 and 0: Reserved: only a write of 0 is possible. Bits 1 and 0: Reserved: only a write of 0 is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration	Read/Write	—,	<del></del> ,	R/W	<u> </u>	R/W	R/W	=	=	
Bit 4: Reserved bit         Bit 1 is reserved: this is always read as 1 and cannot be modified.         Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       0 $=$ 0       0 $=$ $=$ Initial value       1       1       0 $=$ 0       0 $=$ $=$ Read/Write $=$ $=$ R/W       W       R/W       W       W         SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data       inversion switching	SPCR is an 8-bit rea	<u>idable/writ</u> a	<u>ible regis</u> t	<u>ter that per</u>	<u>:forms R)</u>	<u>XD32 and T</u>	<u>'XD32 pin i</u>	input/outp	ut data	
Bit 4 is reserved: this is always read as 1 and cannot be modified.         Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       0       =       0       0       =       =       .         Initial value       1       1       0       =       0       0       =       =       .         Read/Write       -       -       R/W       W       R/W       W       W       W         SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching.	inversion switching.	<u>SPCR is in</u>	<u>iitialized (</u>	to H'D3 by	<u>a reset.</u>					
Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)         Bit       7       6       5       4       3       2       1       0	Bit 4: Reserved bit									
Bits 1 and 0 are reserved: they are always read as 1 and cannot be modified.         (Correct)         Bit       7       6       5       4       3       2       1       0	Bit 4 is reserved; thi	<u>is is always</u>	, read as 1	and canno	<u>ot be mod</u>	ified.				
(Correct) Bit 7 6 5 4 3 2 1 0 	Bits 1 and 0: Reserv	ved bits								
Bit       7       6       5       4       3       2       1       0	Bits 1 and 0 are rese	erved; they	<u>are alway</u>	<u>/s read as 1</u>	and can	<u>not be mod</u>	lified.			
Bit       7       6       5       4       3       2       1       0										
SPC32        SCINV3       SCINV2           Initial value       1       1       0	(Correct)									
Initial value 1 1 0 = 0 0 = = Read/Write R/W W R/W R/W W W SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. Bit 4: Reserved bit Bit 4 is reserved: only a write of 0 is possible. Bits 1 and 0: Reserved bits Bits 1 and 0 are reserved: only a write of 0 is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration	Bit	7	6	5	4	3	2	1	0	
Read/Write       -       R/W       W       R/W       W       W         SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data         inversion switching.         Bit 4: Reserved bit         Bit 4 is reserved: only a write of 0 is possible.         Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved: only a write of 0 is possible.         Section 9 Timers         9.2 Timer A         9.2.1 Overview         3. Register configuration	I	<u> </u>		SPC32		SCINV3	SCINV2	<u> </u>	<u> </u>	
SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data         inversion switching.         Bit 4: Reserved bit         Bit 4 is reserved; only a write of 0 is possible.         Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved; only a write of 0 is possible.         Section 9 Timers         9.2 Timer A         9.2.1 Overview         3. Register configuration	Initial value	1	1	0	Ξ	0	0	=	=	
SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching	Read/Write		`	R/W	W	R/W	R/W	<u>W</u>	W	
inversion switching. <u>Bit 4: Reserved bit</u> <u>Bit 4 is reserved: only a write of 0 is possible.</u> <u>Bits 1 and 0: Reserved bits</u> <u>Bits 1 and 0 are reserved: only a write of 0 is possible.</u> Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration	<u>SPCR is an 8-bit rea</u>		a <u>ble regis</u> t							
Bit 4: Reserved bit         Bit 4 is reserved: only a write of 0 is possible.         Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved; only a write of 0 is possible.         Section 9 Timers         9.2 Timer A         9.2.1 Overview         3. Register configuration								_ <b>_</b>		
Bit 4 is reserved: only a write of 0 is possible. Bits 1 and 0: Reserved bits Bits 1 and 0 are reserved; only a write of 0 is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration										
Bits 1 and 0: Reserved bits         Bits 1 and 0 are reserved; only a write of 0 is possible.         Section 9 Timers         9.2 Timer A         9.2.1 Overview         3. Register configuration			f 0 is poss	ible.						
Bits 1 and 0 are reserved; only a write of 0 is possible. Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration		•	<u> </u>	<u>emory</u>						
Section 9 Timers 9.2 Timer A 9.2.1 Overview 3. Register configuration			a write of	'0 is nossib'	ما					
9.2 Timer A 9.2.1 Overview 3. Register configuration	L100 1 mm	i vou ver	<u>A_112200</u>	0 10 10000	16.					
9.2 Timer A 9.2.1 Overview 3. Register configuration	Section 9 Tir	mers								
3. Register configuration	9.2 Timer A									
Table 9.2 Timer A Registers ·····(r170)	. –	-			<u>הייס</u> וים)					
	1 abie <i>3.4</i> 1 m	ner A regis	iters	/1	2170)					
							,			

Name			Abbrev	<b>v</b> .	R/W	Initial Val	ve	Address
Timer mode register .	A		TMA		R/W	<u>H'F0</u>		H'FFB0
Fimer counter A			TCA		R	H'00	,,	H'FFB1
Clock stop register 1		i	CKSTF	PR1	R/W	H'FF		H'FFFA
						· · · · · · · · · · · · · · · · · · ·		_
(Correct)								
Name			Abbrev	v	R/W	Initial Val	ve	Address
Timer mode register	A	×	TMA		R/W	<u> </u>		H'FFB0
Timer counter A			TCA		R	H'00		H'FFB1
Clock stop register 1			CKSTF	PR1	R/W	H'FF		H'FFFA
Section 9 Ti 9.2 Timer A 9.2.2 Regista 1. Timer mo	er Descript		••••••(	(P1 <b>7</b> 0)				
(Incorrect)								
Bit	7	6	5	4	. 3	2	1	0
				_	TMA3	TMA2	TMA1	TMA0
					0	0	0	0
Initial value	<u>1</u>	1	1	1			-	_
Read/Write	_	=	=	_	R/W	R/W	R/W	R/W
Read/Write TMA is an 8-bit read	 d/write reg	 gister for se	=	_	R/W	R/W	-	_
Read/Write TMA is an 8-bit read Upon reset, TMA is	 d/write reg initialized	 gister for se	=	_	R/W	R/W	-	_
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u>	 d/write reg <u>initialized</u> red bits	 rister for se <u>to H'F0.</u>	 electing the	— e prescale	R/W er, and ing	R/W ut clock.	-	_
Read/Write TMA is an 8-bit read Upon reset, TMA is	 d/write reg <u>initialized</u> red bits	 rister for se <u>to H'F0.</u>	 electing the	— e prescale	R/W er, and ing	R/W ut clock.	-	_
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u>	 d/write reg <u>initialized</u> red bits	 rister for se <u>to H'F0.</u>	 electing the	— e prescale	R/W er, and ing	R/W ut clock.	-	_
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u> (Correct)	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u>	 gister for se <u>to H'F0.</u> are always	electing the	— e prescale and canne	R/W er, and ing ot be modi	R/W out clock. <u>fied.</u>	R/W	R/W
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u>	 d/write reg <u>initialized</u> red bits	 rister for se <u>to H'F0.</u>	 electing the	— e prescale	R/W er, and inp ot be modi 3	R/W out clock. fied. 2	R/W	R/W
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u> (Correct) Bit	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u>	 gister for se <u>to H'F0.</u> are always	electing the	e prescale and canno 4 4	R/W er, and inp ot be modi 3 TMA3	R/W out clock. fied. 2 TMA2	R/W 1 TMA1	R/W 0 TMA0
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u> (Correct) Bit Initial value	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u> 	cister for se to H'FO. are always 6 	 electing the <u>read as 1 a</u> 	— e prescale and canne	R/W er, and inp ot be modi 3 TMA3 0	R/W out clock. fied. 2 TMA2 0	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reserv</u> <u>Bits 7 to 4 are reser</u> (Correct) Bit Initial value Read/Write	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved: they a</u> 7  <u>7</u>  <u>7</u>  <u>W</u>	cister for se to H'FO. are always 6  <u>W</u>	Electing the read as 1 a 5 	e prescale and canne 4 1 -	R/W er, and inp ot be modi 3 TMA3 0 R/W	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1	R/W 0 TMA0
Read/Write TMA is an 8-bit read <u>Upon reset, TMA is</u> <u>Bits 7 to 4: Reservent</u> Bits 7 to 4 are reservent (Correct) Bit Initial value Read/Write TMA is an 8-bit read	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u>	cister for se to H'FO. are always 6  <u>W</u>	Electing the read as 1 a 5 	e prescale and canne 4 1 -	R/W er, and inp ot be modi 3 TMA3 0 R/W	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is <u>Bits 7 to 4: Reserve</u> Bits 7 to 4 are reserve (Correct) Bit Initial value Read/Write TMA is an 8-bit read <u>Bits 7 to 5: Reserve</u>	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u>	cister for se to H'FO. are always 6 6 <u>W</u> gister for se	$\frac{-}{-}$ electing the $\frac{1}{5}$ $\frac{5}{-}$ $\frac{W}{-}$ electing the	e prescale and canno 4 1 - e prescale	R/W er, and inp ot be modi 3 TMA3 0 R/W	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is <u>Bits 7 to 4: Reserv</u> Bits 7 to 4 are reserv (Correct) Bit Initial value Read/Write TMA is an 8-bit read <u>Bits 7 to 5: Reserv</u> Bits 7 to 5 are reservent	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>7</u> <u>8</u> <u>7</u> <u>8</u> <u>7</u> <u>8</u> <u>7</u> <u>8</u> <u>7</u> <u>8</u> <u>7</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u> <u>8</u>	cister for se to H'FO. are always 6 6 <u>W</u> gister for se	electing the $read as 1 a$ 5 - W	e prescale and canno 4 1 - e prescale	R/W er, and inp ot be modi 3 TMA3 0 R/W	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is Bits 7 to 4: Reserve Bits 7 to 4 are reserve (Correct) Bit Initial value Read/Write TMA is an 8-bit read Bits 7 to 5: Reserve Bits 7 to 5 are reserve Bit 4: Reserved bit	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u>      	fister for se to H'FO. are always 6 — — — — W gister for se	electing the read as 1 a 5 - W electing the is possible	e prescale and canno 4 1 - e prescale	R/W er, and inp ot be modi 3 TMA3 0 R/W er, and inp	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is <u>Bits 7 to 4: Reserv</u> Bits 7 to 4 are reserv (Correct) Bit Initial value Read/Write TMA is an 8-bit read <u>Bits 7 to 5: Reserv</u> Bits 7 to 5 are reservent	 d/write reg <u>initialized</u> <u>red bits</u> <u>ved; they a</u>      	fister for se to H'FO. are always 6 — — — — W gister for se	electing the read as 1 a 5 - W electing the is possible	e prescale and canno 4 1 - e prescale	R/W er, and inp ot be modi 3 TMA3 0 R/W er, and inp	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is Bits 7 to 4: Reserve Bits 7 to 4 are reserve (Correct) Bit Initial value Read/Write TMA is an 8-bit read Bits 7 to 5: Reserve Bits 7 to 5 are reserve Bit 4: Reserved bit	<pre> d/write reg initialized red bits ved; they a 7 7 7 4 4 w d/write reg red bits ved; only a is is alway </pre>	cister for se to H'FO. are always 6 6 — — — W gister for se a write of 0 rs read as 1	electing the read as 1 a 5   electing the is possible and canne	e prescale and canno 4 1 - e prescale e. ot be mod	R/W er, and inp ot be modi 3 TMA3 0 R/W er, and inp	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is <u>Bits 7 to 4: Reserve</u> Bits 7 to 4 are reserved (Correct) Bit Initial value Read/Write TMA is an 8-bit read <u>Bits 7 to 5: Reserve</u> Bits 7 to 5 are reserved Bit 4: Reserved bit Bit 4 is reserved: the Section 10 S 10.1 Overvier	d/write reg initialized red bits ved; they a 7 7 2 3 4 4 4 4 4 4 4 4 4 4 5 5 5 5 5 5 5 5 5	cister for se to H'FO. are always 6 — — <u>W</u> gister for se a write of 0 rs read as 1 munication	electing the read as 1 a 5   electing the is possible and canne	e prescale and canno 4 1 - e prescale e. ot be mod	R/W er, and inp ot be modi 3 TMA3 0 R/W er, and inp	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0
Read/Write TMA is an 8-bit read Upon reset, TMA is Bits 7 to 4: Reserve Bits 7 to 4 are reserve (Correct) Bit Initial value Read/Write TMA is an 8-bit read Bits 7 to 5: Reserve Bits 7 to 5 are reserve Bits 7 to 5 are reserve Bit 4: Reserved bit Bit 4 is reserved; the Section 10 S	d/write reg initialized red bits ved; they a ved; they a	cister for se to H'FO. are always 6 6 — — <u>W</u> gister for se a write of 0 as read as 1 munication aration	electing the read as 1 a 5   electing the is possible and canne	e prescale and canno 4 1 - e prescale e. ot be mod	R/W er, and inp ot be modi 3 TMA3 0 R/W er, and inp	R/W out clock. fied. 2 TMA2 0 R/W	R/W 1 TMA1 0	R/W 0 TMA0 0

(Incorrect)				
Name ,	Abbrev.	R/W ·	Initial Value ,	Address
Serial mode register	SMR .	R/W.	H'00.	H'FFA8.
Bit rate register.	BRR.	R/W	H'FF.	H'FFA9
Serial control register 3.	SCR3 <sup>-</sup>	R/W .	H'00 ·	H'FFAA
Transmiț dața register	TDR.	R/W .	H'FF ·	H'FFAB
Serial status register	SSR.	R/W ·	H'84	H'FFAC
Receive data register	RDR	R .	H'00 ·	H'FFAD
Transmit shift register	TSR.	Protected	,	<b>—</b> .
Receive shift register	RSR .	Protected	— ,	-
Bit rate counter ,	BRÇ	Protected .	<u> </u>	<u> </u>
Clock stop register 1 ,	CKSTPR1	R/W	H'FF	H'FFFA
Serial port control register •	SPCR .	R/W 、	<u>H'C0</u> .	H'FF91

#### (Correct)

Name	Abbrev.	R/W	Initial Value	Address
Serial mode register	SMR ·	R/W.	H'00 .	H'FFA8
Bit rate register	BRR .	R/W .	H'FF	H'FFA9
Serial control register 3	SCR3 ·	R/W ·	H'00 .	H'FFAA
Transmit data register	TDR ·	R/W ·	H'FF ,	H'FFAB
Serial status register	SSR ·	R/W	H'84	H'FFAC
Receive data register	RDR '	R	H'00 ·	H'FFAD
Transmit shift register	TSR	Protected	<u> </u>	— <u>,</u>
Receive shift register -	RSR .	Protected	· — ·	
Bit rate counter .	BRC.	Protected .		— 、
Clock stop register 1	CKSTPR1.	R/W	H'FF ·	H'FFFA
Serial port control register	SPCR	R/W	· <u> </u>	H'FF91

Section 10'Serial Communication Interface.

10.1 Overview .

10.1.4 Register configuration

Table 10.2 Registers ......(P235),

#### (Incorrect)

Bit	7 .	6.	5 •	4	3、	2 •	1.	0 .
	·		SPC32 ·	—	SCINV3.	SCINV2		
Initial value	1 ·	1 ,	0 .	1	0	0	<u>1</u>	<u>1</u> .
Read/Write	—.	<del>.</del>	R/W	= [	R/W	R/W .	Ξ.	· <u> </u>

SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset.

Bits 7, 6, 4, 1, and 0: Reserved bits.

Bits 7 and 6 are reserved; they are always read as 1 and cannot be modified.

inversion switching		7	6	5	4	3	2		0
Read/Write       -       -       RW       W       RW       W       W       W         SPCR is an 8-bit readable/writable register that performs RXDs2 and TXDs2 pin input/output data inversion switching       Bits 7 and 6: Reserved bits         Bits 7 and 6: Reserved bits       Bits 7 and 6: Reserved bits         Bits 4. 1. and 0: are reserved: only a write of 0 is possible.         Section 12 A/D Converter         12.2 Register Descriptions         12.2 A/D Mode Register (AMR)         (Incorrect)         Bit       7       6       5       4       3       2       1       0         (Incorrect)       Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W $=$ -       R/W       R/W       R/W         Upon reset, AMR is initialized to H'30.       Bit 6: Reserved bit       Bit 6: Reserved bit, but should not be modified as this may cause erroneous operation.         (Correct),       Bit       7       6       5       4       3       2       1       0         Bit 6: Reserved bit       Ets the adverte register for specifying th		<u>-</u>		SPC32·		SCINV3	SCINV2	<del>.</del> ,	·
SPCR is an 8-bit readable/writable register that performs RXDs2 and TXDs2 pin input/output data inversion switching Bits 7 and 6 Reserved bits Bits 7 and 6 are reserved: they are always read as 1 and cannot be modified. Bits 4.1. and 0 are reserved: only a write of 0 is possible. Section 12 A/D Converter . 12.2 Register Descriptions 12.2 A/D Mode Register (AMR)(P280, P281) . (Incornect) Bit 7 6 5 4 3 2 1 0 CKS CH3 CH2 CH1 CH0 Initial value 0 0, 1, 1, 0, 0 0 0 ReadWrite R/W = R/W R/W E/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger ' option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6 is a readable/write able reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit 7 6 5 4 3 2 1 0 CKS R/W R/W R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger ' option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct). Bit 7 6 5 4 3 2 1 0. $CKS CH3 CH3 CH2 CH1 CH0Initial value 0 0 1 1 0 0 0 0ReadWrite R/W R/W R/W R/W R/W R/WAMR is an 8-bit read/write register for 'specifying the A/D conversion speed, external triggeroption, and the analog input pins.Upon reset, AMR is initialized to H'30.Bit 6: Reserved bitThis bit is reserved. Adm R is this bit to 1.Section 13 LCD Controller/Driver '13.2 Register Descriptions .$	Initial value	1	1.	0 •	Ξ,	0.	0.	Ξ.	Ξ.
Bits 7 and 6 are 'reserved if hey' are always read as 1 and cannot be modified. Bits 4. 1. and 0: Reserved bits Bits 4. 1. and 0: Reserved bits Bits 4. 1. and 0 are reserved: only a write of 0 is possible. Section 12 A/D Converter . 12.2 Register Descriptions . 12.2.2 A/D Mode Register (AMR)(P280, P281) . (Incorrect) Bit 7 6 5 4 3 2 1 0 CKS $         -$	Read/Write	, —		R/W	W	R/W	R/W ·	W	W
Bits 7 and 6: Reserved bits Bits 7 and 6 are reserved: they are always read as 1 and cannot be modified. Bits 4. 1, and 0: Reserved bits Bits 4. 1, and 0 are reserved: only a write of 0 is possible. Section 12 A/D Converter 12.2 Register Descriptions 12.2.2 A/D Mode Register (AMR)(P280, P281) . (Incorrect) Bit $7 6 5 4 3 2 1 0$ CKS CH3 CH2 - CH1 CH0 Initial value 0, 0, 1. 1. 0 0 0 0 0 Read/Write R/W = - R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit $7 6 5 4 3 2 1 0$ CKS R/W R/W R/W R/W R/W R/W Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous opteration. (Correct), Bit $7 6 5 4 3 2 1 0$ CKS R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6: is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct), Bit $7 6 5 4 3 2 1 0$ CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 1 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is 'mitialized to H'30. Bit 6: Reserved bit This bit is reserved. do not set this bit to 1. Section 13 LCD Controller/Driver 13 2 Register Descriptions	<u>SPCR is an 8-bit re</u>	adable/writal	<u>ole regist</u>	ter that perf	orms RX	D32 and T	<u>XD32 pin i</u> 1	<u>nput/outpu</u>	it data
Bits 4. 1, and 0: Reserved bits         Bits 4. 1, and 0 are reserved: only a write of 0 is possible.         Section 12 A/D Converter .         12.2 Register Descriptions .       12.2.2 A/D Mode Register (AMR)(P280, P281) .         (Incorrect)         Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0       0       0       0         Rike 7       6       5       4       3       2       1       CH0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W       =       -       -       R/W       R/W       R/W       R/W         ADD on reset, AMR is initialized to H'30.       Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.       CKS       -       -       -       0	inversion switching	<u> </u>							
12.2 Register Descriptions         12.2.2 A/D Mode Register (AMR)         (P280, P281)         (Incorrect)         Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W $=$ $ -$ R/W       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins,         Upon reset, AMR is initialized to H'30.       Bit 6: Reserved bit       Bit 6: Reserved bit       Bit 6: Is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.         (Correct)       Bit       7       6       5       4       3       2       1       0         Bit 6: Reserved bit       Execution 1       1       0       <	Bits 7 and 6: Reser	rved bits							
Bits 4. 1. and 0 are reserved: only a write of 0 is possible.         Section 12 A/D Converter         12.2 Register Descriptions         12.2.2 A/D Mode Register (AMR)         (P280, P281)         (Incorrect)         Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0	Bits 7 and 6 are res	served; they a	<u>re alway</u>	vs read as 1	and canr	<u>iot be mod</u>	<u>ified.</u>		
Section 12 A/D Converter 12.2 Register Descriptions 12.2.2 A/D Mode Register (AMR) (P280, P281) (Incorrect) Bit $7 6 5 4 3 2 1 0$ CKS CH3 CH2 CH1 CH0 Initial value 0, 0, 1 1 0 0 0 0 0 0 Read/Write R/W = - R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger' option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit $7 6 5 4 3 2 1 0$ CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit $6 Reserved bit$ Bit $7 6 5 4 3 2 1 0$ CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit $6 Reserved bit$ This bit is reserved. do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions	<b>Bits:4, 1, and 0:</b> R	<u>eserved bits</u>							
12.2 Register Descriptions         12.2.2 A/D Mode Register (AMR)         (P280, P281)         (Incorrect)         Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W $=$ $ -$ R/W       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins,         Upon reset, AMR is initialized to H'30.       Bit 6: Reserved bit       Bit 6: Reserved bit       Bit 6: Is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.         (Correct)       Bit       7       6       5       4       3       2       1       0         Bit 6: Reserved bit       Exerce the conversion speed, external trigger       0       0       1       1       0       0       0       0         Read/Write       R/W       R/W $=$ $            -$ <td>Bits 4, 1, and 0 are</td> <td>reserved; onl</td> <td><u>y a write</u></td> <td>e of 0 is poss</td> <td><u>ible.</u></td> <td></td> <td></td> <td></td> <td></td>	Bits 4, 1, and 0 are	reserved; onl	<u>y a write</u>	e of 0 is poss	<u>ible.</u>				
12.2 Register Descriptions         12.2.2 A/D Mode Register (AMR)         (P280, P281)         (Incorrect)         Bit       7       6       5       4       3       2       1       0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W $=$ $-$ R/W       R/W       R/W       R/W         AdR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins,         Upon reset, AMR is initialized to H'30.       Bit 6: Reserved bit       Bit 6: Is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.         (Correct)       Bit       7       6       5       4       3       2       1       0.         Read/Write       R/W       R/W       R/W       R/W       R/W       R/W       R/W         MR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       0									
12.2.2 A/D Mode Register (AMR) $\cdots$ (P280, P281) (Incorrect) Bit 7 6 5 4 3 2 1 0 CKS CH3 CH2 CH1 CH0 Initial value 0, 0, 1 1 0 0 0 0 Read/Write R/W R/W R/W R/W R/W AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger ' option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit 7 6 5 4 3 2 1 0 CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6 Keserved bit Bit 6 Keserved bit R/W R/W R/W R/W AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit Diff 6: Reserved bit Life is a readable/Write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit This bit is reserved. do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions									
(Incorrect) Bit $76542.$ CH3 CH2 CH1 CH0 Initial value 0, 0, 1 1 0 0 0 0 0 Read/Write $R/W = R/W = R/W = R/W = R/W$ AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger ' option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit <u>6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous</u> operation. (Correct) Bit <u>7.654322.100</u> Bit <u>7.654322.100</u> CKS CH32 <u>CH2</u> <u>CH1</u> <u>CH0</u> Initial value 0 0 1 1 0 0 0 0 Read/Write $R/W = R/W = - R/W = R/W = R/W = R/W$ AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger operation. (Lorencet) Bit <u>7.654322.100</u> Read/Write $R/W = R/W = - R/W = R$	0	-		· · · · · (P	280. P28	31) -			
Bit $7$ 6543210 $CKS$ $   CH3$ $CH2$ $CH1$ $CH0$ Initial value00110000Read/Write $R/W$ $=$ $  R/W$ $R/W$ $R/W$ $R/W$ AMR is an 3 bit read/write register for specifying the A/D conversion speed, external trigger 'option, and the analog input pins,Upon reset, AMR is initialized to H'30. <b>Bit 6</b> :s a readable/writeable reserved bit, but should not be modified as this may cause erroneousoperation(Correct)Bit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ Initial value0011 $0$ $0$ $0$ $0$ Read/Write $R/W$ $R/W$ $R/W$ $R/W$ $R/W$ $R/W$ AMR is an 8 bit read/write register for specifying the A/D conversion speed, external triggeroption, and the analog input pins.Upon reset, AMR is initialized to H'30. <b>Bit 6</b> : Reserved bit <b>Bit 6</b> : Reserved bit <b>This bit is reserved.</b> do not set this bit to 1.Section 13 LCD Controller/Driver13.2 Register Descriptions				(1					
CKSCH3CH2CH1CH0Initial value001100000Read/WriteR/W $-$ -R/WR/WR/WR/WAMR is an 8-bit read/write register for specifying the A/D conversion speed, external triggeroption, and the analog input pins,Upon reset, AMR is initialized to H'30.Bit 6: Reserved bitBit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneousoperation.(Correct),Bit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ Initial value0011 $0$ $0$ $0$ Read/WriteR/W		7	6	. 5	4	- 3	2	1	0
Initial value $0$ , $0$ , $1$ , $1$ , $0$ , $0$ , $0$ , $0$ Read/Write $R/W =  R/W = R/W = R/W = R/W = R/W$ AMR is an 3-bit read/write register for specifying the A/D conversion speed, external trigger ' option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit $7$ , $6$ , $5$ , $4$ , $3$ , $2$ , $1$ , $0$ , CKS, $-$ , $-$ , $-$ , $CH3$ , $CH2$ , $CH1$ , $CH0Initial value 0, 0, 1, 1, 0, 0, 0Read/Write, R/W, R/W, -, -, R/W, R/W, R/W, R/WAMR is an 8-bit read/write register for specifying the A/D conversion speed, external triggeroption, and the analog input pins.Upon reset, AMR is 'initialized to H'30.Bit 6: Reserved bitThis bit is reserved. do not set this bit to 1.Section 13 LCD Controller/Driver13.2 Register Descriptions$		CKS ·		-					•
Read/Write       R/W $R/W$ $R/W$ $R/W$ $R/W$ $R/W$ $R/W$ AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins,         Upon reset, AMR is initialized to H'30. <b>Bit 6</b> : Reserved bit <b>Bit 6</b> : a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.         (Correct)       Bit       7       6       5       4       3       2       1       0.         Bit       7       6       5       4       3       2       11       CH0         Initial value       0       0       1       1       0       0       0         Read/Write       R/W       R/W $  -$ <	Initial value		0	1	1				
AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins, Upon reset, AMR is initialized to H'30. <u>Bit 6: Reserved bit</u> Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit $7 \cdot 6$ , $5 \cdot 4 \cdot 3$ , $2 \cdot 1$ , $0 \cdot CRS \cdot -$ , $-$ , $-$ , $CH3 \cdot CH2 \cdot CH1 \cdot CH0$ Initial value $0 \cdot 0 \cdot 1 \cdot 1 \cdot 0 \cdot 0 \cdot 0 \cdot 0$ Read/Write $R/W \cdot R/W \cdot -$ , $R/W \cdot R/W \cdot R/W \cdot R/W$ AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. <u>Bit 6: Reserved bit</u> This bit is reserved. do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions		· -	/	- , _		•			
option, and the analog input pins, Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit 7.6543.2.10. (Correct) Bit 7.6543.2.10. (Correct) Bit 7.6543.2.10. (Correct) Bit 7.6543.2.10. (Correct) Distribution of the second se		•	— . ter for si	pecifying the	$\Delta/D$ cor	• 1			
Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit 7.6.54.3.2.1.0. CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 0 0 0 0 Read/Write R/W	ontion and the ana	log input nin							
Bit 6: Reserved bit         Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.         (Correct)         Bit       7.6.5       4.3.2       1.0.         CKS       -       -       CH3       CH2       CH1       CH0         Initial value       0       0       1       1       0       0       0         Read/Write       R/W       R/W       -       -       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins       .       Upon reset, AMR is initialized to H'30.         Bit 6: Reserved bit       This bit is reserved.do not set this bit to 1.       .       Section 13 LCD Controller/Driver 13.2 Register Descriptions									
Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation. (Correct) Bit 7 6 5 4 3 2 1 0. CKS CH3 CH2 CH1 CH0 Initial value 0 0 1 1 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/writé register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit This bit is reserved. do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions	Opon reset, Amit is	s minanzeu u	5 11 SQ.						
operation.         (Correct)         Bit       7       6       5       4       3       2       1       0         CKS       -       -       -       CH3       CH2       CH1       CH0         Initial value       0       0       1       1       0       0       0       0         Initial value       0       0       1       1       0       0       0       0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W       R/W       M/W       R/W       R/W       R/W         AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins.         Upon reset, AMR is initialized to H'30.       Bit 6: Reserved bit       This bit is reserved.do not set this bit to 1.         Section 13 LCD Controller/Driver       13.2 Register Descriptions       Section 13 LCD Controller/Driver	Dit C' Decouved hi	4							
(Correct) Bit 7.6.543.2.10. CKS — — — — CH3. CH2. CH1 CH0 Initial value 0 0 1 1 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. Bit 6: Reserved bit This bit is reserved: do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions		-	awad hit	but should	not ho n	adified as	this man		
Bit       7       6       5       4       3       2       1       0         CKS       -       -       -       CH3       CH2       CH1       CH0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W       R/W       R/W       -       -       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins.       Upon reset, AMR is initialized to H'30.         Bit 6: Reserved bit       This bit is reserved; do not set this bit to 1.       Section 13 LCD Controller/Driver '13.2 Register Descriptions	Bit 6 is a readable/	-	erved bit	, but should	<u>not be n</u>	nodified as	this may o	ause erroj	<u>1eous</u>
Bit       7       6       5       4       3       2       1       0         CKS       -       -       -       CH3       CH2       CH1       CH0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W       R/W       R/W       -       -       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins.       Upon reset, AMR is initialized to H'30.         Bit 6: Reserved bit       This bit is reserved; do not set this bit to 1.       Section 13 LCD Controller/Driver '13.2 Register Descriptions		-	erved bit	, but should	not be n	nodified as	this may o	ause erroi	<u>1eous</u>
CKS       -       -       -       CH3       CH2       CH1       CH0         Initial value       0       0       1       1       0       0       0       0         Read/Write       R/W       R/W       R/W       -       -       R/W       R/W       R/W         AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins.       .         Upon reset, AMR is initialized to H'30.       .       .       .       .         Bit 6: Reserved bit       .       .       .       .       .         Section 13 LCD Controller/Driver       13.2 Register Descriptions       .       .       .	Bit 6 is a readable/ operation.	-	erved bit	, but should	<u>not be n</u>	nodified as	this may o	ause erroi	<u>1eous</u>
Initial value       0       0       1       1       0       0       0         Read/Write       R/W       R/W       R/W       R/W       R/W       R/W       R/W         AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins.       .         Upon reset, AMR is initialized to H'30.       .       .         Bit 6: Reserved bit       .         This bit is reserved. do not set this bit to 1.       .         Section 13 LCD Controller/Driver       13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct)	writeable rese			<u>not be n</u>				
Read/Write       R/W       R/W       R/W       R/W       R/W       R/W       R/W         AMR is an 8 bit read/write register for specifying the A/D conversion speed, external trigger       option, and the analog input pins.       Upon reset, AMR is initialized to H'30.         Bit 6: Reserved bit       This bit is reserved; do not set this bit to 1.         Section 13 LCD Controller/Driver       13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct)	writeable rese			<u>not be n</u>	3.	2	, 1 ,	0
AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins. Upon reset, AMR is initialized to H'30. <u>Bit 6: Reserved bit.</u> <u>This bit is reserved; do not set this bit to 1.</u> Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct) Bit	7 . CKS ·	6,	5	4	3 . CH3 .	2 CH2.	1 CH1	0 CH0
option, and the analog input pins. Upon reset, AMR is initialized to H'30. <u>Bit 6: Reserved bit.</u> <u>This bit is reserved: do not set this bit to 1.</u> Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct) Bit Initial value	writeable rese	6,  0	5	4	3 . CH3 . 0 .	2 CH2.	1 CH1	0 CH0
Upon reset, AMR is initialized to H'30. <u>Bit 6: Reserved bit</u> <u>This bit is reserved; do not set this bit to 1.</u> Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correci), Bit Initial value Read/Write	7 CKS · 0 R/W	6, — 0 <u>R/W</u> `	5	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
<u>Bit 6: Reserved bit</u> <u>This bit is reserved; do not set this bit to 1.</u> Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correci), Bit Initial value Read/Write	7 CKS · 0 R/W	6, — 0 <u>R/W</u> `	5	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
This bit is reserved; do not set this bit to 1. Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct), Bit Initial value Read/Write AMR is an 8-bit rea	7 <u>CKS</u> 0 R/W ad/write regis	6 . — 0 <u>R/W</u> ` ter for sj	5	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
Section 13 LCD Controller/Driver 13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana	7 CKS 0 R/W ad/writé regis	6 — 0 R/W ter for si	5	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is	7 CKS 0 R/W ad/write regis llog input pints s'initialized to	6 — 0 R/W ter for si	5	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
13.2 Register Descriptions	Bit 6 is a readable/ operation. (Correct), Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit	7 CKS 0 R/W ad/writé regis llog input pint s'initialized to	6 — 0 <u>R/W</u> ter for si s. o H'30.	5 — 1 — · Decifying the	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
	Bit 6 is a readable/ operation. (Correct), Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit	7 CKS 0 R/W ad/writé regis llog input pint s'initialized to	6 — 0 <u>R/W</u> ter for si s. o H'30.	5 — 1 — · Decifying the	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
13.2.1 LCD Port Control Register (LPCR) ······(P292)	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit This bit is reserved Section 13 J	7 CKS 0 R/W ad/write regis log input pint s'initialized to j. do not set th LCD Controll	6 – 0 <u>R/W</u> ` ter for si s o H'30. his bit to er/Driver	5 1  Decifying the 1.	4  1 	3 CH3 0 R/W	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit. This bit is reserved Section 13 I 13.2 Regist.	7 CKS 0 R/W ad/write regis llog input pin s'initialized to <u>5</u> <u>i.do not set th</u> LCD Controlle er Description	6, – 0 <u>R/W</u> ter for si s. o H'30. his bit to his bit to er/Driven	5 1  Decifying the 1.	4 — . 1 — . 2 A/D con	3 CH3 0 R/W aversion sp	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8-bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit. This bit is reserved Section 13 I 13.2 Regist	7 CKS 0 R/W ad/write regis llog input pin s'initialized to <u>5</u> <u>i.do not set th</u> LCD Controlle er Description	6, – 0 <u>R/W</u> ter for si s. o H'30. his bit to his bit to er/Driven	5 1  Decifying the 1.	4 — . 1 — . 2 A/D con	3 CH3 0 R/W aversion sp	2 CH2 0 R/W	1 CH1 0 R/W	0 CH0 0
	Bit 6 is a readable/ operation. (Correct) Bit Initial value Read/Write AMR is an 8 bit rea option, and the ana Upon reset, AMR is Bit 6: Reserved bit. This bit is reserved Section 13 I 13.2 Regist	7 CKS 0 R/W ad/write regis llog input pin s'initialized to <u>5</u> <u>i.do not set th</u> LCD Controlle er Description	6, – 0 <u>R/W</u> ter for si s. o H'30. his bit to his bit to er/Driven	5 1  Decifying the 1.	4 — . 1 — . 2 A/D con	3 CH3 0 R/W aversion sp	2 CH2 0 R/W	1 CH1 0 R/W	0 <u>CH0</u> 0

(Incorrect)								
	7	c	K	4	9 ,	9	1	٩
Bit	7. DTS1	6 · DTS0 ·	5 CMX	4	3 · SGS3 ·	2. SCS2		0
T-itialalua		0 DTS0	<u> </u>	i	<u> </u>	<u>SGS2 ·</u>	SGS1	SGSO
Initial value Read/Write	0 R/W	0. R/W.	0. R/W	0 . 	0 R/W	0 R/W	0 R/W	0 R/W
Bit 4: Reserved bit		Γ./ ΥΥ ,	IV 11	<u> </u>	D/ 11	IV/ W	EV VV	Γ// ΥΥ
<u>Bit 4: Reserved bit</u> · <u>Bit 4 is a readable/w</u>		wood hit ]	(+'io initia	lized to 0'	vi a reset			
<u>Dit + 10 a roumane</u>	IIIanie Ien-	IVCU DID	.6 10 11110-0-	<u>.1120 u vo e</u>	<u>)y a root.</u>			
(Correct)								
Bit	7	6	5 .	<u>4</u> ·	3.	2 .	1 .	0'
	DTS1	DTS0	CMX.		SGS3.	SGS2	SGS1	SGS0·
Initial value	0 ·	0 ·	0	• 0	0.	0 、	0.	0
Read/Write '	R/W	R/W	R/W	<u>R/W</u>	R/W	R/W	R/W	R/W
Bit 4: Reserved bit .	r	-	·	•	•	-		·
<u>This bit is reserved;</u>	<u>do not set t</u>	<u>his bit to l</u>	<u>1.</u>					
<b>2</b> 10 10 1								
Section 13 L 13.2 Registe			*					
13.2.3 LCD (	-		CR2) (	· · · · · (P	·296)			
(Incorrect)								
Bit ,	7	<u> </u>	5.	4 -	3.	2 -	1 .	0.
	LCDAB			_	—,		— .	<u> </u>
Initial value	0.	1 .	1 ·	0.	0	0 -	0.	0
Read/Write	R/W.		<del>.</del>	<u> </u>	Ξ.	Ξ,	Ξ,	=
Bits 4 to 0: Reserve	<u>d bits</u> .			-				
Bits.4 to 0 are reserv	<u>ved; they ca</u>	<u>n be read</u>	and writt	en, and are	<u>e initializ</u> e	<u>ed to 0 upo</u>	<u>ņ reset.</u>	
(Correct) .								
Bit	7.	6 \	5.	4 、	3、	2	1 `	0 -
	LCDAB	i i	1		— ,	<u> </u>	<del></del>	<u>`</u>
						I		
Initial value	0	1 -	 1 .	0.	0,	0	~ 0 ·	0 -
Read/Write	0 R/W	<u> </u>	<u> </u>	0 . <u>R/W</u> .		0 R/W	• 0 • <u>R/W</u> ·	0 · <u>R/W</u>
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			•
Read/Write	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			•
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			•
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			•
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			•
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			Ŧ
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			Ŧ
Read/Write Bits 4 to 0: Reserv	0 · · R/W · · <u>ved bits</u> ·	<b>—</b> 、	<del>-</del> .		0,			Ŧ

B.2 Function SPCR	18	• • • •	· (P348)					
ncorrect)								
SPCR-Serial Port C	ontrol Regis	ster			H'91			SCI
Bit	7	6	5	4	3	2	. 1	0
			SPC32		SCINV3	SCINV2		_
Initial value	1	1	0	<u>1</u>	0	0 -	<u>1</u>	1
Read/Write	_	-	R/W	Ξ	R/W	R/W	<u> </u>	=
Correct)			•		II'o 1			
SPCR Serial Port C					H'91			SCI
Bit	7	6	5	4	3	2	1	0
			SPC32	. —	SCINV3	SCINV2	_	
Initial value	1	1	0 DAV	=	0	0	=	=
Read/Write		_	R/W	<u>W</u>	R/W	R/W	W	<u>W</u>
ncorrect) TMA-Timer mode re	egister A				H'B0			Timer A
Bit	7	6	5	4	3	2	1	0
					TMA3	TMA2	TMA1	TMA0
Initial value	<u>1</u>	1	<u>1</u>	1	0	0	0	0
Read/Write	<u> </u>	_	. =	_	R/W	R/W	R/W	R/W
Correct)								
Correct) TMA-Timer mode re	egister A				H'B0	' <u>.</u>		Timer A
-	egister A	6	5	4	H'B0	2	11	Timer A
TMA-Timer mode re	-	6	5	4		2 TMA2	1 TMA1	
TMA-Timer mode re	-	<u> </u>	5 —   —	41	3			0
TMA-Timer mode re Bit	-	6 — — 	_		3 TMA3	TMA2	TMA1	0 TMA0
TMA-Timer mode re Bit Initial value	7				3 TMA3 0	TMA2 0	TMA1 0	0 TMA0 0
TMA-Timer mode re Bit Initial value Read/Write Appendix B I	7 — — <u>W</u> Internal I/(	  	— — — — — — — — — — — — — — — — — — —		3 TMA3 0	TMA2 0	TMA1 0	0 TMA0 0
TMA-Timer mode re Bit Initial value Read/Write	7 — — <u>W</u> Internal I/(	— — W O Registe	— — — — — — — — — — — — — — — — — — —		3 TMA3 0	TMA2 0	TMA1 0	0 TMA0 0
TMA-Timer mode re Bit Initial value Read/Write Appendix B I B.2 Function	7 — — <u>W</u> Internal I/(	— — W O Registe	□ − □ Ξ <u>₩</u> rs		3 TMA3 0	TMA2 0	TMA1 0	0 TMA0 0

LPCR-LCD port c	ontrol register	c			H'C0	. ]	LCD contro	ller/drive
Bit	7	6	5	4	3	2	1	0
	DTS1.	DTS0	CMX.	— .	SGS3	SGS2	SGS1	SGS0
Initial value	0 .	0	0	0,	0	0	0.	0.
Read/Write	R/W	R/W	R/W	=	R/W	R/W	R/W	R/W
orrect)				-				
LPCR-LCD port c	ontrol register	2			H'C0	Į	CD contro	ller/driver
Bit	7	6	5	4	3	2	1 ·	0,
	DTS1	DTS0	CMX <sup>.</sup>	<u> </u>	SGS3	SGS2	SGS1	SGS0 <sup>,</sup>
Initial value	0	0.	0,	0,	0,	0.	0.	. 0 .
Read/Write	R/W	R/W	R/W	<u>R/W</u> ,	R/W.	R/W	R/W.	R/W
B.2 Function	B Internal I/(	_						
LCR2 . Icorrect)			(P365)					
LCR2-LCD contro	l register 2				H'C2			LCD
Bit	. 7	6	5	4	3	2	1	0
	LCDAB	— •	<u> </u>	<u> </u>	— ·		<u> </u>	_
Initial value	0.	1 .	1.	0	0、	0	0.	0
Read/Write	R/W -	·	— .	Ξ.	<u> </u>	Ξ.	Ξ.	=
orrect)								
LCR2-LCD contro	l register 2				H'C2	I	CD control	ller/driver
Bit	7	6	5	4	3	2	1	0
	LCDAB.	-,	.—	— ,	<u> </u>	·,	— ı	<del>,</del>
Initial value	0	1 、	1	0	0	0	ο.	0
Read/Write	R/W	<b>—</b> .	`	<u>R/W</u> ,	<u>R/W</u>	<u>R/W</u> .	<u>R/W</u>	<u>R/W</u> •
Appendix E B.2 Functio	3 Internal I/(	O Register	8					
AMR	/115		(P366) ·	-				
correct)								
AMR·A/D mode re	gister				H'C6		A/D	converter
Bit	7	6	5	4	3	2	1	0
	CKS .	- ,	- *	_ '	CH3	CH2	СН1 ,	CH0
Initial value	0.	0.	· <b>1</b>	1 -	0	0.	0	0.
minina vanue								

Correct)	• •				*****			
AMR-A/D mode re	gister				H'C6	·.	A/D	) converte
Bit	7	6	5	4	3	2	1	0
	CKS		_		CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	<u>R/W</u>	_	_	R/W	R/W	R/W	R/W
Appendix B B.2 Functio PMR2		-	rs ∙(P368)					
Incorrect)			·(£306)	•				
	Damiatan O				TPCO			TO
PMR2-Port Mode I					H'C9			I/O por
Bit	7	6	5	4	3	2	1	0
		<u> </u>	POF1	-		_		IRQ0
Initial value	1	1	0	1	. 1	<u>1</u>	1	0
Read/Write	_	_	R/W		_	· _	=	R/W
Correct)								
PMR2-Port Mode I	Register 2				H'C9			I/O por
Bit	7	6	5	4	3	2	1	0
	_	-	POF1	_	_		_	IRQ0
Initial value	1	1	0	1.	1	_	· · · · ·	0
Read/Write	· <u> </u>	—	R/W	_	—	W	W	R/W
Appendix B B.2 Functio		O Register	rs					
PMR3			·(P369)					
ncorrect)						•		
PMR3 Port Mode I	Register 3				H'CA			I/O por
Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	–			TMOFH	TMOFL	
Initial value	0	0	_	_		0	0	_
Read/Write	R/W	R/W	—		, <u> </u>	R/W	R/W	_
Correct)								
PMR3-Port Mode H	Register 3				H'CA			I/O por
Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	—	<u> </u>		TMOFH	TMOFL	_
<b>T</b> '' <b>N</b> N	0	0	_	=		0	0	
Initial value								

	B Internal I/	O Registe	rs					
B.2 Functi PDR3	.ons		· (P372)					
(Incorrect)								
PDR3-Port data 1	egister 3				H'D6			I/O ports
Bit	7	6	• 5	4	3	2	1	0
	P37	<b>P3</b> 6	P35	P34	P33	P32	P31	
Initial value	0	0	0	0	0	0	0	1
Read/Write	· R/W	R/W	R/W	R/W	R/W	R/W	R/W	_
(Correct)								
PDR3-Port data 1	egister 3				H'D6			<u>I/O port</u>
Bit	7	6	5	4	3	2	1	0
	P37	<b>P3</b> 6	<b>P3</b> 5	P34	P33	P32	P31	
Initial value	0	0	0	0	0	0	0	· _
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
B.2 Functi PDR8	B Internal I/0 ons		rs • (P373)					
(Incorrect)								
PDR8-Port data r	egister 8				H'DB			<u>I/O ports</u>
Bit	7	6	5	4	3	2	1	0
		_		_		_	-	P80
Initial value	1	<u>1</u>	1	<u>1</u>	1	<u>1</u>	1	0
Read/Write	-	-	_	_	_			R/W
Correct)								
PDR8-Port data r	egister 8				H'DB	÷		<u>I/O port</u>
Bit	7	6	5	4	3	2	1	0
			—		—	—		P80
Initial value	=	<u> </u>	=	Ξ	=	<u> </u>	=	0
Read/Write		_	-	_		_	_	R/W
	B Internal I/( ons	— O Register	— 'S	_			_	R/W
Appendix I B.2 Functi PUCR3			— s (P374)		 	-	_	R/W
Appendix I B.2 Functi PUCR3 Incorrect)	ons	<i></i>			<u></u>	_	_	
Appendix 1 B.2 Functi PUCR3 Incorrect) PUCR3-Port pull <sup>.</sup>	ons up control reg		· (P374)		H'E1	_	_	<u>I/O_ports</u>
Appendix I B.2 Functi PUCR3 Incorrect)	ons up control reg	 ister 3 6	· (P374) 5	4	3	2	1	
Appendix J B.2 Functi PUCR3 Incorrect) PUCR3-Port pull- Bit	ons rup control reg 7 PUCR37	ister 3 6 PUCR36	• (P374) 5 PUCR35	PUCR34	3 PUCR33	PUCR32	PUCR31	<u>I/O_ports</u>
Appendix 1 B.2 Functi PUCR3 Incorrect) PUCR3-Port pull <sup>.</sup>	ons up control reg	 ister 3 6	· (P374) 5		3			<u>I/O_ports</u>

PUCR3-Port pull	up control reg	gister 3			H'E1.			<u>I/O</u> port
Bit	7 ·	6	5	4	3	2	1	0
	PUCR37	PUCR36	PUGR35	PUCR34	PUCR33	PUCR32	PUCR3i	
Initial value	0,	0	0`	<b>`</b> 0	0、	0,	ο.	<u> </u>
Read/Write	R/W	R/W	R/Ŵ	R/W	R/W	R/W	R/W	<u>W</u> ,
	3 Internal I/	O Register	rs .					
B.2 Functi PCR3	ons		·(P375)					
ncorrect)	•		·(F375),					
PCR3-Port contro	l nomistor 9				H'E6			TO
		_						<u>I/O ports</u>
Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	<b>—</b> ,
Initial value	0.	0.	<sup>0</sup> .	<sup>0</sup> .	Ο.	Ο.	0	1
Read/Write	<b>W</b> -	W _	W .	W .	W.	W	W .	. —
Correct) PCR3-Port contro	l nacistar 2				IVEC			1/0
		_			H'E6		·	<u>I/O</u> port
Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	,
Initial value	0.	0.	0.	0,	0,	,0	0,	
Read/Write	W	W	W	w	W .	W	W	• <u>W</u>
Appendix I	3 Internal I/	O Register	's					
B.2 Function								
PCR8			·(P377),					
ncorrect)								
PCR8-Port control	l register 8				H'EB .	*		<u>I/O ports</u>
Bit	7	6	5	4	3	2	1	0
	<u> </u>	<u> </u>	<u> </u>	-,	<u> </u>	<u> </u>	— <i>,</i>	PCR80
Initial value	<u>1</u> .	<u>1</u> .	1	<u>1</u> .	<u>1</u>	<u>1</u> .	<u>1</u>	0
Read/Write	Ξ.	Ξ.	<u> </u>	Ξ.	=.	Ξ.	Ξ,	W
Correct)								
PCR8 Port control	register 8				H'EB			<u>I/O port</u>
Bit	7	6	5	4	3	2	1	0
		'	_		_		_	PCR80
Initial value		·	` _`	Ξ`	·			0
Read/Write	<u> </u>	<u></u>	<u></u>	— <u>₩</u>	<u></u>	 <u>W</u>	<u> </u>	w
· · · · · · · · · · · ·	- <u></u> ,	<u></u>	<u></u>	<u>.</u>	<u></u>	<u></u>		**

Bit       7       6       5       4       3       2       1       0         Initial value       1       1       1       1       0       1       0       0       0         Read/Write       -       -       -       R/W       =       R/W       E/W       E/W       E/W         Correct)       PMR9-Port mode register 9       FTEC       IO       IO       E/W       E/W <th< th=""><th>Appendix B I</th><th></th><th>O Registe</th><th>ers</th><th>•</th><th></th><th></th><th></th><th></th></th<>	Appendix B I		O Registe	ers	•				
PMR9-Port mode register 9       HEC $UOL$ Bit       7       6       5       4       3       2       1 $OOL$ Bit       7       6       5       4       3       2       1 $OOL$ Initial value       1       1       1       1       0       1       0       0       0         Read/Write       -       -       -       -       R/W       =       R/W       R/W         PMR9-Port mode register 9       HEC       IOO       1       0       =       0       0         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       1       0       =       0       0       0         Read/Write       -       -       -       -       R/W       W       R/W       R/W         Bit       7       6       5       4       3       2       1       0         IBGR-IRQ edge select register       HTP2       System cor       Bit       7       6       5       4       3       2       1       0         IDG		S		· (P377)					
Bit       7       6       5       4       3       2       1       0 $[  -$	(Incorrect)								
- $  -$	PMR9-Port mode reg	gister 9				H,EC			I/O ports
Initial value       1       1       1       1       0       1       0       0       0         Read/Write       -       -       -       R/W $=$ R/W       R/W       R/W       R/W         PMR9-Port mode register 9       H'EC       IOO         Bit       7       6       5       4       3       2       1       0         Ditital value       1       1       1       1       0 $\equiv$ 0       0       0         Bit       7       6       5       4       3       2       1       0 </td <td>Bit</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td>	Bit	7	6	5	4	3	2	1	0
Read/Write       -       -       R/W       -       R/W       R/W <th< td=""><td></td><td>_</td><td>—</td><td>_</td><td></td><td>PIOFF</td><td>  _</td><td>PWM2</td><td>PWM1</td></th<>		_	—	_		PIOFF	_	PWM2	PWM1
(Correct)       PMR9-Port mode register 9       HTEC       IO         Bit       7       6       5       4       3       2       1       O         Bit       7       6       5       4       3       2       1       O         Bit       7       6       5       4       3       2       1       O         Initial value       1       1       1       1       0 $\equiv$ 0       O         Read/Write       -       -       -       -       R/W       W       R/W       R/W         Appendix B Internal I/O Registers       B.2 Functions       IEGR	Initial value	1	1	1	1	0	1	0	0
PMR9-Port mode register 9       HEC       IO         Bit       7       6       5       4       3       2       1       0         Bit       7       6       5       4       3       2       1       0         Initial value       1       1       1       1       0       =       0       0         Read/Write       -       -       -       R/W       W       R/W       R/W         Appendix B Internal I/O Registers       B.2 Functions       IEGR       W       W       R/W       R/W         (Incorrect)       IEGR-IRQ edge select register       H'F2       System cor       System cor         Bit       7       6       5       4       3       2       1       0         Initial value       0       1       1       1       1       0       0       0         Read/Write       -       -       -       -       -       R/W       R/W         IEGR-IRQ edge select register       H'F2       System cor       1       1       1       1       0       0         Read/Write       1       1       1       =       =       0 <t< td=""><td>Read/Write</td><td></td><td><del>-</del> .</td><td>-</td><td></td><td>R/W</td><td>=</td><td>R/W</td><td>R/W</td></t<>	Read/Write		<del>-</del> .	-		R/W	=	R/W	R/W
Bit       7       6       5       4       3       2       1       0         Initial value       1       1       1       1       0 $\equiv$ 0       0         ReadWrite       -       -       -       -       RW       W       R/W       R/W         Appendix B Internal I/O Registers       B.2 Functions       IEGR      (P381)	(Correct)								
- $   -$	PMR9-Port mode reg	rister 9				H'EC			<u>I/O port</u>
Initial value1110 $\equiv$ 0(0Read/WriteR/WWR/WR/WR/WR/WR/WR/WAppendix B Internal I/O RegistersB.2 FunctionsIEGR(P381)(P381)(P381)(Incorrect)Bit $7$ 65432100 $\square$ Initial value $0$ 1111000Read/Write $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ IEGR-IRQ edge select registerHTF2System corrSystem corrBit $7$ 6543210 $\square$	Bit	7	6	5	4	3	2	1	0
Read/Write       -       -       -       R/W       W       R/W       R		_	—			PIOFF	_	PWM2	PWM1
Appendix B Internal I/O Registers B.2 Functions IEGR IEGR IEGR IEGR-IRQ edge select register Bit 7 6 - - - - - - - -	Initial value	1	1	1	1	0	Ξ	0	0
B.2 Functions IEGR      (P381)         (Incorrect)         IEGR IRQ edge select register       HF2       System correct)         Bit       7       6       5       4       3       2       1       0       0         Bit       7       6       5       4       3       2       1       0       0         Initial value       0       1       1       1       1       0       0       0         Read/Write       -       -       -       -       -       R/W       R/W         Bit       7       6       5       4       3       2       1       0       0         Bit       7       6       5       4       3       2       1       0       0       0         Initial value       1       1       =       =       0	Read/Write		—	_	—	R/W	W	R/W	R/W
IEGR·IRQ edge select register       HF2       System control         Bit       7       6       5       4       3       2       1       0         Initial value       0       1       1       1       1       0       0         Read/Write       -       -       -       -       -       -       IEG1       IEG1         IEGR-IRQ edge select register       H'F2       System control       R/W       R/W       R/W         (Correct)       IEGR-IRQ edge select register       H'F2       System control       System control         Bit       7       6       5       4       3       2       1       0         Bit       7       6       5       4       3       2       1       0       0         Read/Write       1       1       1       =       =       0       0       0         Read/Write       1       1       1       =       =       0       0       0         Read/Write       -       -       -       -       -       R/W       R/W         Appendix B Internal I/O Registers       B.2 Functions       IENR1       HT3       System control	<b>B.2</b> Functions		-						
Bit       7       6       5       4       3       2       1       0         Initial value       0       1       1       1       1       1       0       0         Read/Write       -       -       -       -       -       -       IEG1       IEA         Initial value       0       1       1       1       1       0       0         Read/Write       -       -       -       -       -       R/W       R/W         (Correct)       IEGR-IRQ edge select register       HTF2       System corr         Bit       7       6       5       4       3       2       1       0         IEGR-IRQ edge select register       HTF2       System corr       IEG1       IEM         Bit       7       6       5       4       3       2       1       0         Gead/Write       1       1       1       =       =       0       0       0         Read/Write       -       -       -       -       -       R/W       R/W         Appendix B Internal I/O Registers       B.2 Functions       IENR1       HTF3       System corr       0	(Incorrect)								
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IEGR-IRQ edge selec	ct register				H'F2		Syste	em control
Initial value $\underline{0}$ 11 $\underline{1}$ $\underline{1}$ $\underline{1}$ $\underline{1}$ $\underline{0}$ $\underline{1EG1}$ $\underline{1EG1}$ $\underline{1EG1}$ Read/Write $       R/W$ $R/W$ (Correct)Bit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ $       1$ $1$ Initial value $1$ $1$ $1$ $=$ $=$ $0$ $0$ Read/Write $      R/W$ $R/W$ Appendix B Internal I/O Registers B.2 Functions IENR1(P382) $HF3$ System cord(Incorrect)IENR1 $ HF3$ System cordBit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ $\overline{1ENTA}$ $ IENWP$ $  IENEC2$ $IEN1$	Bit	7	6	5	4	3	2	1	0
Read/WriteR/WR/W(Correct)IEGR-IRQ edge select registerH'F2System corrBit7654321 $-$ IEG1IEG1Initial value111==00Read/WriteRead/Write0Read/WriteR/WR/WAppendix B Internal I/O Registers B.2 Functions IENR1(P382)Krain System corr(Incorrect) Bit76543210IENR1-Interrupt enable register 1H'F3System corrBit76543210IENTA-IENWPIENEC2IEN1IEN		_	· <u> </u>		_		_	IEG1	IEG0
(Correct)         IEGR-IRQ edge select register       H'F2       System correction         Bit       7       6       5       4       3       2       1       0         Bit       7       6       5       4       3       2       1       0         It       1	Initial value	<u>0</u>	1	1	<u>1</u>	1	1	0	0
IEGR-IRQ edge select registerH'F2System controlBit76543210 $     -$ IEG1IEMInitial value111 $=$ $=$ 00Read/Write $    -$ R/WR/WAppendix B Internal I/O Registers B.2 Functions IENR1(P382)H'F3System control(Incorrect)IENR1·Interrupt enable register 1H'F3System controlBit7654321 $0$ IENTA $-$ IENWP $ -$ IENEC2IEN1	Read/Write		_	_	<b>—</b> ,	-,	•	R/W	R/W
Bit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ $          -$ Initial value $1$ $1$ $1$ $       -$ Initial value $1$ $1$ $1$ $   -$	(Correct)								
- $   -$	IEGR·IRQ edge selec	ct register				H'F2	*	Syste	em control
Initial value $1$ $1$ $1$ $=$ $=$ $=$ $0$ $0$ Read/Write $     R/W$ $R/W$ Appendix B Internal I/O Registers B.2 Functions IENR1(P382)(Incorrect)IENR1·Interrupt enable register 1H'F3System corrBit $7$ $6$ $5$ $4$ $3$ $2$ $1$ $0$ IENTA $-$ IENWP $ -$ IENEC2IEN1IEN	Bit	7	6	5	4	3	2	1	0
Read/Write     -     -     -     -     R/W     R/W       Appendix B Internal I/O Registers       B.2 Functions       IENR1       IENR1       IENR1       IENR1·Interrupt enable register 1       Bit     7     6     5     4     3     2     1     0       IENTA     -     IENWP     -     -     IENEC2     IEN1     IEN			_					IEG1	IEG0
Appendix B Internal I/O Registers         B.2 Functions         IENR1      (P382)         (Incorrect)         IENR1·Interrupt enable register 1       H'F3       System corr         Bit       7       6       5       4       3       2       1       0         IENTA       —       IENWP       —       —       IENEC2       IEN1       IEN	Initial value	1	1	1		_	Ξ.	0	0 '
B.2 Functions IENR1 ······(P382) (Incorrect) IENR1·Interrupt enable register 1 H'F3 System cor Bit 7 6 5 4 3 2 1 0 IENTA - IENWP IENEC2 IEN1 IEN	Read/Write			-	<b>—</b> ,	— .	—	R/W	R/W
(Incorrect)         IENR1-Interrupt enable register 1       H'F3       System cor         Bit       7       6       5       4       3       2       1       0         IENTA       —       IENWP       —       —       IENEC2       IEN1       IEN	B.2 Functions		-						
IENR1-Interrupt enable register 1H'F3System corBit76543210IENTA-IENWPIENEC2IEN1IEN				- (F382)					
Bit 7 6 5 4 3 2 1 0 IENTA - IENWP IENEC2 IEN1 IEN	-	able registe	r 1			H'F3		Svste	em control
IENTA – IENWP – – IENEC2 IEN1 IEN				5	4		2		0
						_			IENO
	∟ Initial value		1		1	1			
Read/Write R/W — R/W — R/W R/W R/					<u> </u>	. <u> </u>			R/W

· · · · · · · ·						*****		
(Correct)								
IENR1-Interrupt	enable regist	er 1			H'F3		Syst	em contro
Bit	7	6	5	4	3	2	1	0
	IENTA		IENWP	_	_	IENEC2	IEN1	IEN0
Initial value	0	=	0.	=		0 .	0	0
Read/Write	R/W	<u> </u>	R/W	<u> </u>	<del>,</del>	R/W -	R/W	R/W
Appendix B.2 Functi IENR2	B Internal I/ Ions	-	rs · (P383)		·			
(Incorrect)								
IENR2-Interrupt	enable registe	er 2			H'F4		Syst	em contro
Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD			IENTFH	IENTFL		IENEC
Initial value	0	0	1	1	0	0	<u>1</u>	0
Read/Write	<u>R/(W)</u>	<u>R/(W)</u>	=	_	<u>R/(W)</u>	<u>R/(W)</u>	Ξ	<u>R/(W)</u>
Correct)								
IENR2-Interrupt	enable registe	er 2			H'F4		Syst	em contro
Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	_	_	IENTFH	IENTFL		IENEC
Initial value	0	0	<b>—</b>	<u> </u>	0	0΄	<u> </u>	0
Read/Write	<u>R/W</u>	<u>R/W</u>	W	W	<u>R/W</u>	<u>R/W</u>	W	<u>R/W</u>
Appendix 1 B.2 Functi IRR1	B Internal I/ ons	-	rs · (P384)					
Incorrect)						*		
IRR1-Interrupt re	equest register	r 1			H'F6		Syste	em contro
Bit	7	6	5	4	3	2	1	0
	IRRTA	—		_		IRREC2	IRRI1	IRRIO
Initial value	0	<u>1</u>	1	<u>1</u>	1	0	0	0
Read/Write	R/W*	•	<b></b>	<b>—</b>	<del>.</del> .	R/W*	R/W*	R/W*
Correct)								
		r 1			H'F6		Syste	em contro
IRR1-Interrupt re	equest register							
IRR1-Interrupt re Bit	equest register	6	5	4	3	2	1	0
			5	4	3	2 IRREC2	1 IRRI1	0 IRRI0
	7		5	4 	3 — —			

 $\mathbf{22}$ 

				and the second					
Appendix B	Internal 1/	O Register	cs						
B.2 Functior	ıs								
IRR2	·····(P385)								
(Incorrect)									
IRR2-Interrupt request register 2				H'F6			System control		
Bit	7	6	5	4	3	2	1	0	
	IRRDT	IRRAD		_	IRRTFH	IRRTFL		IRREC	
Initial value	0	0	<u>1</u>	1	0	0	<u>1</u>	<u>0</u>	
Read/Write	<u>R/(W)*</u>	<u>R/(W)*</u>	=	=	<u>R/(W)*</u>	<u>R/(W)*</u>	<b></b>	<u>R/(W)*</u>	
(Correct)									
IRR2-Interrupt request register 2				H'F6			Syst	System control	
Bit	7	6	5	4	3	2	1	0	
	IRRDT	IRRAD			IRRTFH	IRRTFL	_	IRREC	
Initial value	0	0	=	=	0	0	=	=	
Read/Write	<u>R/W*</u>	<u>R/W*</u>	W	W	<u>R/W*</u>	<b>R/W*</b>	<u>w</u>	<u>R/W*</u>	