

RENESAS TECHNICAL UPDATE

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|--------------------|--|----------|----------------------|------------------------|------|------|
| Product Category | MPU/MCU | | Document No. | TN-V85-A033B/E | Rev. | 2.00 |
| Title | Additional precaution on store buffer of RAM. | | Information Category | Technical Notification | | |
| Applicable Product | V850E2/Dx4 series V850E2/Dx4-H series V850E2/Fx4 series V850E2/Fx4-G series V850E2/Fx4-H series V850E2/Fx4-L series V850E2/Mx4 series V850E2/Px4 series V850E2/Px4-L series V850E2/Sx4-H series | Lot No. | Reference Document | User manual | | |
| | | All lots | | | | |

We would like to inform you of the precautions of write and read regarding RAM of the products above.

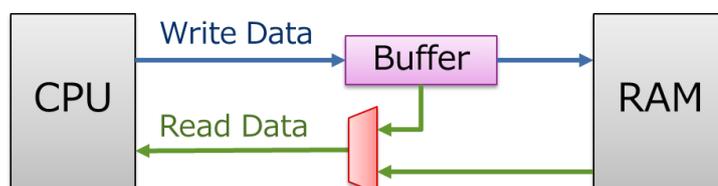
In the case of using "User's Manual: Hardware" regarding the products above, please use it together with this material.

[Additional Description]

In the products shown in "Applicable Product", there is store buffer between CPU and its Local RAM (LRAM) for the fast access to RAM. The CPU may read data from the buffer instead of RAM if the CPU reads from the same address where the CPU writes before the read.

There is no problem for reading from the buffer functionally, and it does not affect the operation of software.

However, if you are doing writing to and reading from LRAM for the test purpose, there is a possibility to perform unexpected operation (reading from the buffer, not from RAM). Since the buffer is not described in the UMs, you may encounter this problem unintentionally.



Take one of the following procedures to ensure to read out data from RAM:

- Read out the first written data, only after more than 4 bytes of data are written into RAM.
(for all products)
- Execute one or more instructions which do not access to the memory (e.g. NOP instruction) before a load instruction is executed on the same address after a store instruction to the RAM.
(for V850E2/Fx4-L, Fx4-G only)

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