

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A028A/E	Rev.	1.00
Title	Additional explanation for Pin Multiplexing and PFC of RZ/G Series		Information Category	Technical Notification		
Applicable Product	RZ/G Series RZ/G1E	Lot No.	Reference Document	RZ/G1E User's Manual: Hardware Rev.1.00 (R01UH0544EJ0100)		
		All lots				

There is a following additional explanation about the RZ/G1E.

[Summary]

Additional explanation when these pins were used as I2C interface.

[Products]

RZ/G1E

[Note]

There is no specification change (additional explanation only).

[Additional Explanation]

(Following gray highlighted parts (abcd) are newly added.)

1. Section 4, Pin Multiplexing

1) Table 4.2, No.278 to 281 (page 4-24), No.302, 303 (page 4-25), and Notes

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
. . .							
278	Y5	I2C0_SCL ^(*6)	IO	I	GP3_30	I	On
279	Y4	I2C0_SDA ^(*6)	IO	I	GP3_31	I	On
280	Y24	I2C1_SCL ^(*6)	IO	I	GP4_0	I	On
281	Y25	I2C1_SDA ^(*6)	IO	I	GP4_1	I	On
. . .							
302	AD21	I2C2_SCL ^(*6)	IO	I	GP4_22	I	On
303	AC20	I2C2_SDA ^(*6)	IO	I	GP4_23	I	On
. . .							
340	V22	IIC1_SDA	IO	Z	IIC1_SDA	Z	-

Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.

. . .

- 5. No.201 CS1#/A26 Default state:
MD4 = 0: (area 0 64-Mbyte mode): high output
MD4 = 1: (area 0 128-Mbyte mode): low output

6. No.278 to 281, 302 and 303 Pin Name (Function 1):
When these pins are used as I2C interface, external pull-up resistors are mandatory.

2) Table 4.3, No.278 to 281 (page 4-33), No.302, 303 (page 4-34), and Notes

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Default Boot	Default Pull-up	Pin Handling when not in Use
. . .							
278	Y5	I2C0_SCL ^(*5)	I	-	-	On	Open
279	Y4	I2C0_SDA ^(*5)	I	-	-	On	Open
280	Y24	I2C1_SCL ^(*5)	I	-	-	On	Open
281	Y25	I2C1_SDA ^(*5)	I	-	-	On	Open
. . .							
302	AD21	I2C2_SCL ^(*5)	I	-	-	On	Open
303	AC20	I2C2_SDA ^(*5)	I	-	-	On	Open
. . .							
340	V22	IIC1_SDA	Z	-	-	-	Pulled-up to VCCQ18

Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.

. . .

- 4. No.201 CS1#/A26 Default state:
MD4 = 0: (area 0 64-Mbyte mode): high output
MD4 = 1: (area 0 128-Mbyte mode): low output

5. No.278 to 281, 302 and 303 Pin Name (Function 1):
When these pins are used as I2C interface, external pull-up resistors are mandatory.

2. Section 5. Pin Function Controller (PFC)

1) 5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Bit Name	Set Value = 1
PUPR3[31]	I2C1_SDA is pull up ^(*)
PUPR3[30]	I2C1_SCL is pull up ^(*)
PUPR3[29]	I2C0_SDA is pull up ^(*)
PUPR3[28]	I2C0_SCL is pull up ^(*)
. . .	
PUPR3[0]	VI0_DATA1_VI0_B1 is pull up

Note: 1. When these pins are used as I2C interface, external pull-up resistors are mandatory.

2) 5.3.30 LSI Pin Pull-Up Control Register 4 (PUPR4)

Bit Name	Set Value = 1
PUPR4[31]	SSI_SCK0129 is pull up
. . .	
PUPR4[21]	I2C2_SDA is pull up ^(*)
PUPR4[20]	I2C2_SCL is pull up ^(*)
. . .	
PUPR4[0]	MSIOF0_RXD is pull up

Note: 1. When these pins are used as I2C interface, external pull-up resistors are mandatory.

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