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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A022A/E	Rev.	1.00
Title	Addition of Specifications regarding Sub-clock Oscillator Drive Ability Control Bit		Information Category	Technical Notification		
Applicable Product	RX63N Group, RX631 Group	Lot No. All	Reference Document	RX63N Group, RX631 Group User's Manual: Hardware Rev.1.00 (R01UH0041EJ0100)		

This document describes addition of specifications regarding the sub-clock oscillator drive ability control bit in RX63N Group and RX631 Group and notes on using a low CL crystal unit.

(1) Sub-clock oscillator drive ability control bit specifications

Added specifications of the RTCDV[2:0] bits (sub-clock oscillator drive ability control) to bits b3 to b1 in the RTC control register 3 (RCR3) as follows:

RTC Control Register 3 (RCR3)

Bit	Symbol	Bit Name	Description	R/W
b0	RTCEN	Sub-clock Control	0: Sub-clock oscillator is stopped. 1: Sub-clock oscillator is running.	R/W
b3 to b1	RTCDV[2:0]	Sub-clock Oscillator Drive Ability Control	b3 b1 0 0 1: Drive ability for low CL 1 1 0: Drive ability for standard CL Settings other than those listed above are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RTCDV[2:0] bits (Sub-Clock Oscillator Drive Ability Control)

These bits control the drive ability of the sub-clock oscillator. When connecting a standard CL crystal unit, set these bits to 110b (drive ability for standard CL). When connecting a low CL crystal unit, set these bits to 001b (drive ability for low CL).

Set the RTCDV[2:0] bits while the sub-clock oscillator stop bit (SOSCCR.SOSTP) in the sub-clock oscillator control register is 1 and the sub-clock oscillator control bit (RCR3.RTCEN) in RTC control register 3 is 0.

(2) Notes on using a low CL crystal unit

When the RCR3.RTCDV[2:0] bits are 001b (drive ability for low CL), the oscillator is susceptible to noise. Especially when the signal level of any pin near the XCIN or XCOUT pin is changed, the oscillation accuracy of the sub-clock oscillator may be affected. The accuracy is affected differently depending on the board traces and how the signal level of any pin near the XCIN or XCOUT pin is changed. When designing a board using a low CL crystal unit, refer to the application note "Design Guide for Low CL Sub-clock Circuits" (R01AN1187EJ) to reduce the influence from the noise.

The following are examples that may significantly affect the oscillation accuracy:

(a) When connecting an on-chip debugging emulator to the FINED pin

Since the FINED pin (FINE interface pin) is near the XCIN and XCOUT pins, the oscillation accuracy of the sub-clock oscillator is affected by debugging with the FINED pin. When debugging with the FINED pin, keep using the low CL crystal unit and set the RCR3.RTCDV[2:0] bits to 110b (drive ability for standard CL). However, this measure may affect the reliability of the crystal unit. Therefore, use this measure only when using an on-chip debugging emulator. Set the RCR3.RTCDV[2:0] bits to 001b (drive ability for low CL) in mass production programs. When connecting an emulator to the JTAG pin (TCK pin, TRST pin, TMS pin, TDI pin, TDO pin), the oscillation accuracy is not affected.

(b) When supplying an external clock to the main clock oscillator

When inputting an external clock to the EXTAL pin, the oscillation accuracy of the sub-clock oscillator may be affected. In addition, when the inverted external clock is input to the XTAL pin, the oscillation accuracy may be more severely affected.