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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A166A/E	Rev.	1.00
Title	Addition of Specification for the ID code protection of the RX65N and RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All Mass-produced Products	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)		

This document describes the addition of a specification for the ID code protection to the RX65N and RX651 Group and includes changes in the user's manual: hardware, which are resulted from this addition.

1. Additional Function

A function, that all blocks in the user area and the option-setting memory area are erased when the ID codes do not match three times consecutively, is added to the specifications of the ID code protection.

2. Changes in the Contents of the User's Manual: Hardware

The descriptions in the user's manual are changed as follows according to the addition of the specification mentioned above.

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The descriptions in the table and below the table in section 7.2.2, OCD/Serial Programmer ID Setting Register (OSIS) are changed as follows:

Before correction

Address	Bit 31			Bit 0
FE7F 5D50h to FE7F 5D53h	OCD/serial ID4	OCD/serial ID3	OCD/serial ID2	OCD/serial ID1
FE7F 5D54h to FE7F 5D57h	OCD/serial ID8	OCD/serial ID7	OCD/serial ID6	OCD/serial ID5
FE7F 5D58h to FE7F 5D5Bh	OCD/serial ID12	OCD/serial ID11	OCD/serial ID10	OCD/serial ID9
FE7F 5D5Ch to FE7F 5D5Fh	OCD/serial ID16	OCD/serial ID15	OCD/serial ID14	OCD/serial ID13

OCD/Serial ID 1 to 16

These fields hold the ID for use in ID authentication for the OCD/serial programmer.
The OCD/serial ID1 field is reserved; set this field to FFh.

After correction

Address	Bit 31			Bit 0
FE7F 5D50h to FE7F 5D53h	OCD/serial ID4	OCD/serial ID3	OCD/serial ID2	OCD/serial ID1 (control code)
FE7F 5D54h to FE7F 5D57h	OCD/serial ID8	OCD/serial ID7	OCD/serial ID6	OCD/serial ID5
FE7F 5D58h to FE7F 5D5Bh	OCD/serial ID12	OCD/serial ID11	OCD/serial ID10	OCD/serial ID9
FE7F 5D5Ch to FE7F 5D5Fh	OCD/serial ID16	OCD/serial ID15	OCD/serial ID14	OCD/serial ID13

OCD/Serial ID 1 to 16

These fields hold the ID for use in ID authentication for the OCD/serial programmer.
OCD/serial ID1 functions as a control code when the MCU is connected to a serial programmer and as an ID code when the MCU is connected to an OCD.
For details of the control code, refer to section 7.4, Settings of the Option-Setting Memory and ID Code Authentication.

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A description is added to the descriptions of the FSPR bit (Access Window Protection) in section 7.2.8, Flash Access Window Setting Register (FAW) as follows:

After Correction

FSPR Bit (Access Window Protection)

Setting the FSPR bit protects the following operations.

- Setting the areas including the FAW register by using the configuration setting command of the FACI commands.
- Setting the areas including the FAW register by using the configuration program command in boot mode.
- Erasing the option-setting memory area by using the configuration clearing command in boot mode.
- Changing the setting of the start-up area protection by using the FSUACR register.
- Erasing all blocks in the user area and the option-setting memory area, when the ID codes do not match three times consecutively in boot mode while the control code is 45h.

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The descriptions in section 7.4, Settings of the Option-Setting Memory and ID Code Authentication, Reading, Programming, and Erasure are changed as follows:

Before correction

7.4 Settings of the Option-Setting Memory and ID Code Authentication, Reading, Programming, and Erasure

Table 7.3 shows the settings of the option-setting memory and ID code authentication, reading, programming, and erasure.

Table 7.3 Settings of the Option-Setting Memory and ID Code Authentication, Reading, Programming, and Erasure

No.	SPCC.SPE	OSIS	Connection of a Serial Programmer	Reading, Programming and Erasure after the Connection of a Serial Programmer
1	0	Any value	Connection prohibited	—
2	1		ID code authentication*1	Reading permitted, programming permitted, erasure permitted

Note 1. This determines whether the ID code sent by the serial programmer matches the ID code set in the OSIS register. When the ID codes match, connection is permitted; if not, connection is not possible.

After correction

7.4 Settings of the Option-Setting Memory and ID Code Authentication

Table 7.3 shows the settings of the option-setting memory and ID code authentication when the MCU is connected to a serial programmer.
Table 7.4 shows the settings of the option-setting memory and ID code authentication when the MCU is connected to an OCD.

Table 7.3 Settings of the Option-Setting Memory and ID Code Authentication When the MCU is Connected to a Serial Programmer

No.	SPCC.SPE	OSIS (OCD/Serial ID1 (Control Code))	OSIS (OCD/Serial ID2 to ID16)	Connection to a Serial Programmer	Reading, Programming and Erasure after the Connection to a Serial Programmer
1	0	Any value	Any value	Connection prohibited	—
2	1	45h	Any value	ID codes matched: Transition to the command waiting phase ID codes unmatched: Transition to the state of waiting for a serial programming ID code check command again. When the ID codes do not match three times consecutively, all blocks in the user area and the option-setting memory area are erased.*1	Reading permitted, programming permitted, erasure permitted
3	1	Other than 45h	Any value	ID codes matched: Transition to the command waiting phase ID codes unmatched: Transition to the state of waiting for a serial programming ID code check command again.	Reading permitted, programming permitted, erasure permitted

Note 1. When the FAW.FSPR bit is 0, the blocks in those areas are not erased.

Table 7.4 Settings of the Option-Setting Memory and ID Code Authentication When the MCU is Connected to an OCD

No.	SPCC. SPE	OSIS (OCD/Serial ID1 (Control Code))	OSIS (OCD/Serial ID2 to ID16)	Connection to an OCD
1	—	Any value	Any value	ID codes matched: Connection to an OCD is permitted ID codes unmatched: Waiting for the input of ID code

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The description of the example of setting the OCD/serial programmer ID setting register in section 7.5.1, Allocation of Data in the Option-Setting Memory is changed as follows:

Before correction

Setting the following ID codes in the OCD/serial programmer ID setting register (OSIS)
ID1 = FFh, ID2 = 02h, ID3 = 03h, ID4 = 04h, ID5 = 05h, ID6 = 06h, ID7 = 07h, ID8 = 08h
ID9 = 09h, ID10 = 0Ah, ID11 = 0Bh, ID12 = 0Ch, ID13 = 0Dh, ID14 = 0Eh, ID15 = 0Fh, ID16 = 10h
.ORG 0FE7F5D50h
.LWORD 0040302FFh, 008070605h, 00C0B0A09h, 0100F0E0Dh

After correction

Setting the following ID codes in the OCD/serial programmer ID setting register (OSIS)
ID1 (control code) = FFh, ID2 = 02h, ID3 = 03h, ID4 = 04h, ID5 = 05h, ID6 = 06h, ID7 = 07h, ID8 = 08h
ID9 = 09h, ID10 = 0Ah, ID11 = 0Bh, ID12 = 0Ch, ID13 = 0Dh, ID14 = 0Eh, ID15 = 0Fh, ID16 = 10h
.ORG 0FE7F5D50h
.LWORD 0040302FFh, 008070605h, 00C0B0A09h, 0100F0E0Dh

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The descriptions of section 56.10.2, ID Code Protection are changed as follows:

Before correction

This function is used to prohibit connection with the serial programmer. When connecting a serial programmer, the ID code set in the OCD/serial programmer ID setting register (OSIS) and written in the option-setting memory is used to judge ID code protection on connection of the serial programmer.
When the ID code protection is enabled, the code sent from the serial programmer is compared with the ID code set in the OCD/serial programmer ID setting register (OSIS) to determine whether they match. If they match, connection with the serial programmer is allowed. If they do not match, the serial programmer cannot be connected.

After correction

This function is used to prohibit connection with the serial programmer. When the MCU is connected to a serial programmer, OCD/serial ID1 in the OCD/serial programmer ID setting register (OSIS) functions as a control code.
When the MCU is connected to a serial programmer, the control code and ID code stored in the OCD/serial programmer ID setting register (OSIS) on the option-setting memory are used to judge ID code protection on connection of the serial programmer.
The code sent from the serial programmer is compared with the control code and ID code set in the OCD/serial programmer ID setting register (OSIS) to determine whether they match. If they match, connection with the serial programmer is allowed. If they do not match, the serial programmer cannot be connected. However, when the control code is 45h and if the codes do not match three times consecutively, all blocks in the user area and option-setting memory area are erased.*1

Note 1. When the FAW.FSPR bit is 0, the blocks in those areas are not erased.

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Figure 56.8 State Transitions in Boot Mode (for the SCI Interface) is changed as follows:

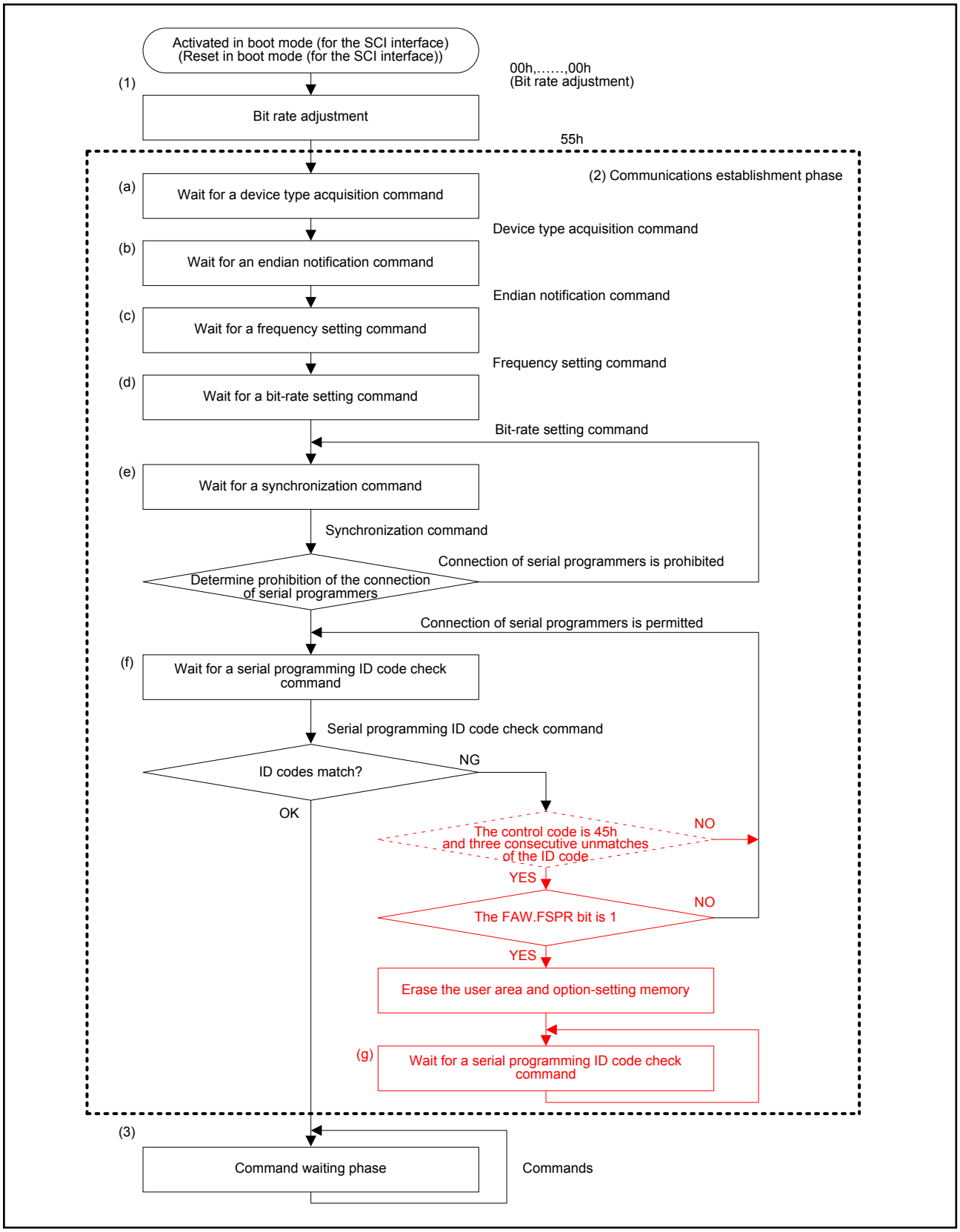

Figure 56.8 State Transition Flow in Boot Mode (for the SCI Interface)

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The descriptions of (f) Waiting for a serial programming ID code check command in (2) Communications establishment phase in section 57.11.2.1, State Transitions in Boot Mode (for the SCI Interface) are changed as follows:

Before correction

(f) Waiting for a serial programming ID code check command

In this state, the MCU is waiting for a serial programming ID code check command to be sent. The ID code sent from the host is compared with the ID code written in the option-setting memory area, and the command waiting phase is entered if the two match. If they do not match, the next transition is back to the state of waiting for a serial programming ID code check command. For details of the ID code check command, see section 56.11.15, Serial Programming ID Code Check Command.

After correction

(f) Waiting for a serial programming ID code check command

In this state, the MCU is waiting for a serial programming ID code check command to be sent. The code sent from the host is compared with the control code and ID code written in the option-setting memory area, and the MCU enters into the command waiting phase if the two match. If they do not match, the MCU enters back to the state of waiting for a serial programming ID code check command.
However, when the control code is 45h and if the codes do not match three times consecutively, all blocks in the user area and option-setting memory area are erased.*1
For details of the ID code check command, refer to section 56.11.15, Serial Programming ID Code Check Command.

Note 1. When the FAW.FSPR bit is 0, the blocks in those areas are not erased.

(g) Waiting for a serial programming ID code check command (after erasure)

After all blocks in the user area and option-setting memory area are erased, reboot the MCU in boot mode.

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Figure 56.9 State Transitions in Boot Mode (for the USB Interface) is changed as follows:

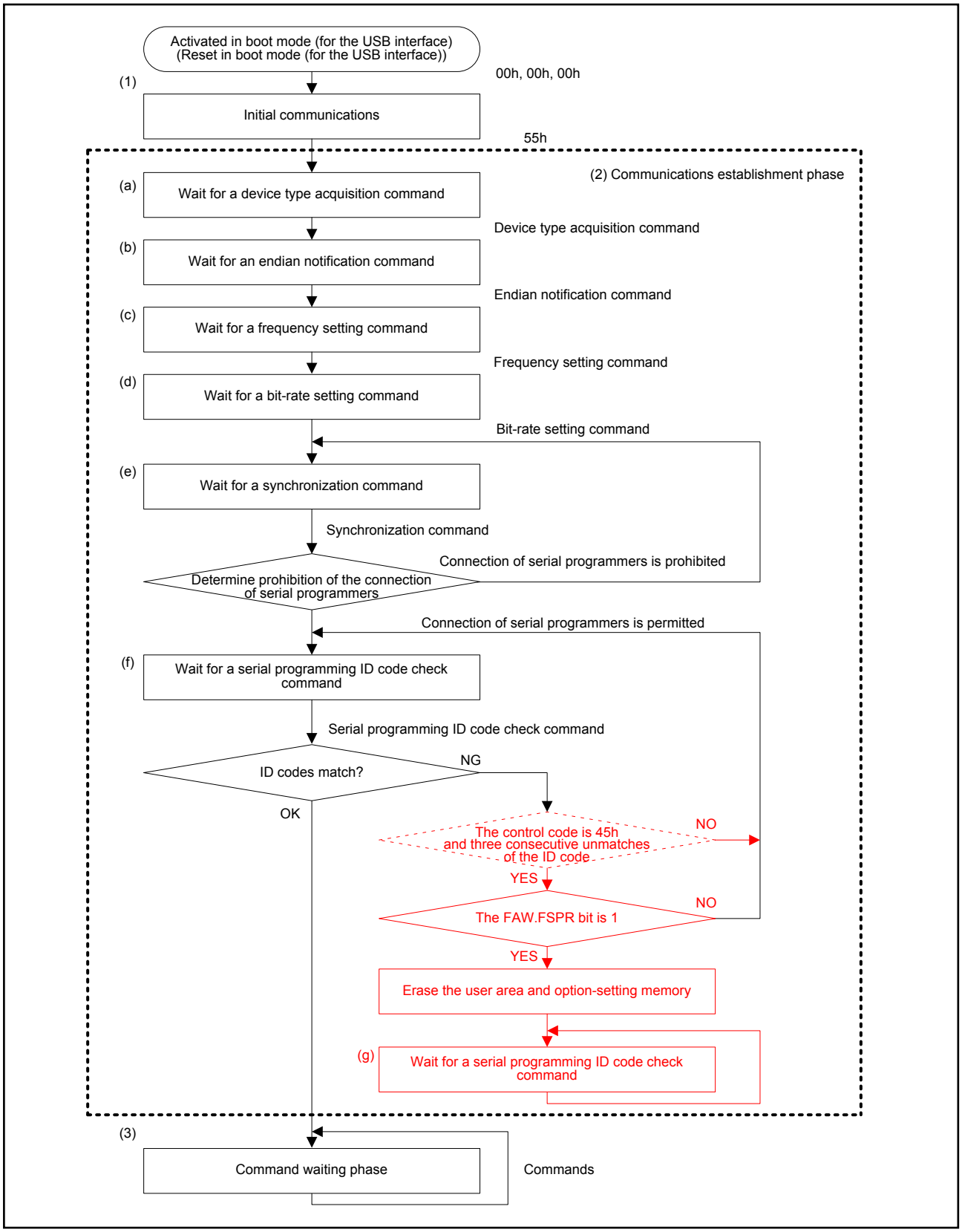

Figure 56.9 State Transition Flow in Boot Mode (for the USB Interface)

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The descriptions of (f) Waiting for a serial programming ID code check command in (2) Communications establishment phase in section 57.11.2.2, State Transitions in Boot Mode (for the USB Interface) are changed as follows:

Before correction

(f) Waiting for a serial programming ID code check command

In this state, the MCU is waiting for a serial programming ID code check command to be sent. The ID code sent from the host is compared with the ID code written in the option-setting memory area, and the command waiting phase is entered if the two match. If they do not match, the next transition is back to the state of waiting for a serial programming ID code check command. For details of the ID code check command, see section 56.11.15, Serial Programming ID Code Check Command.

After correction

(f) Waiting for a serial programming ID code check command

In this state, the MCU is waiting for a serial programming ID code check command to be sent. The code sent from the host is compared with the control code and ID code written in the option-setting memory area, and the MCU enters into the command waiting phase if the two match. If they do not match, the MCU enters back to the state of waiting for a serial programming ID code check command.
However, when the control code is 45h and if the codes do not match three times consecutively, all blocks in the user area and option-setting memory area are erased.*1
For details of the ID code check command, refer to section 56.11.15, Serial Programming ID Code Check Command.

Note 1. When the FAW.FSPR bit is 0, the blocks in those areas are not erased.

(g) Waiting for a serial programming ID code check command (after erasure)

After all blocks in the user area and option-setting memory area are erased, reboot the MCU in boot mode.

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The descriptions in the body of section 57.11.15, Serial Programming ID Code Check Command and the contents of (3) Status packet structure, error occurrence are changed as follows:

After correction

The MCU checks whether its own ID matches that sent from the host and notifies the host of the result.
This command can be accepted in the communications establishment phase. When ID authentication in boot mode is enabled, the MCU does not enter the command waiting phase unless processing in response to this command ends normally.
However, when the OCD/serial ID1 (control code) is 45h and if the codes do not match three times consecutively, all blocks in the user area and option-setting memory area are erased.*1
In this case, the Trusted Memory area is also erased*1 regardless of the setting of the Trusted Memory.

Note 1. When the FAW.FSPR bit is 0, the blocks in those areas are not erased.

(3) Status packet structure, error occurrence

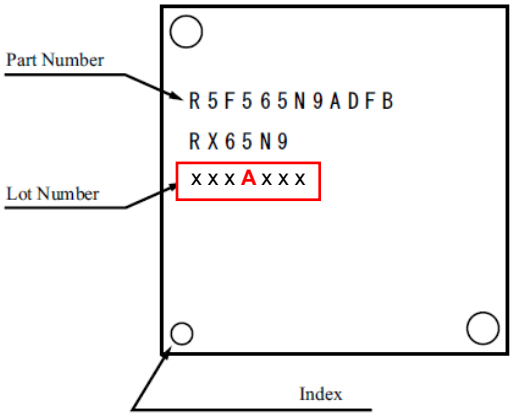
SOD	LNH	LNL	RES	ERR	SUM	ETX

SOD: 81h
LNH: 00h
LNL: 02h
RES: B0h (error)
ERR: Error code
C1h (packet error)
C2h (checksum error)
C3h (flow error)
DBh (ID code mismatch error)
E1h (erase error)
SUM: Sum of values
ETX: 03h

3. Applicable Products

The function is supported in all of the mass-produced products. A mass-produced product is identified by "**A**" in the fourth character from the left of the lot number.

Example of Marking Specification



Note 1. The above figure is an example of mark specification.
A part of the Part Number of real product is printed.

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