Customer Notification

78K0R/Fx3

16-Bit Single-Chip Microcontroller

Injected Current Specification

78K0R/FB3 Series

78K0R/FC3 Series

78K0R/FE3 Series

78K0R/FF3 Series

78K0R/FG3 Series

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Table of Contents

A) Related Products

List of related products:

78K0R/FB3

Non A-Version Products
μPD78F1804MCA, μPD78F1805MCA, μPD78F1806MCA, μPD78F1807MCA,
μPD78F1804MCA2, μPD78F1805MCA2, μPD78F1806MCA2, μPD78F1807MCA2

A-Version Products
μPD78F1804AMCA, μPD78F1805AMCA, μPD78F1806AMCA, μPD78F1807AMCA,
μPD78F1804AMCA2, μPD78F1805AMCA2, μPD78F1806AMCA2, μPD78F1807AMCA2

78K0R/FC3

Non A-Version Products
μPD78F1808K8A, μPD78F1809K8A, μPD78F1810K8A, μPD78F1811K8A,
μPD78F1808K8A2, μPD78F1809K8A2, μPD78F1810K8A2, μPD78F1811K8A2

A-Version Products
μPD78F1808AK8A, μPD78F1809AK8A, μPD78F1810AK8A, μPD78F1811AK8A,
μPD78F1808AK8A2, μPD78F1809AK8A2, μPD78F1810AK8A2, μPD78F1811AK8A2

Non A-version Products
μPD78F1812GAA, μPD78F1813GAA, μPD78F1814GAA, μPD78F1815GAA, μPD78F1816GAA,
μPD78F1817GAA, μPD78F1826GAA, μPD78F1827GAA, μPD78F1828GAA, μPD78F1829GAA,
μPD78F1830GAA,
μPD78F1812GAA2, μPD78F1813GAA2, μPD78F1814GAA2, μPD78F1815GAA2, μPD78F1816GAA2,
μPD78F1817GAA2, μPD78F1826GAA2, μPD78F1827GAA2, μPD78F1828GAA2, μPD78F1829GAA2,
μPD78F1830GAA2

A-Version Products
μPD78F1812AGAA, μPD78F1813AGAA, μPD78F1814AGAA, μPD78F1815AGAA,
μPD78F1816AGAA, μPD78F1817AGAA, μPD78F1826AGAA, μPD78F1827AGAA,
μPD78F1828AGAA, μPD78F1829AGAA, μPD78F1830AGAA, μPD78F1812AGAA2,
μPD78F1813AGAA2, μPD78F1814AGAA2, μPD78F1815AGAA2, μPD78F1816AGAA2,
μPD78F1817AGAA2, μPD78F1826AGAA2, μPD78F1827AGAA2, μPD78F1828AGAA2,
μPD 78F1829AGAA2, μPD78F1830AGAA2

Non A-version Products
μPD78F1812K8A, μPD78F1813K8A, μPD78F1814K8A, μPD78F1815K8A, μPD78F1816K8A,
μPD78F1817K8A, μPD78F1826K8A, μPD78F1827K8A, μPD78F1828K8A, μPD78F1829K8A,
μPD78F1830K8A
μPD78F1812K8A2, μPD78F1813K8A2, μPD78F1814K8A2, μPD78F1815K8A2, μPD78F1816K8A2,
μPD78F1817K8A2, μPD78F1826K8A2, μPD78F1827K8A2, μPD78F1828K8A2, μPD78F1829K8A2,
μPD78F1830K8A2

A-Version Products
μPD78F1812AK8A, μPD78F1813AK8A, μPD78F1814AK8A, μPD78F1815AK8A, μPD78F1816AK8A,
μPD78F1817AK8A, μPD78F1826AK8A, μPD78F1827AK8A, μPD78F1828AK8A, μPD78F1829AK8A,
μPD78F1830AK8A
μPD78F1812AK8A2, μPD78F1813AK8A2, μPD78F1814AK8A2, μPD78F1815AK8A2,
μPD78F1816AK8A2, μPD78F1817AK8A2, μPD78F1826AK8A2, μPD78F1827AK8A2,
μPD78F1828AK8A2, μPD78F1829AK8A2, μPD78F1830AK8A2

78K0R/FE3

Non A-Version Products

μPD78F1818GBA, μPD78F1819GBA, μPD78F1820GBA, μPD78F1821GBA, μPD78F1822GBA, μPD78F1831GBA, μPD78F1832GBA, μPD78F1833GBA, μPD78F1834GBA, μPD78F1835GBA, μPD78F1818GBA2, μPD78F1819GBA2, μPD78F1820GBA2, μPD78F1821GBA2, μPD78F1822GBA2, μPD78F1831GBA2, μPD78F1832GBA2, μPD78F1833GBA2, μPD78F1834GBA2, μPD78F1835GBA2

A-Version Products

μPD78F1818AGBA, μPD78F1819AGBA, μPD78F1820AGBA, μPD78F1821AGBA, μPD78F1822AGBA, μPD78F1831AGBA, μPD78F1832AGBA, μPD78F1833AGBA, μPD78F1834AGBA, μPD78F1835AGBA, μPD78F1818AGBA2, μPD78F1819AGBA2, μPD78F1820AGBA2, μPD78F1821AGBA2, μPD78F1822AGBA2, μPD78F1831AGBA2, μPD78F1832AGBA2, μPD78F1833AGBA2, μPD78F1834AGBA2, μPD78F1835AGBA2

78K0R/FF3

Non A-Version Products

μPD78F1823GKA, μPD78F1824GKA, μPD78F1825GKA, μPD78F1836GKA, μPD78F1837GKA, μPD78F1838GKA, μPD78F1839GKA, μPD78F1840GKA, μPD78F1823GKA2, μPD78F1824GKA2, μPD78F1825GKA2, μPD78F1836GKA2, μPD78F1837GKA2, μPD78F1838GKA2, μPD78F1839GKA2, μPD78F1840GKA2

A-Version Products

μPD78F1823AGKA, μPD78F1824AGKA, μPD78F1825AGKA, μPD78F1836AGKA, μPD78F1837AGKA, μPD78F1838AGKA, μPD78F1839AGKA, μPD78F1840AGKA μPD78F1823AGKA2, μPD78F1824AGKA2, μPD78F1825AGKA2, μPD78F1836AGKA2, μPD78F1837AGKA2, μPD78F1838AGKA2, μPD78F1839AGKA2, μPD78F1840AGKA2

78K0R/FG3

Non A-Version Products

μPD78F1841GCA, μPD78F1842GCA, μPD78F1843GCA, μPD78F1844GCA, μPD78F1845GCA, μPD78F1841GCA2, μPD78F1842GCA2, μPD78F1843GCA2, μPD78F1844GCA2, μPD78F1845GCA2

A-Version Products

μPD78F1841AGCA, μPD78F1842AGCA, μPD78F1843AGCA, μPD78F1844AGCA, μPD78F1845AGCA, μPD78F1841AGCA2, μPD78F1842AGCA2, μPD78F1843AGCA2, μPD78F1844AGCA2, μPD78F1845AGCA2

B) Electrical Specification for Injected Current

(**Ta = -40 to +125 °C**, V_{DD}=EV_{DD0}=EV_{DD1}=AV_{REF}= 2.7V to 5.5V, V_{SS}=EV_{SS0}= EV_{SS1}=AV_{SS}=0V) (Notes 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Pos. Injected Current $V_{IN} > V_{DD}$ (Peak) (Note 3, 5)	I_{INJP}	Per Digital input pin			5	mA
		Per Analog input pin (Note 2)			2	mA
Neg. Injected Current $V_{IN} < V_{SS}$ (Peak) (Note 5)	I_{INJN}	Per Digital input pin			-5	mA
		Per Analog input pin (Note 2)			-0.15	mA
Sum of all Positive Injected Currents (Peak) (Note 3, 4)	$\Sigma I_{INJP\ D}$	Sum for all Digital input pins			20	mA
	$\Sigma I_{INJP\ A}$	Sum for all Analog input pins (Note 2)			4	mA
Sum of all Negative Injected Currents (Peak) (Note 4)	$\Sigma I_{INJN\ D}$	Sum for all Digital input pins			-20	mA
	$\Sigma I_{INJN\ A}$	Sum for all Analog input pins (Note 2)			-0.6	mA
Total Sum of all Injected Currents (Positve and Negative) (Peak) (Note 3, 4)	$\Sigma \lvert I_{INJP\ D} \rvert + \Sigma \lvert I_{INJN\ D} \rvert$	Total Sum for all Digital input pins			20	mA
	$\Sigma \lvert I_{INJP\ A} \rvert + \Sigma \lvert I_{INJN\ A} \rvert$	Total Sum for all Analog input pins (Note 2)			4	mA
Pos. Injected Current (Digital Input) $V_{IN} > V_{DD}$ (Average) (Note 3, 6, 7)	$I_{INJPD\ AVG}$	Per Digital input pin			0.4	mA
	$\Sigma I_{INJPD\ AVG}$	Total Sum for all Digital input pins			4	mA
Pos. Injected Current (Analog Input) $V_{IN} > V_{DD}$ (Average) (Note 6, 7)	$I_{INJPA\ AVG}$	Per Analog input pin (Note 2)			0.15	mA
	$\Sigma I_{INJPA\ AVG}$	Total Sum for all Analog input pins (Note 2)			1	mA

Note 1: Only 78K0R/FG3(100pin) has EV_{DD1}, EV_{SS1}. For all other products EV_{DD0} is EV_{DD} and EV_{SS0} is EV_{SS}

Note 2: Analog pins for the product are as follows

Series				Analog input port
78K0R/Fx3	78K0R/FB3	30 pin	MC	P80/ANI00-P87/ANI07
		32 pin	K8	P80/ANI00-P85/ANI05
	78K0R/FC3	40 pin	K8	P80/ANI00-P87/ANI07
		48 pin	GA	P80/ANI00-P87/ANI07 P90/ANI08-P92/ANI10
			K8	
	78K0R/FE3	64 pin	GB	P80/ANI00-P87/ANI07 P90/ANI08-P96/ANI14
	78K0R/FF3	80 pin	GK	P80/ANI00-P87/ANI07 P90/ANI08-P97/ANI15
	78K0R/FG3	100 pin	GC	P80/ANI00-P87/ANI07 P90/ANI08-P97/ANI15 P100/ANI16-P107/ANI23

Note 3: The injection current specification ($V_{IN} > V_{DD} = I_{INJP}$) is not valid for the N-ch Open Drain ports (P60 – P63) and not for P121 to P124, because these port pins don't have the protection Diode to V_{DD}.

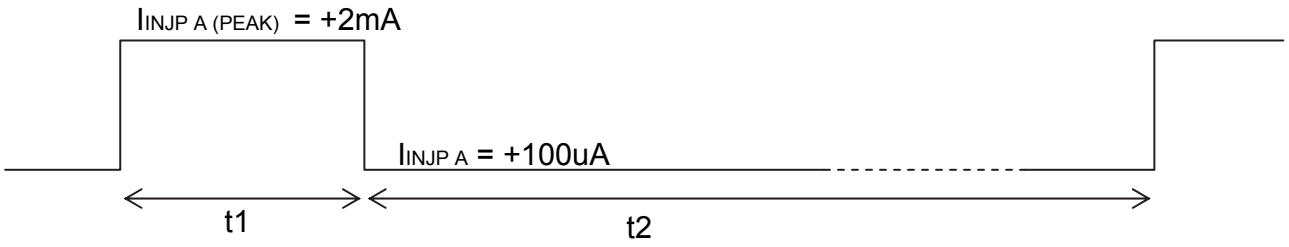
Note 4: If the Sum of the Injected Currents specifications (Peak values) are exceed even momentarily, there is a possibility to destroy the device.

Note 5: If any of the above Injected Current specifications (Peak values) are exceeded even momentarily, there is a possibility to destroy the device.

Note 6: When the Injected Current value exceeds the allowed Injected Current value (Average value), the electrical characteristics can't be specified.

Note 7: If the allowed Injected Current value (Average value) is exceeded permanently, the product life time could be influenced.
However, when the injected current exceed the Average value but is **still below** the Peak value the product life time will not be influenced if the injected current will follow the example as given here:

Example for an Analog Input:



Requirement :

$I_{INJPA\ AVG} \leq (I_{INJP\ A\ (PEAK)} \times t1) + (I_{INJ\ P\ A} \times t2) / (t1 + t2) \leq 150uA$

$I_{INJPA\ AVG} \leq (2mA \times t1) + (100uA \times t2) / (t1 + t2) \leq 150uA$

Remark :

The above mentioned example could also be used for the digital input pins with $I_{INJPD\ AVG} \leq 400uA$

Cautions:

1. An Injected Current conditions occur, if the standard operating conditions are exceeded.
   Example: The input voltage on any pin exceeds the specified range:
   $V_{IN} > EV_{DD} / V_{DD} / AV_{REF} + 0.3\ V \rightarrow (I_{INJP} > 0)$ or
   $V_{IN} < EV_{SS} / V_{SS} / AV_{SS} - 0.3\ V \rightarrow (I_{INJN} < 0)$.
   I_{INJP}, I_{INJN} = Injected current value that doesn't influence to the operation of the device.
2. The supply voltages must always remain within the specified limits.
3. A proper operation is not specified if an Injected Current occurs on the functional pins such as P121/X1, P122/X2/EXCLK, P123, P124/EXCLKS, P120/EXLVI/INTP0/TI11/TO11, RESET and FLMD0.
4. The above specifications are not tested in the outgoing inspection, but they are specified based on the design rules and the device characterization.

C) The influence on an adjacent pin caused by the Injected Current

(**Ta = -40 to +125 °C**, V_{DD}=EV_{DD0}=EV_{DD1}=AV_{REF}= 2.7V to 5.5V, V_{SS}=EV_{SS0}= EV_{SS1}=AV_{SS}=0V) (Notes 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Leakage current coupling factor for a Positive Injected Current	K_{INJP}	Digital input pins			5×10^{-3}	-
		Analog input pins (Note 2)			1×10^{-4}	-
Leakage current coupling factor for a Negative Injected Current	K_{INJN}	Digital input pins (Except P121 to P124)			1×10^{-2}	-
		Digital input pins (P121 to P124)			3.8×10^{-2}	-
		Analog input pins (Note 2)			3.2×10^{-3}	-

Note 1: Only 78K0R/FG3(100pin) has $EV_{DD1,}$ EV_{SS1}. For all other products EV_{DD0} is EV_{DD} and EV_{SS0} is EV_{SS}

Note 2: Analog pins for the product are as follows

Series				Analog input port
78K0R/Fx3	78K0R/FB3	30 pin	MC	P80/ANI00-P87/ANI07
		32 pin	K8	P80/ANI00-P85/ANI05
	78K0R/FC3	40 pin	K8	P80/ANI00-P87/ANI07
		48 pin	GA	P80/ANI00-P87/ANI07 P90/ANI08-P92/ANI10
			K8	
	78K0R/FE3	64 pin	GB	P80/ANI00-P87/ANI07 P90/ANI08-P96/ANI14
	78K0R/FF3	80 pin	GK	P80/ANI00-P87/ANI07 P90/ANI08-P97/ANI15
	78K0R/FG3	100 pin	GC	P80/ANI00-P87/ANI07 P90/ANI08-P97/ANI15 P100/ANI16-P107/ANI23

Cautions:

1. An Injected Current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (I_{LIH} / I_{LIL}) of the adjacent pins.
2. The amount of error leakage current depends on the Injected Current and it is defined by the coupling factor K_{INJ}.
3. The total leakage current through a pin is $| I_{Ltotal} | = | I_{LIH} / I_{LIL} | + (| I_{INJn} | \times K_{INJn})$
4. The additional error current may affect the input voltage on the analog inputs.
5. These specifications are not tested in the outgoing inspection, but it is specified based on the design rules and the device characterization.

D) Valid Specification

Item	Date published	Document No.	Document Title
1	July 2011 or later	R01UH0007EJ0500 or later	User's Manual: Hardware

E) Revision History

Item	Date published	Document No.	Comment
1	January 30 , 2012	R01TU0031ED0100	1st Release

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