

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A197A/E	Rev.	1.00
Title	Disclosure of the Electrical Characteristics for SD Host Interface (SDHI) in RX231 Group		Information Category	Technical Notification		
Applicable Product	RX231 Group	Lot No.	Reference Document	RX230 Group, RX231 Group User's Manual: Hardware Rev.1.10 (R01UH0496EJ0110)		
		All				

This document discloses the AC characteristics for the SD host interface (SDHI) in the RX231 group. The disclosed details are as follows.

## Table 1. SDHI Timing

Conditions:  $2.7\text{ V} \leq \text{VCC} = \text{VCC\_USB} = \text{AVCC0} \leq 3.6\text{ V}$ ,  $\text{VSS} = \text{AVSS0} = \text{VSS\_USB} = 0\text{ V}$ ,  $\text{fPCLKB} \leq 32\text{ MHz}$ ,

$T_a = -40\text{ to }+105^\circ\text{C}$

when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 1
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	-18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

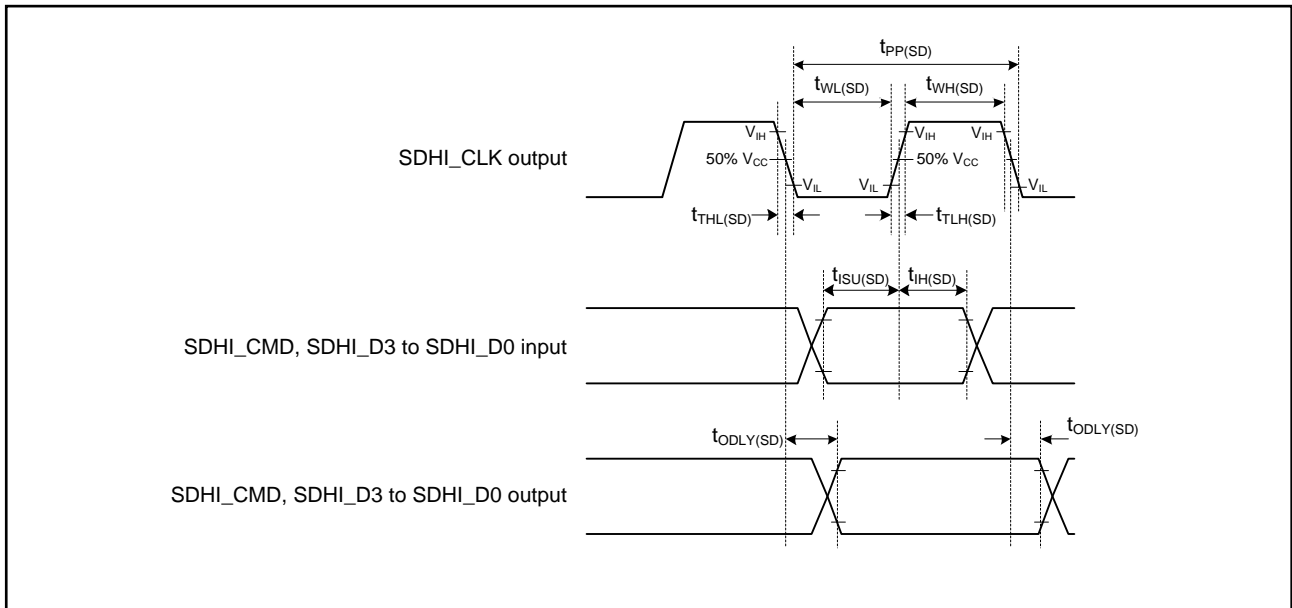


Figure 1. SD Host Interface Input/Output Signal Timing