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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A892A/E	Rev.	1.00
Title	Added the Description on the SDRAM Mode Register of the Bus State Controller (BSC)		Information Category	Technical Notification		
Applicable Product	• SH7286 Group	Lot No. All lots	Reference Document	• SH7280 Group, SH7243 Group User's Manual: Hardware Rev.3.00 (R01UH0229EJ0300)		

Regarding the bus state controller (BSC) in the above applicable products, we would like to inform you of the additional description on the SDRAM mode register.

Description on the SDRAM Mode Register

9.5.6 SDRAM Interface

Added:

Table 9.18 Access Address in SDRAM Mode Register Write

- Setting for Area 2

Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC4440	H'0000440
	3	H'FFFC4460	H'0000460
32 bits*	2	H'FFFC4880	H'0000880
	3	H'FFFC48C0	H'00008C0

Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC4040	H'0000040
	3	H'FFFC4060	H'0000060
32 bits*	2	H'FFFC4080	H'0000080
	3	H'FFFC40C0	H'00000C0

- Setting for Area 3

Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5440	H'0000440
	3	H'FFFC5460	H'0000460
32 bits*	2	H'FFFC5880	H'0000880
	3	H'FFFC58C0	H'00008C0

Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5040	H'0000040
	3	H'FFFC5060	H'0000060
32 bits*	2	H'FFFC5080	H'0000080
	3	H'FFFC50C0	H'00000C0

When a mode register write command is issued, the outputs of the external address pins are as follows.

When the data bus width of the area connected to SDRAM is 32 bits*	A15 to A9	0000000 (burst read/burst write) 0000100 (burst read/single write)
	A8 to A6	010 (CAS latency 2), 011 (CAS latency 3)
	A5	0 (lap time = sequential)
	A4 to A2	000 (burst length 1)
When the data bus width of the area connected to SDRAM is 16 bits	A14 to A8	0000000 (burst read/burst write) 0000100 (burst read/single write)
	A7 to A5	010 (CAS latency 2), 011 (CAS latency 3)
	A4	0 (lap time = sequential)
	A3 to A1	000 (burst length 1)

Note: * The 32-bit bus width is supported on the SH7286 only.