## MX0141KA1AVW

1:4 High-Speed Memory Bus MUX

The MX0141KA1AVW is $1: 4$ high-speed MUX that is comprised of a high-speed 1:4 multiplexer (mux) path and a low speed multi-function control logic path.

The high-speed path consists of four passive switches that connects input port IN to four output ports A, B, C, and D. Each ports is 16-bit. The passive switches, which closed selectively, form a bidirectional multiplexer.

The low-speed path consists of active multi-function IOs that can be configured in different modes. This path also can be configured as unidirectional 1:4 mux with a 4-bit port width, 4:16 decoder, or 16-bit signals for port selection. The CIO pins can be used to drive Chip Enable pins of the NAND dies or highspeed mux selector.

Both high-speed and low-speed paths support SSTL_12 and SSTL_18 signaling.

## Block Diagram



## Typical Applications

- SSD drive memory expansion or load reduction for both ONFI3/4 and TOGGLE NAND Flash system
- General-purpose bus 1:4 multiplexer for highspeed, low-power product solutions


## Main Features

- 1:4 high bandwidth 16 bit bus multiplexer
- SSTL18 and SSTL12 signaling
. $4 \times 11 \mathrm{~mm}$ FCCSP package with $0.65 / 0.5 \mathrm{~mm}$ ball pitch


## High-Speed MUX Features

- Bidirectional passive port switches
- Pull-up/Pull-down/Tristate/bus-hold for deselected ports
- Pin-to-pin output skew < 30ps (within a port)
- Pin-to-pin output skew < 10ps (Differential pairs)
- Propagation delay < 150ps
- Insertion loss $<1 \mathrm{~dB}$ at 800 MHz
- Bus holding, weak pull-down, or weak pull-up for deselected ports in different configurations via the CFG pins


## Low-Speed MUX/Control Logic Features

- 4-bit in, 16 -bit input/output logic targeted for Chip Enables or port selections
- Multiplexing or decoding
- Unidirectional, active multiplexing
- Multiple function selected via the CFG pins

Table 1. Characteristics of High-Speed Paths

| Feature | High-Speed Path |
| :---: | :---: |
| Port speed | Up to 1600MT/s |
| Port size | 16-bit |
| Direction | Bidirectional IN $\leftarrow \mathrm{A}, \mathrm{B}, \mathrm{C}$, or D |
| Control pins | SEL[1:0], ENB, ENCB, CIN[3:0], <br> CIO[15:0] |
| Signaling through port | SSTL_12, SSTL_18 |

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