

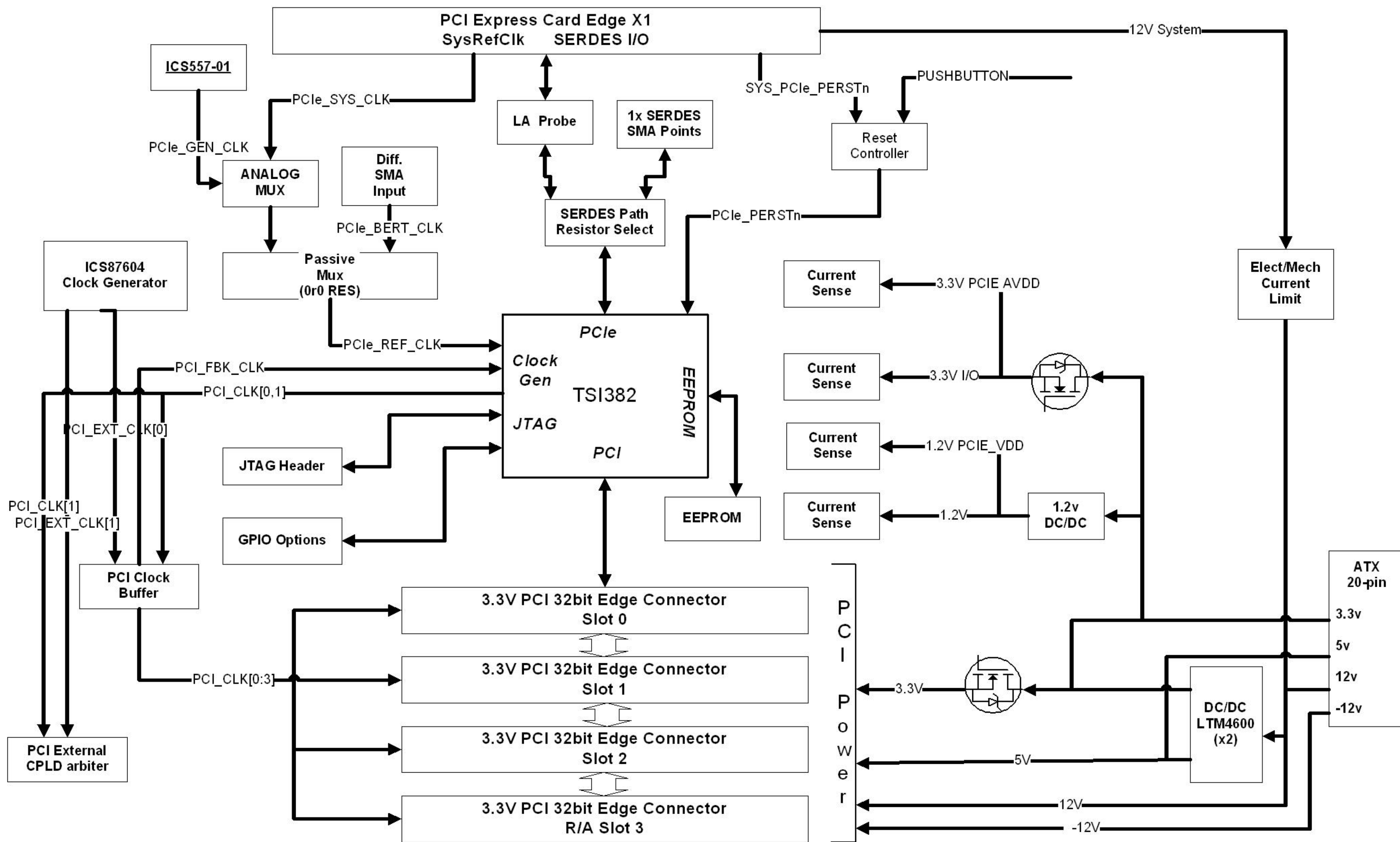
# Tsi382 (LQFP) Evaluation Board Schematics

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C	60E2020_SC001	1.0	PHILIP LAUZON
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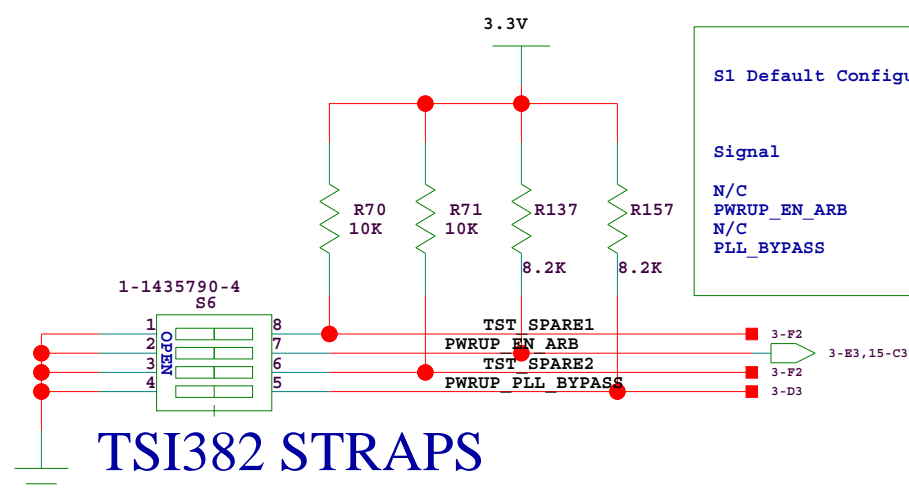
# BLOCK DIAGRAM



TITLE : <b>BLOCK DIAGRAM</b>			
SIZE : <b>C</b>	DRAWING NUMBER : <b>60E2020_SC001</b>	Version : <b>1.0</b>	DESIGNER : <b>PHILIP LAUZON</b>
LAST MODIFIED DATE : <b>6-12-2008_15:42</b>		SHEET <b>2</b> OF <b>15</b>	

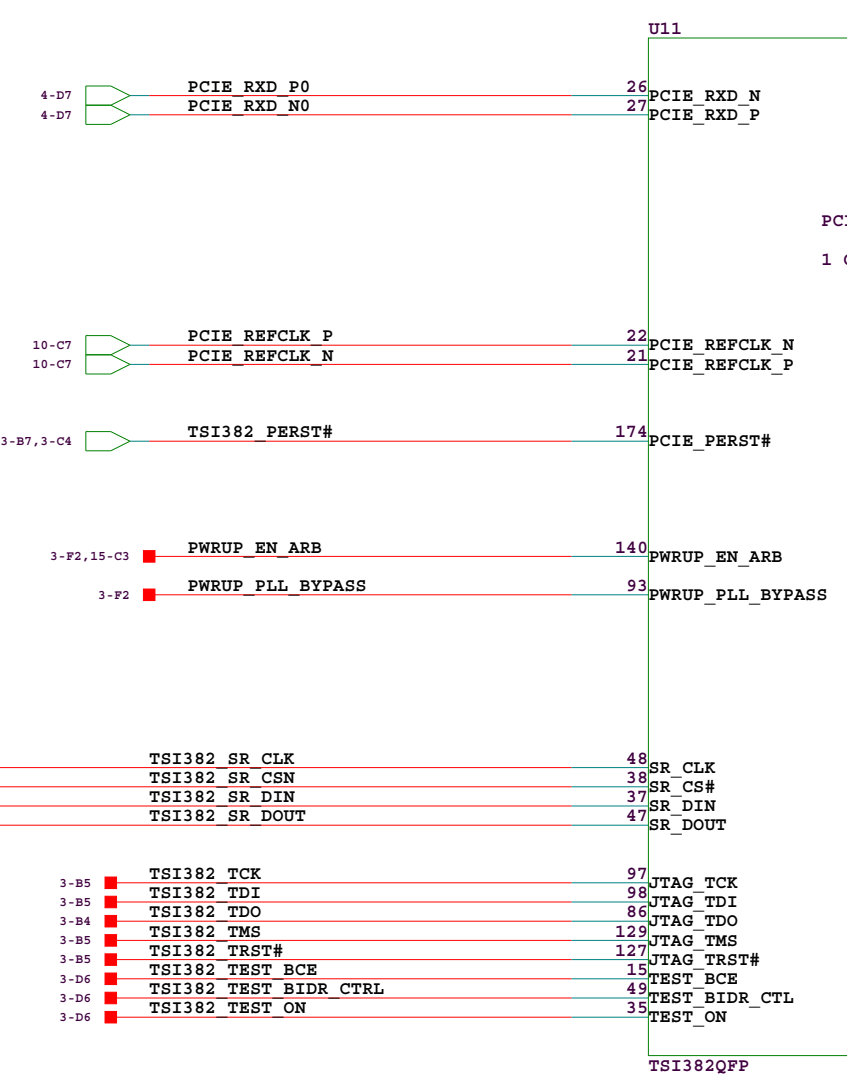
# TSI382 PCIE/MISC INTERFACE

## TSI382 STRAPS

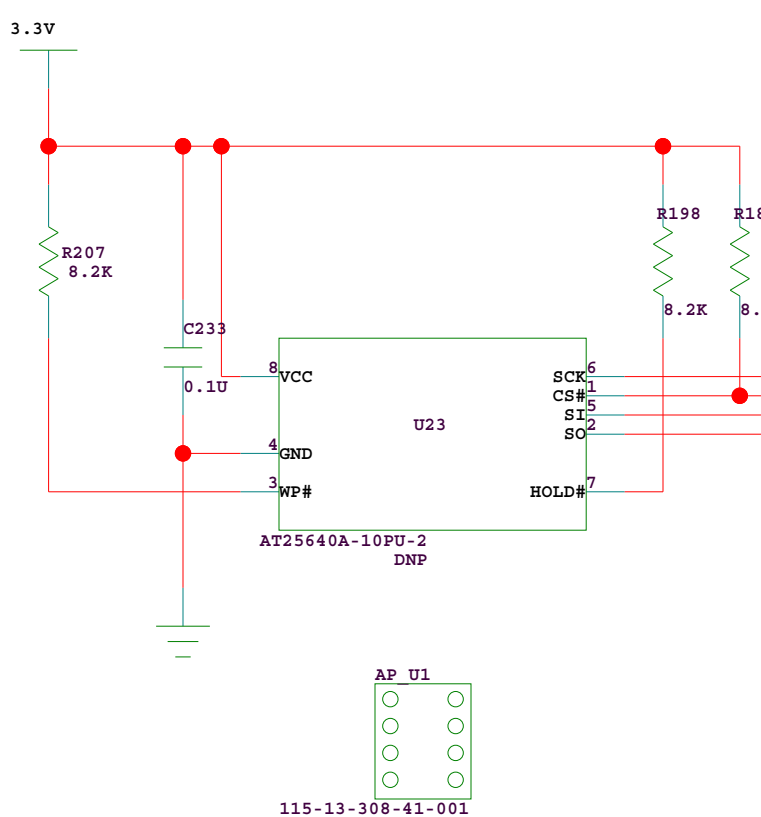
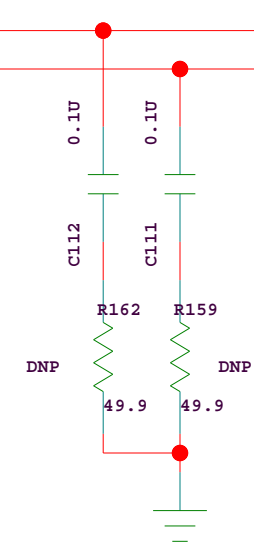


S1 Default Configuration

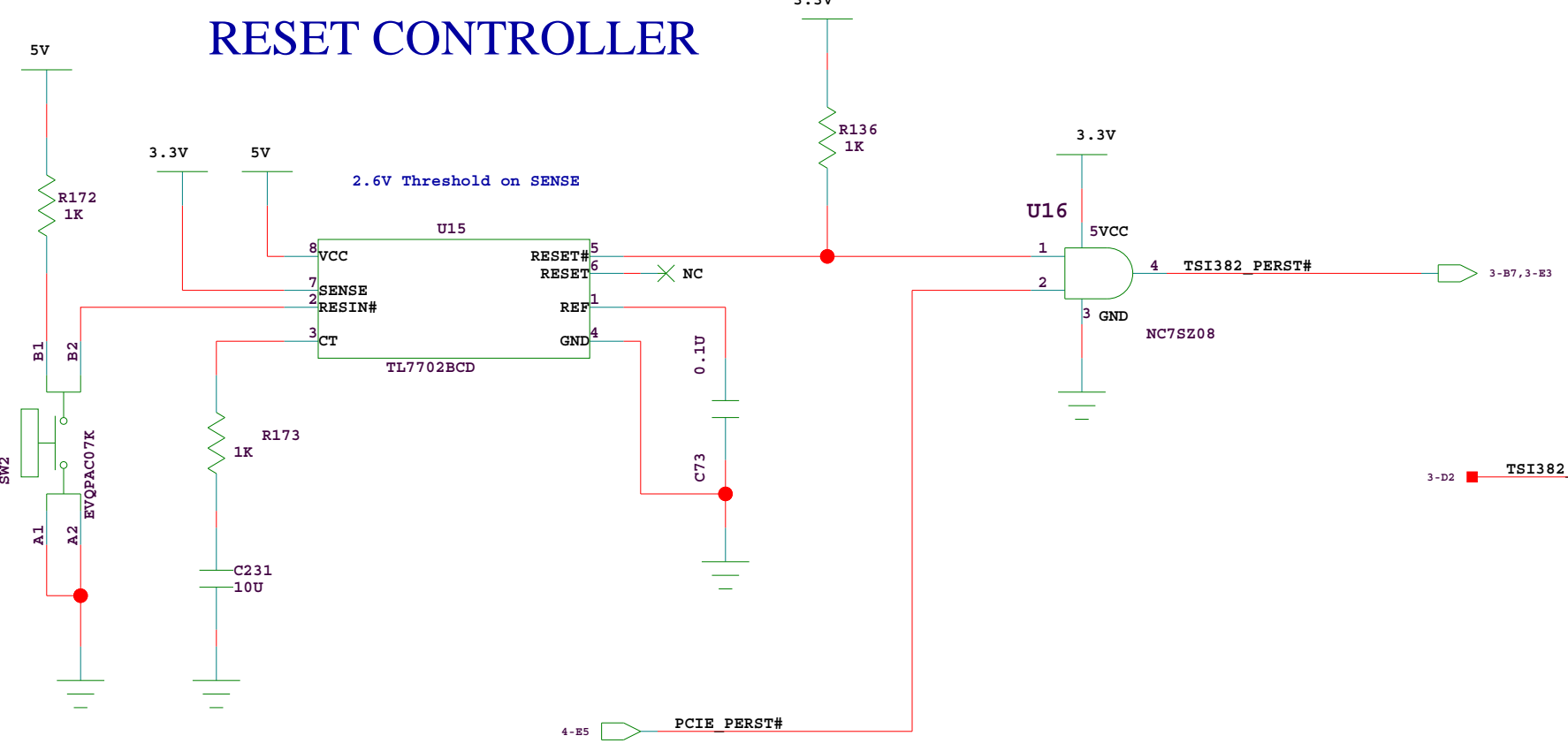
Signal	(1=High,0=Low)
N/C	
PWRUP_EN_ARB	0
N/C	
PLL_BYPASS	0



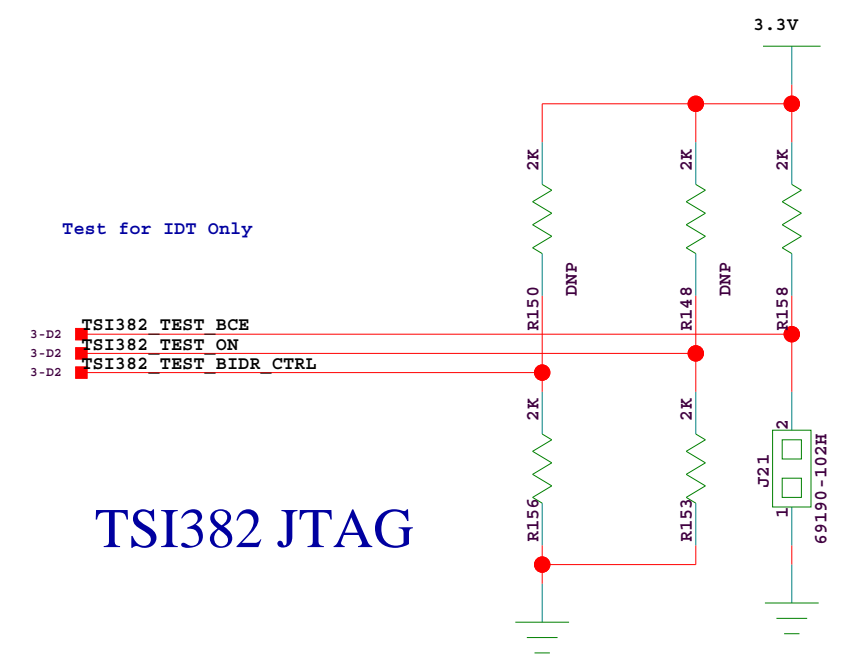
## TX Compliance Testing



## RESET CONTROLLER

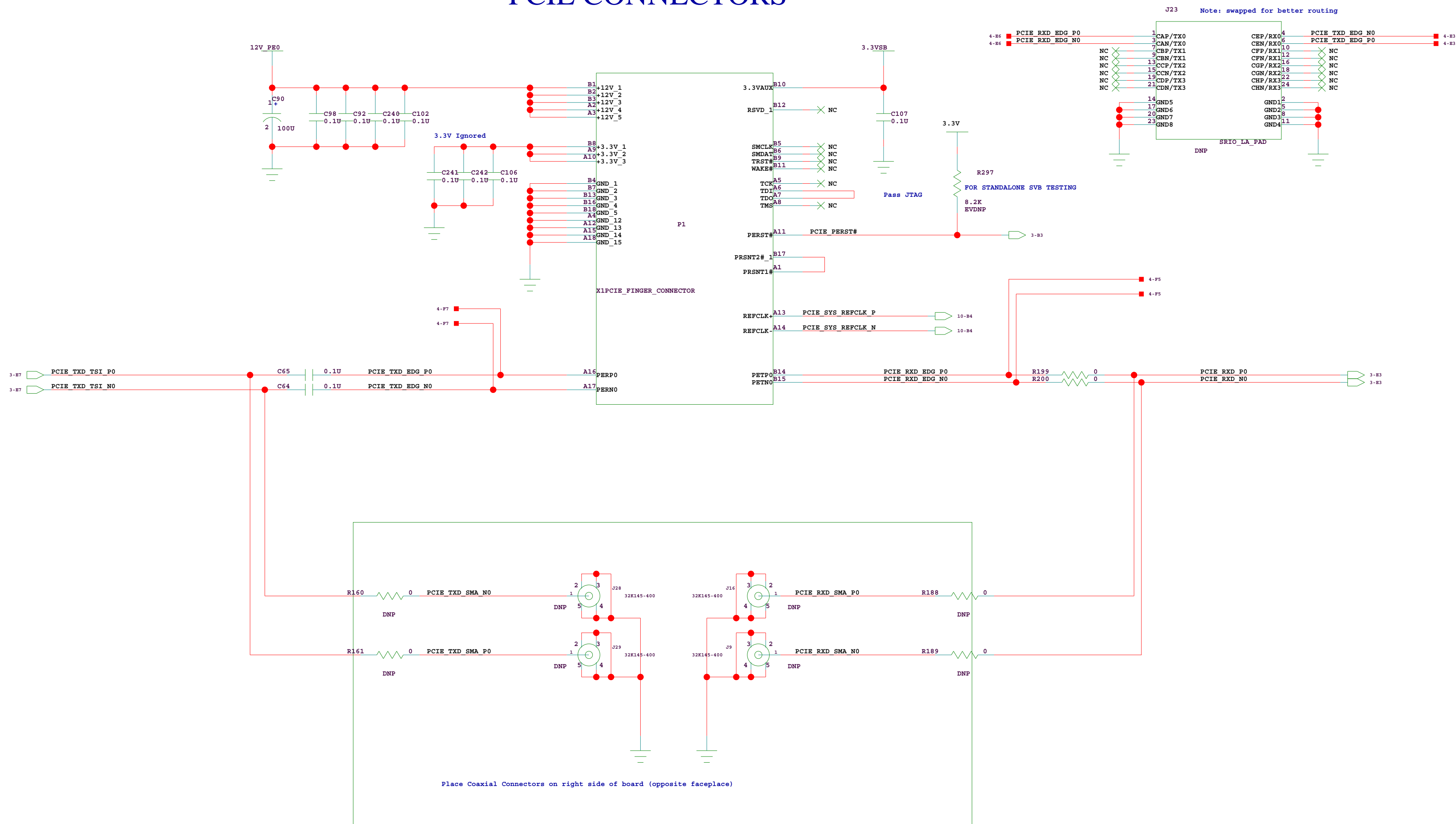


## TSI382 JTAG



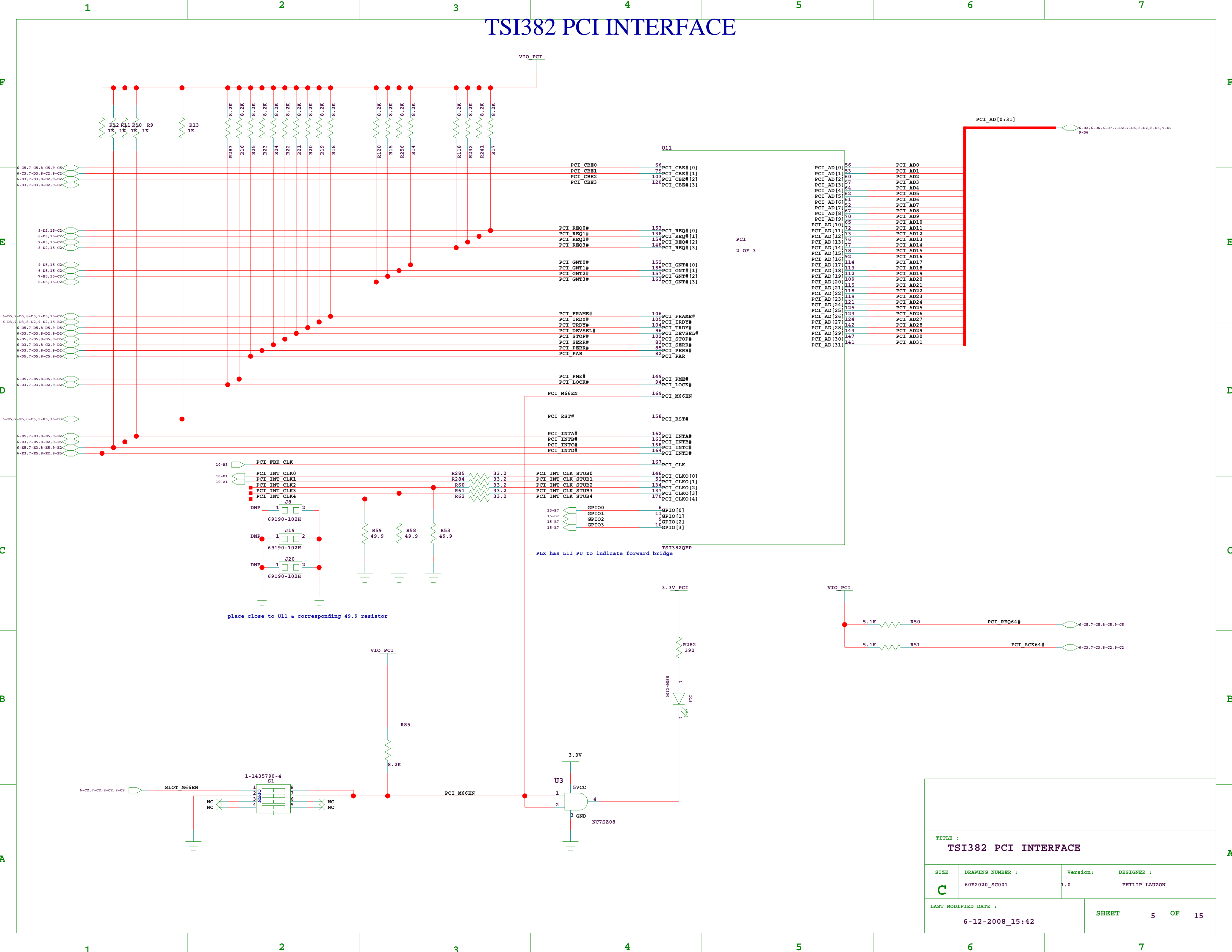
TITLE : <b>TSI382 PCIE/MISC</b>			
SIZE <b>C</b>	DRAWING NUMBER : 60E2020_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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# PCIE CONNECTORS



TITLE :			
PCIE CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2020_SC001	1.0	PHILIP LAUZON
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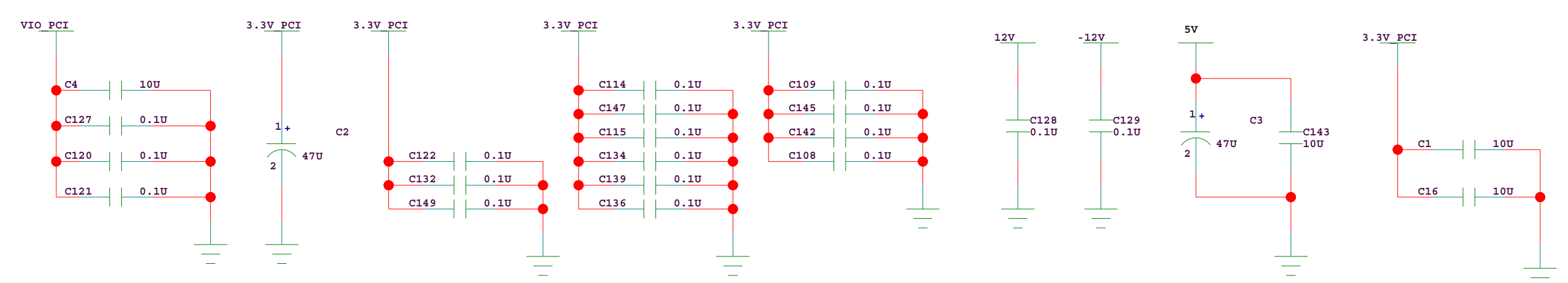
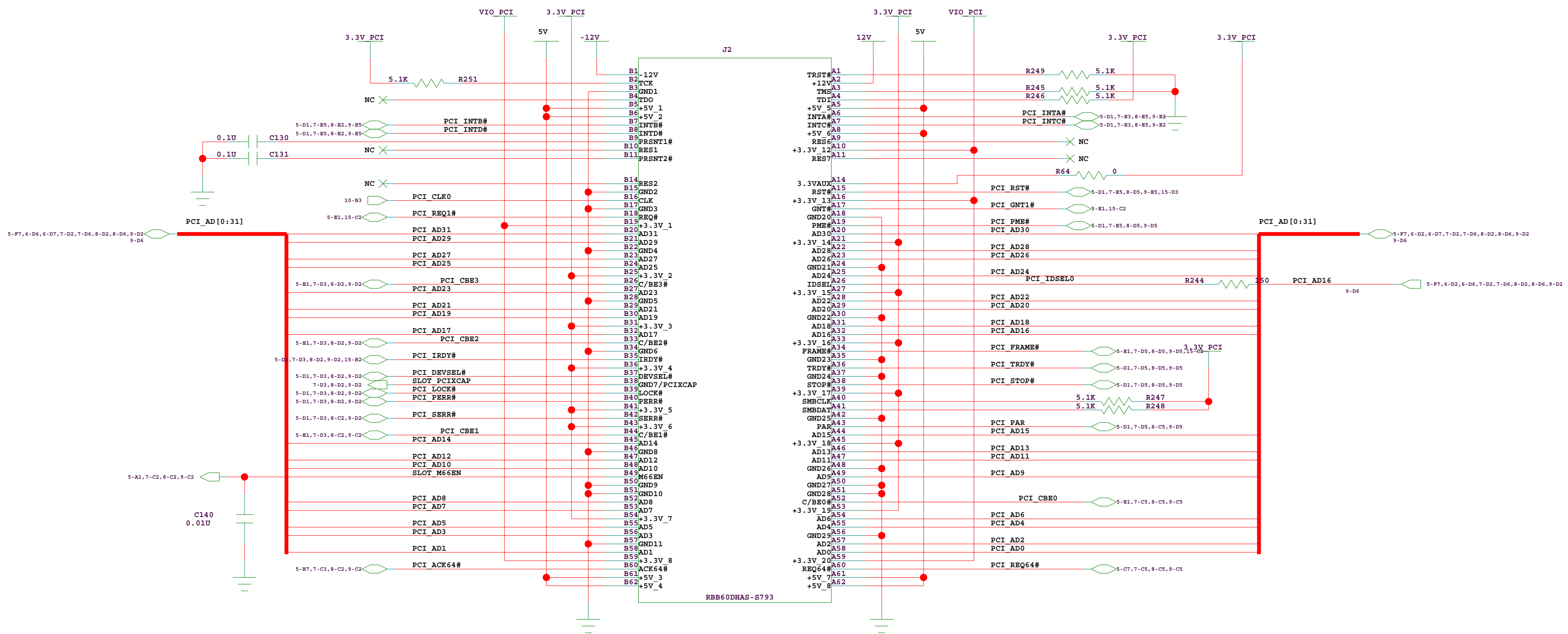
# TSI382 PCI INTERFACE



TITLE : <b>TSI382 PCI INTERFACE</b>			
SIZE <b>C</b>	DRAWING NUMBER : 60E2020_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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# PCI SLOT 0 (R/A)

IDSEL AD16  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTA  
 INTB -> INTB  
 INTC -> INTC  
 INTD -> INTD  
 - PCI Clock PCI\_CLK0  
 - PCI Arbitration PCI\_GNT#1/PCI\_REQ#1



TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# PCI SLOT 1 (Vertical)

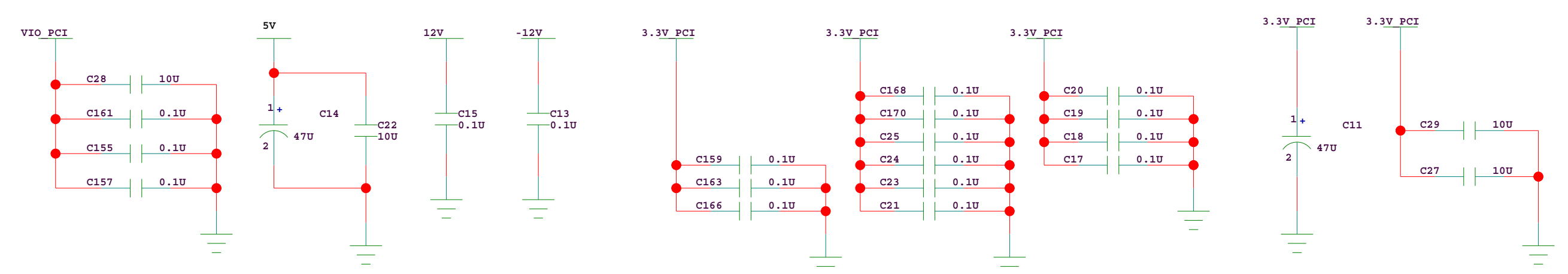
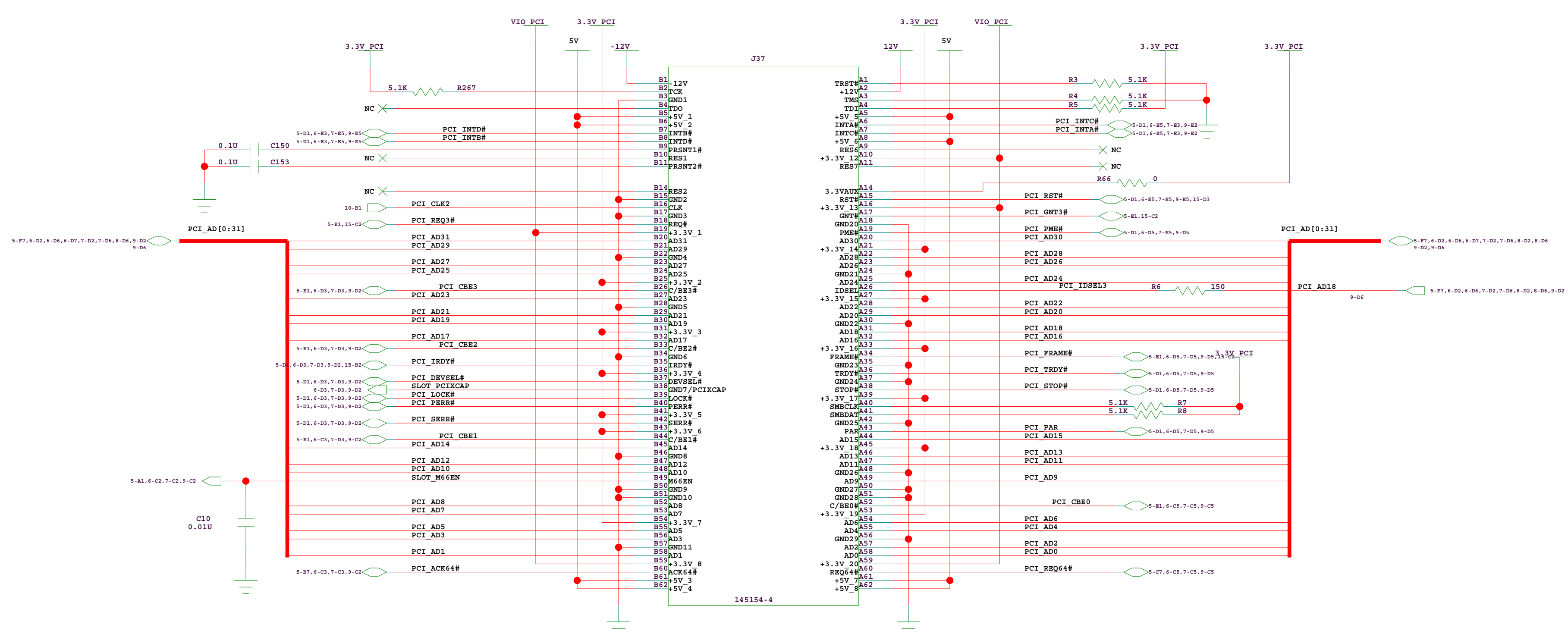
**IDSEL AD17**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTB  
 INTB -> INTC  
 INTC -> INTD  
 INTD -> INTA  
 - PCI Clock PCI\_CLK1  
 - PCI Arbitration PCI\_GNT2#/PCI\_REQ#2



TITLE :			
PCI SLOT 1			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# PCI SLOT 3 (Vertical)

**IDSEL AD18**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTC  
 INTB -> INTD  
 INTC -> INTA  
 INTD -> INTB  
  
 - PCI Clock PCI\_CLK2  
  
 - PCI Arbitration PCI\_GNT#3/PCI\_REQ#3

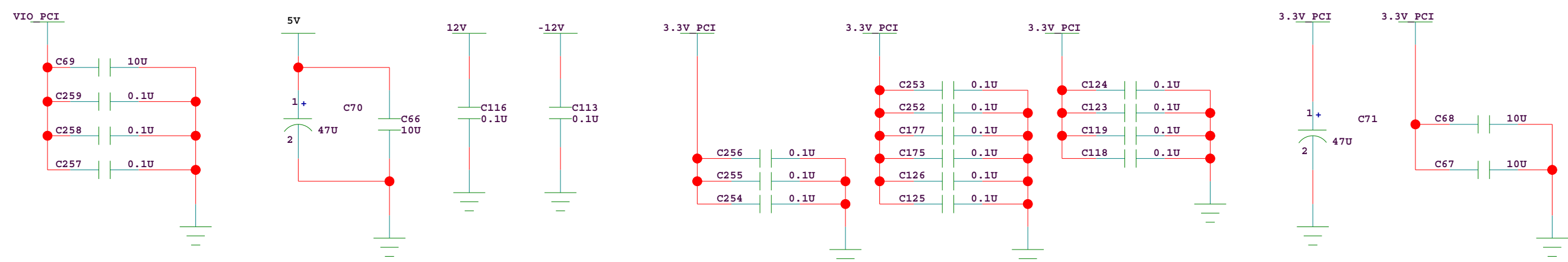
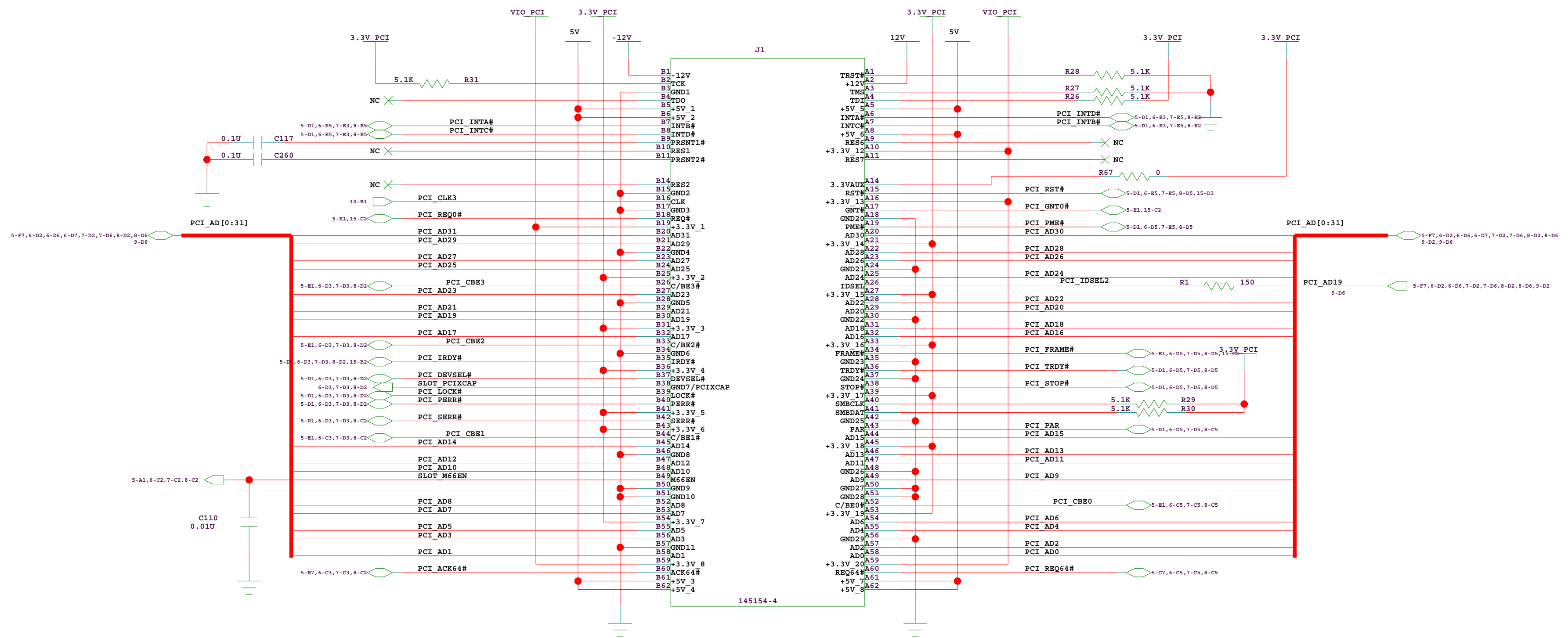


TITLE : <b>PCI SLOT 3</b>			
SIZE : <b>C</b>	DRAWING NUMBER : 60E2020_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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# PCI SLOT 2 (Vertical)

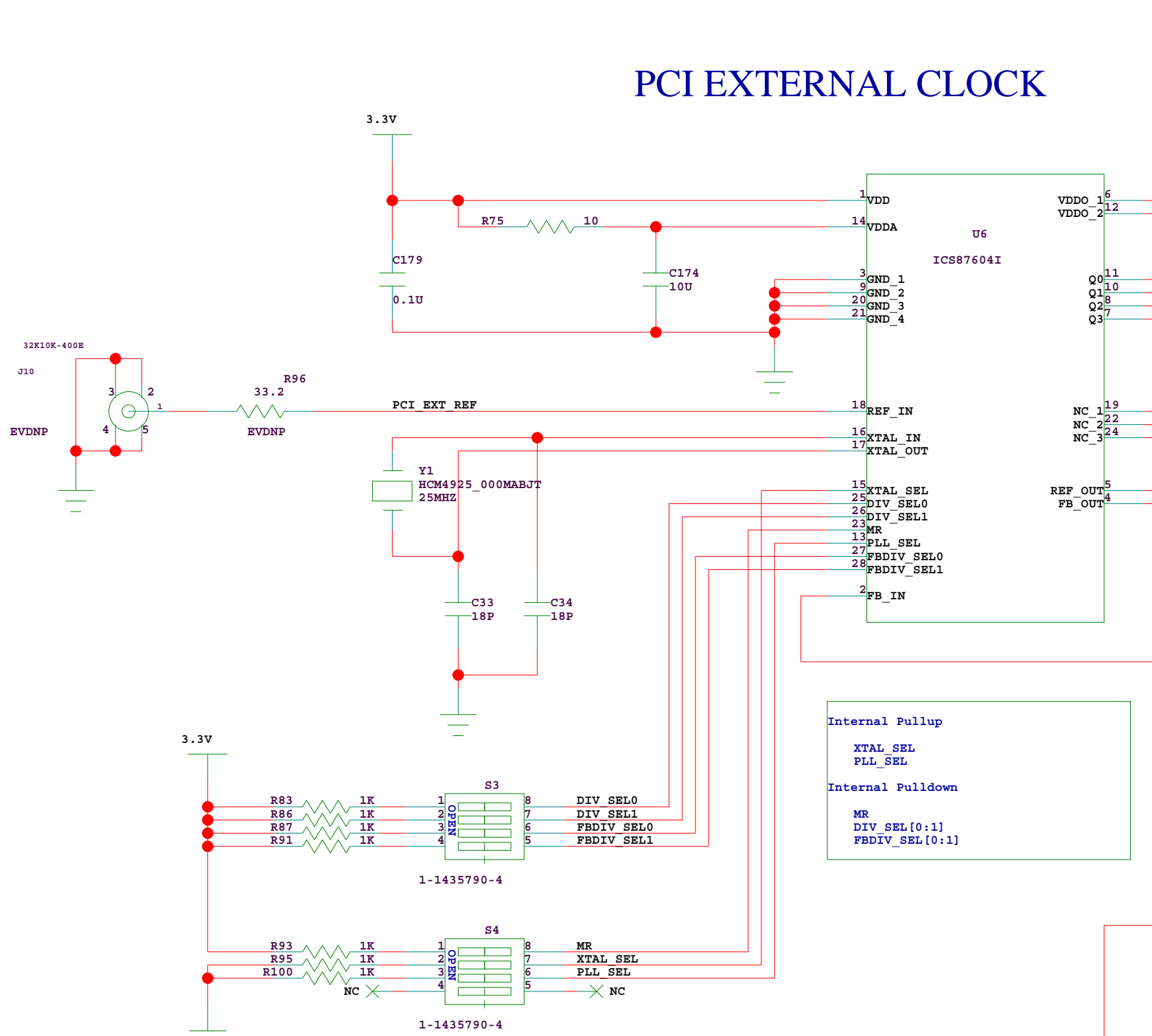
**IDSEL AD19**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTD  
 INTB -> INTA  
 INTC -> INTB  
 INTD -> INTC  
  
 - PCI Clock PCI\_CLK3  
  
 - PCI Arbitration PCI\_GNT0#/PCI\_REQ#0



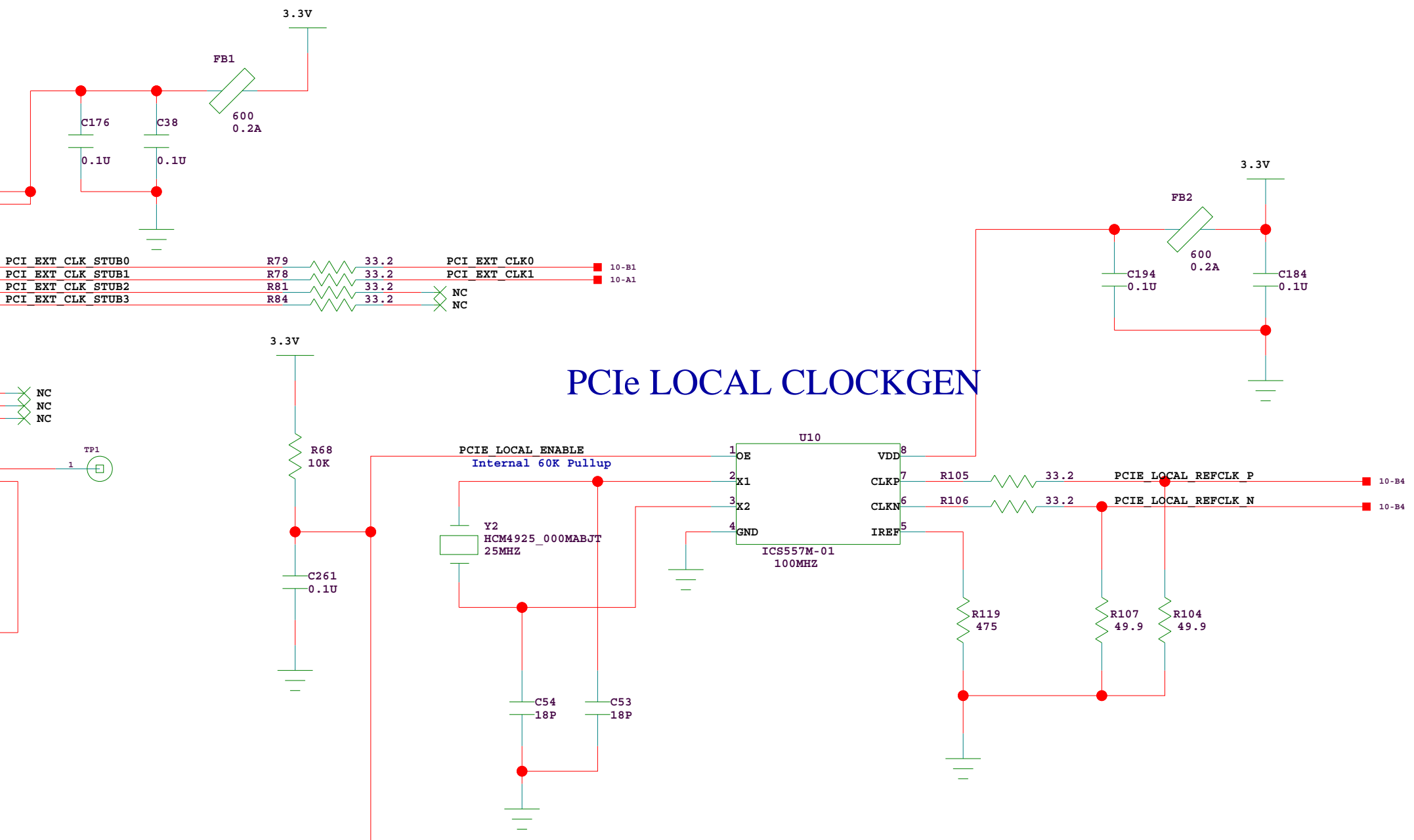
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PCI SLOT 2			
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# CLOCK DISTRIBUTION

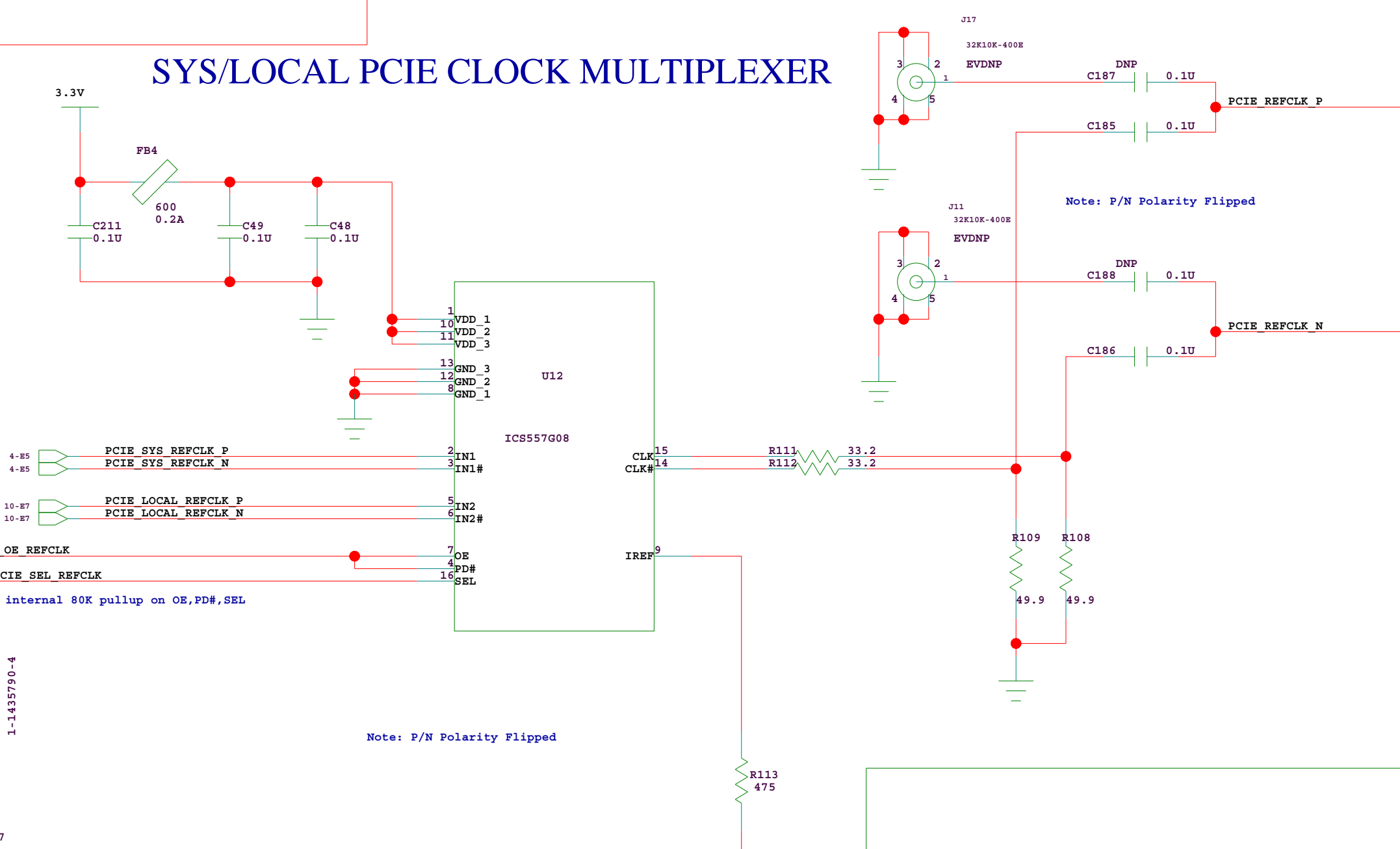
## PCI EXTERNAL CLOCK



## PCIe LOCAL CLOCKGEN



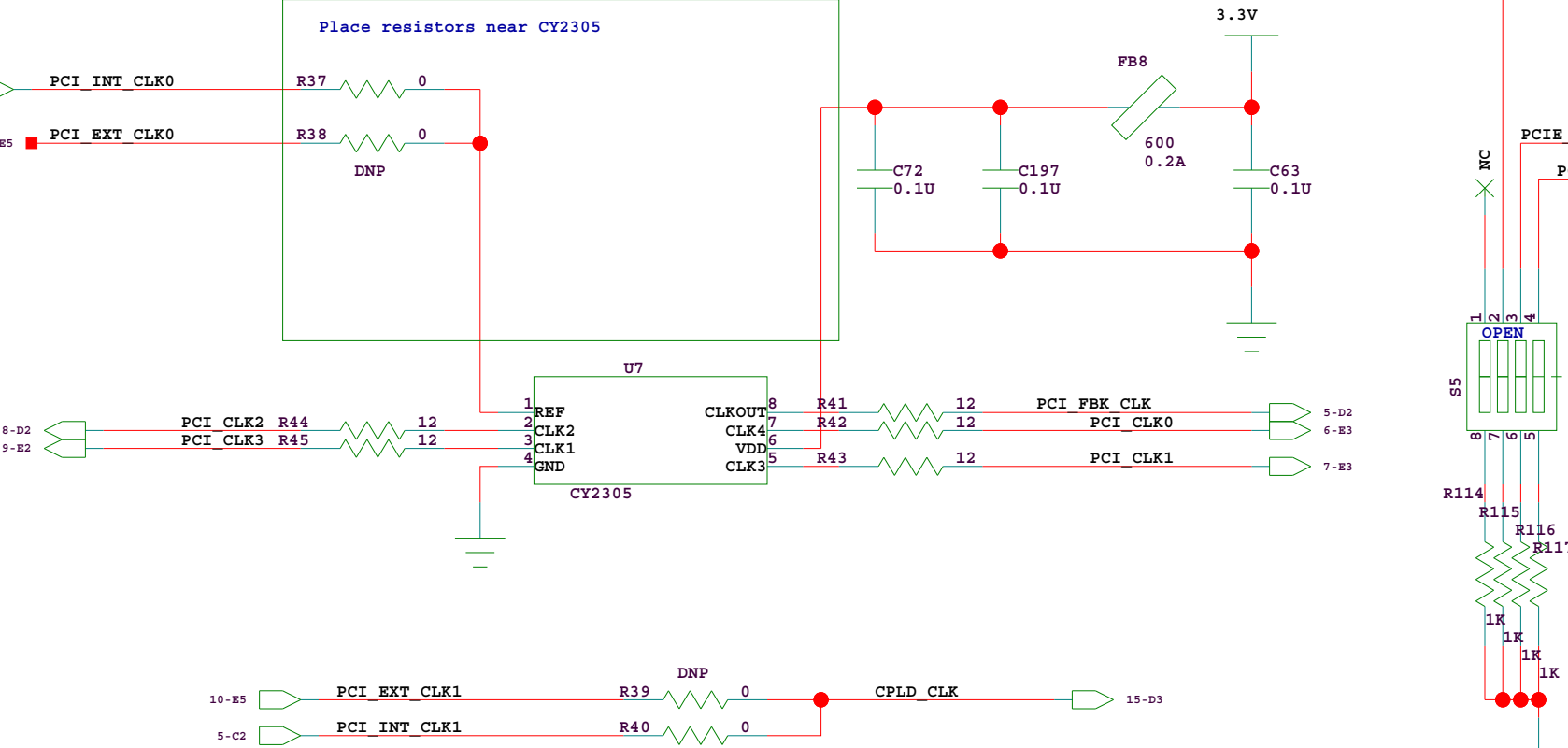
## SYS/LOCAL PCIe CLOCK MULTIPLEXER



Frequency Select (ICS87604I)

FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

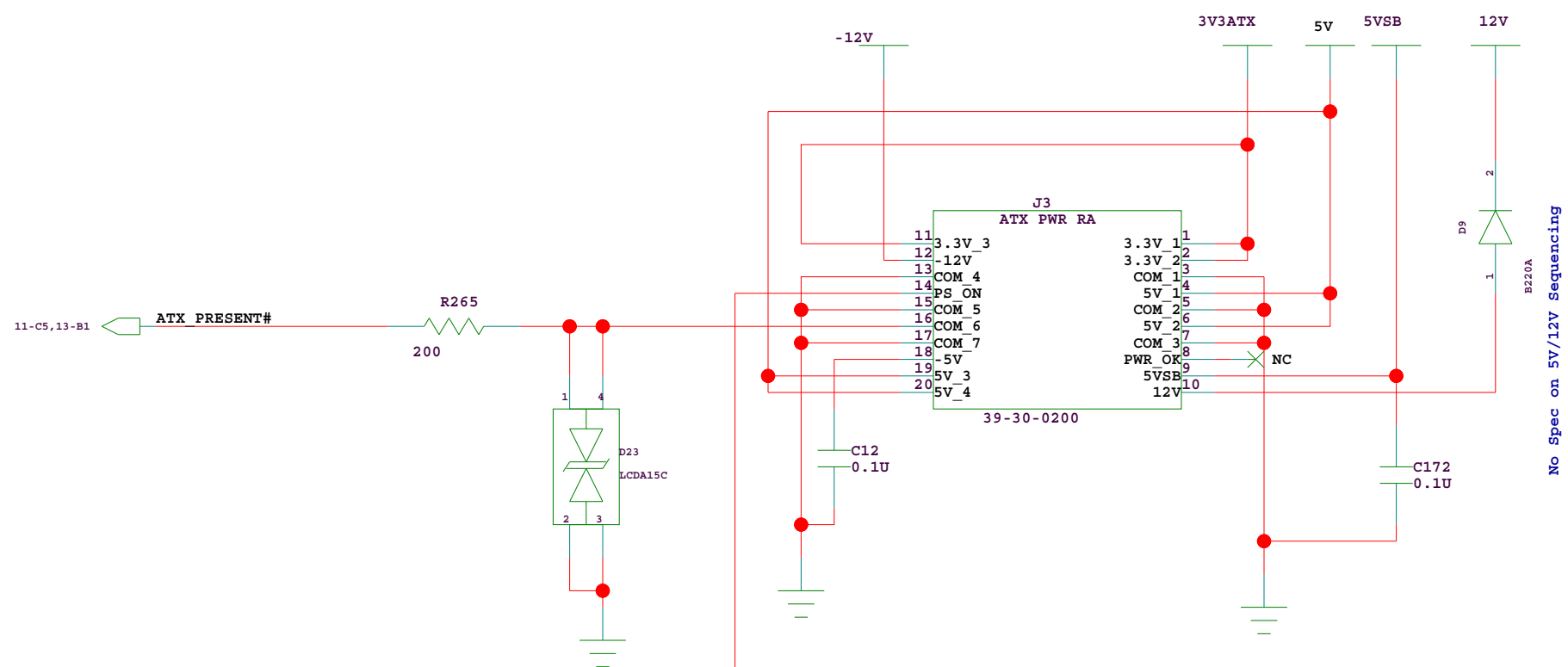
Place resistors near CY2305



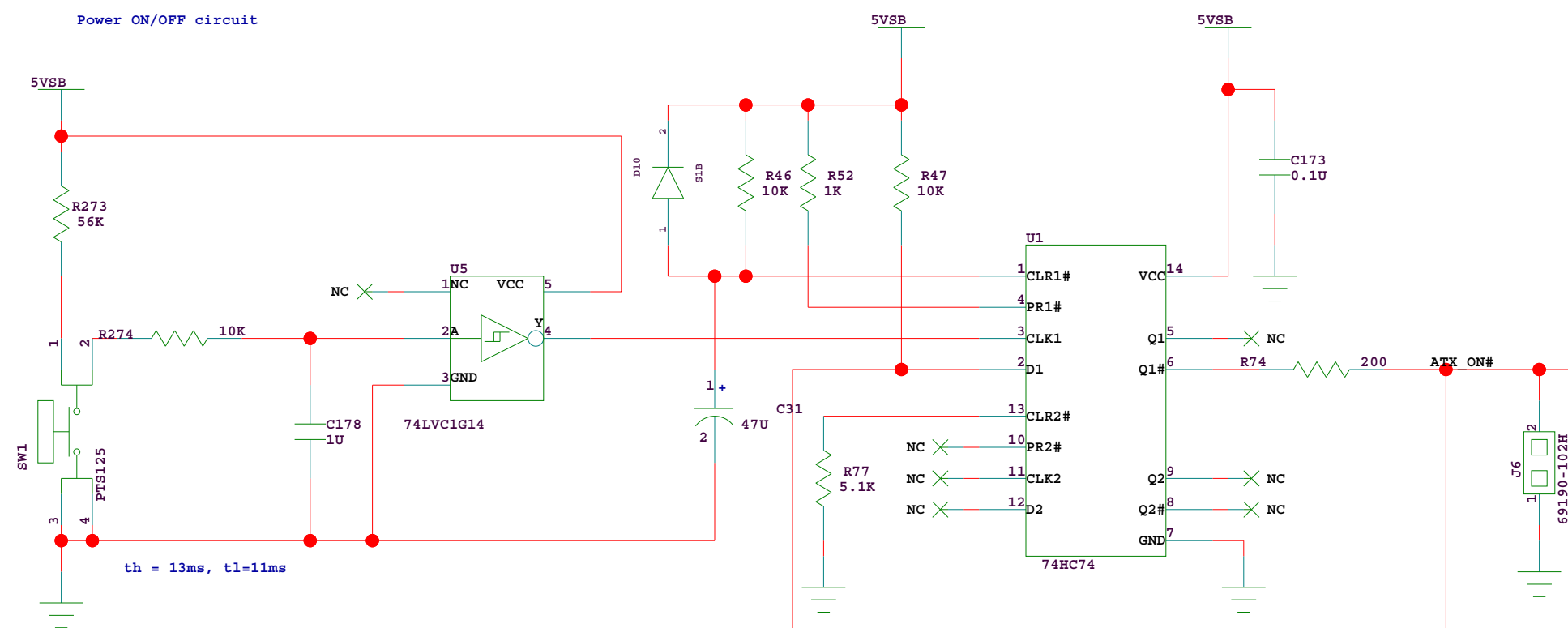
TITLE :			
CLOCK DISTRIBUTION			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# POWER SOURCES

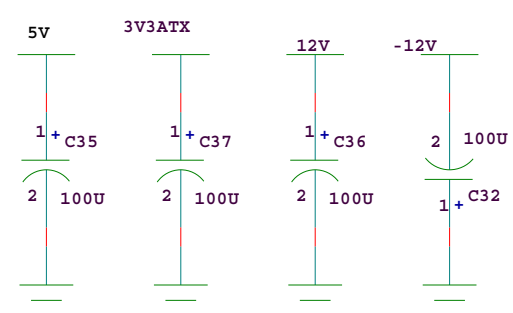
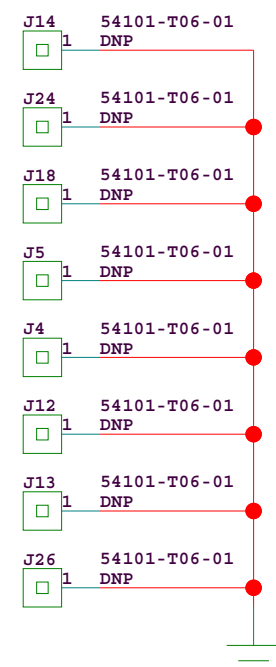
## ATX



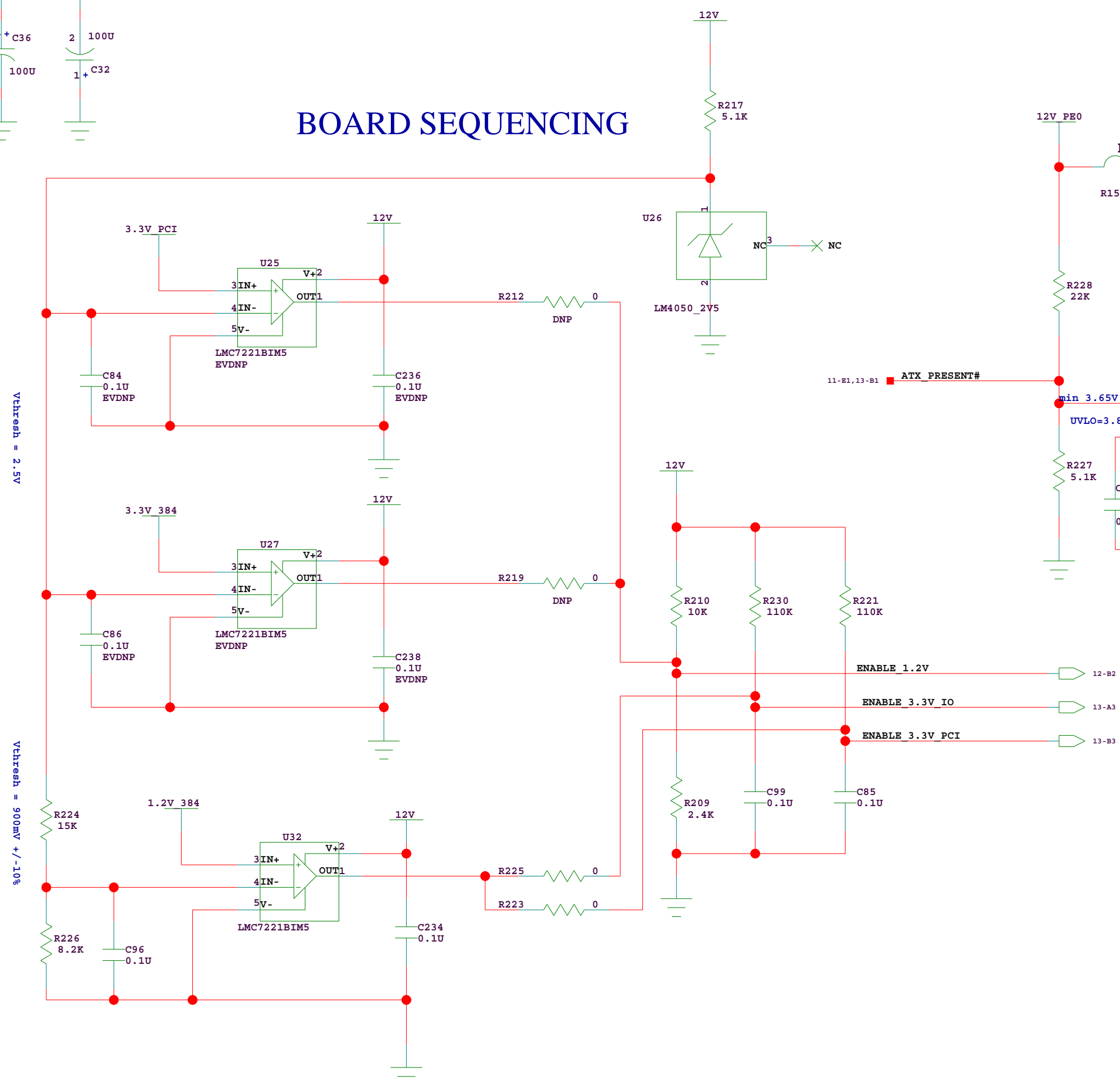
## ATX SUPPLY TOGGLE



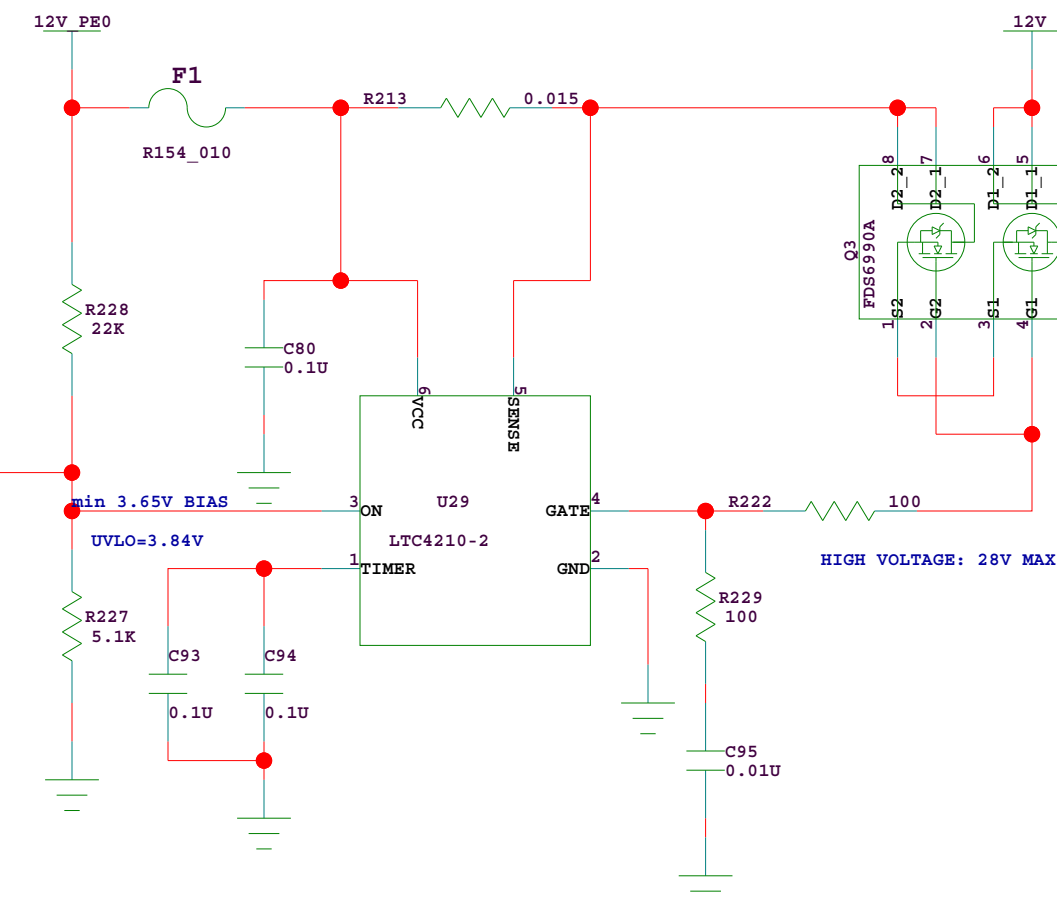
## GND TESTPOINTS



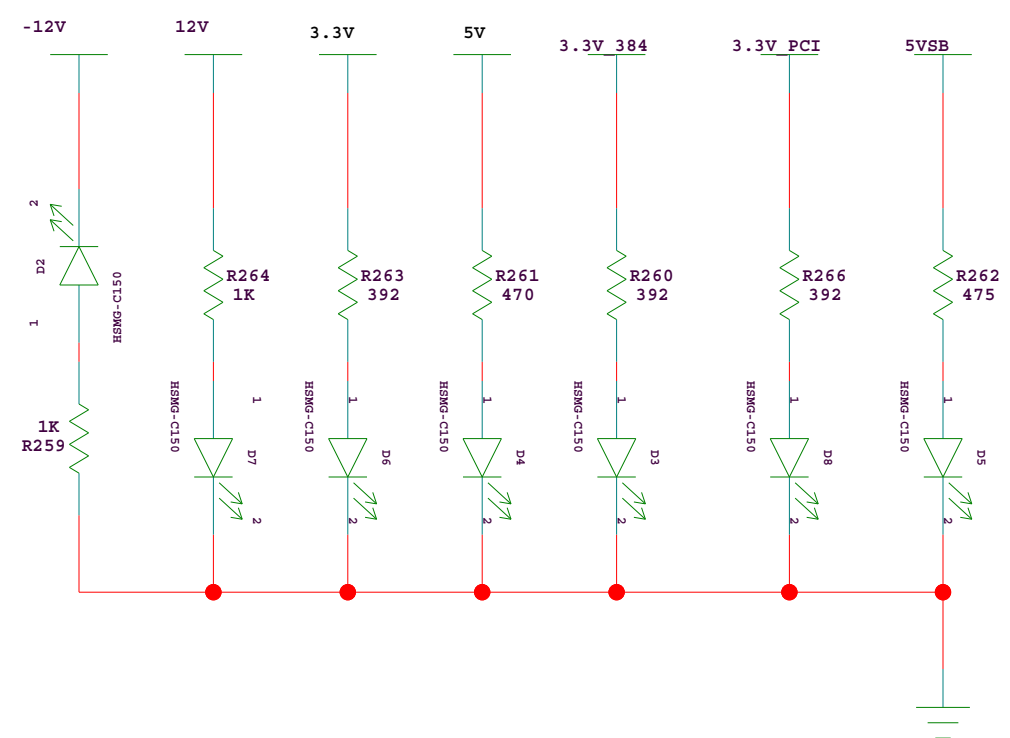
## BOARD SEQUENCING



## SYS SUPPLY SWITCH

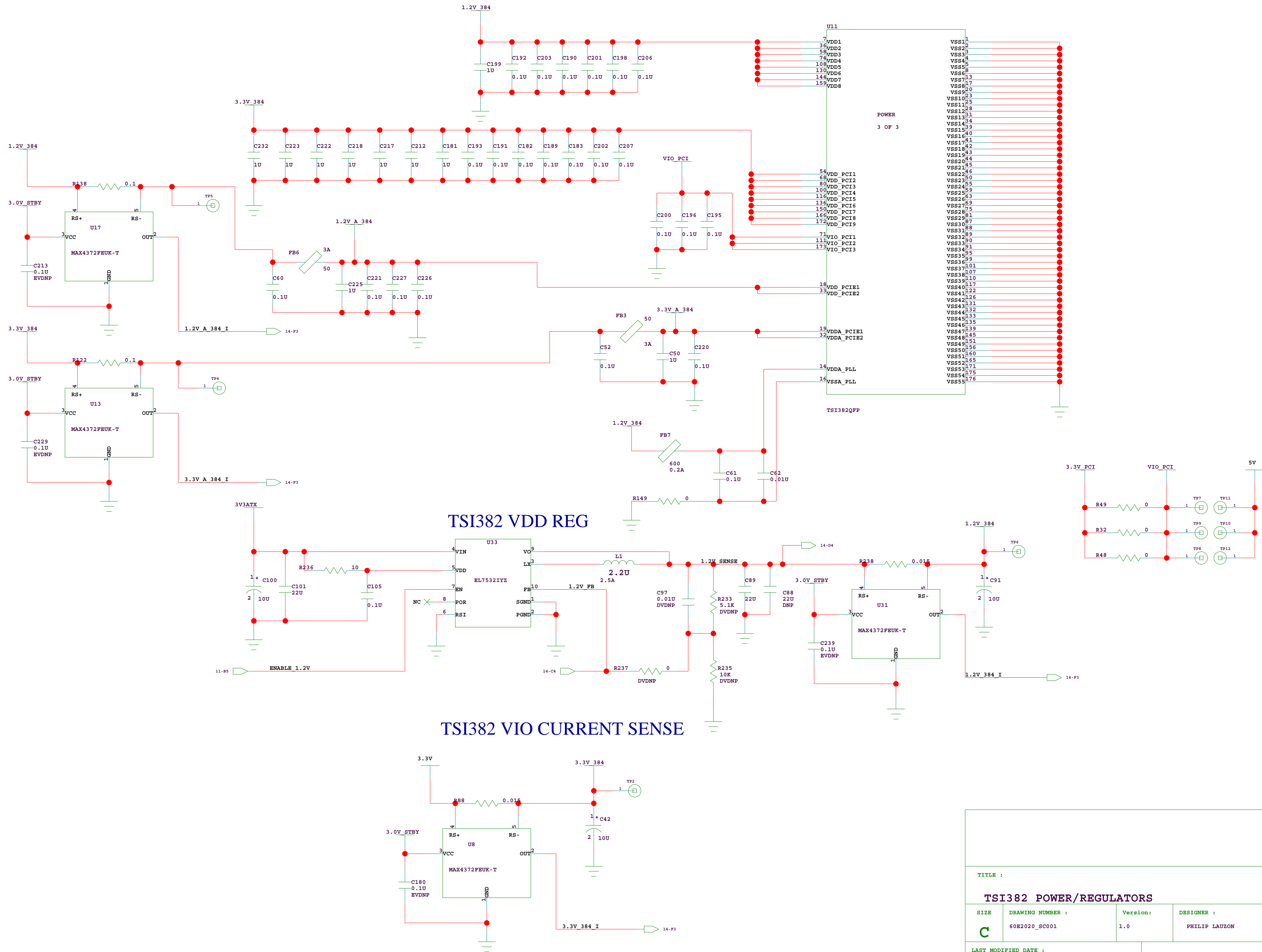


## POWER STATUS



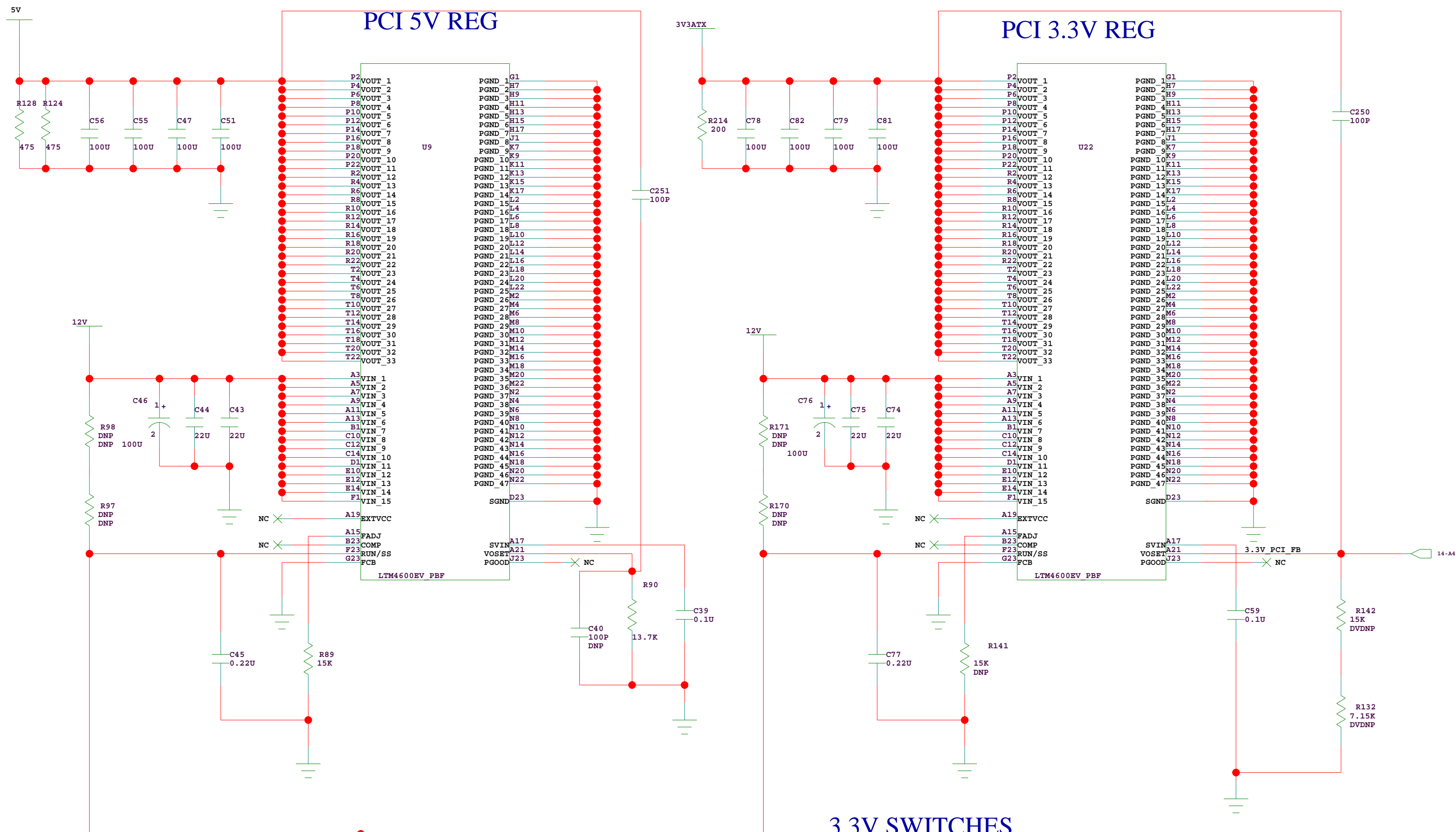
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# TSI382 POWER/REGULATORS

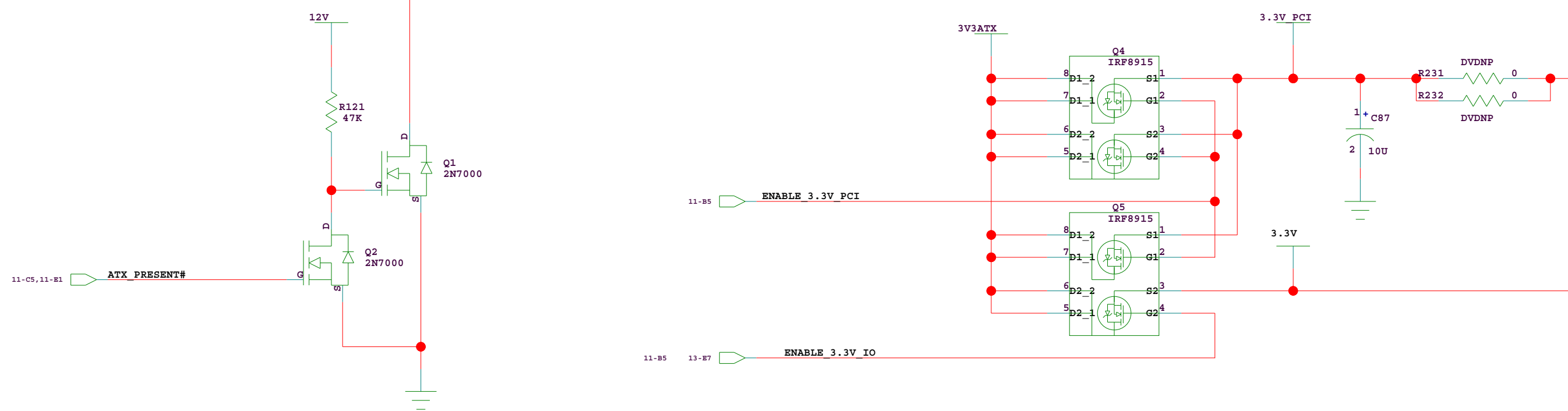


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# PCI POWER REGULATORS



## 3.3V SWITCHES



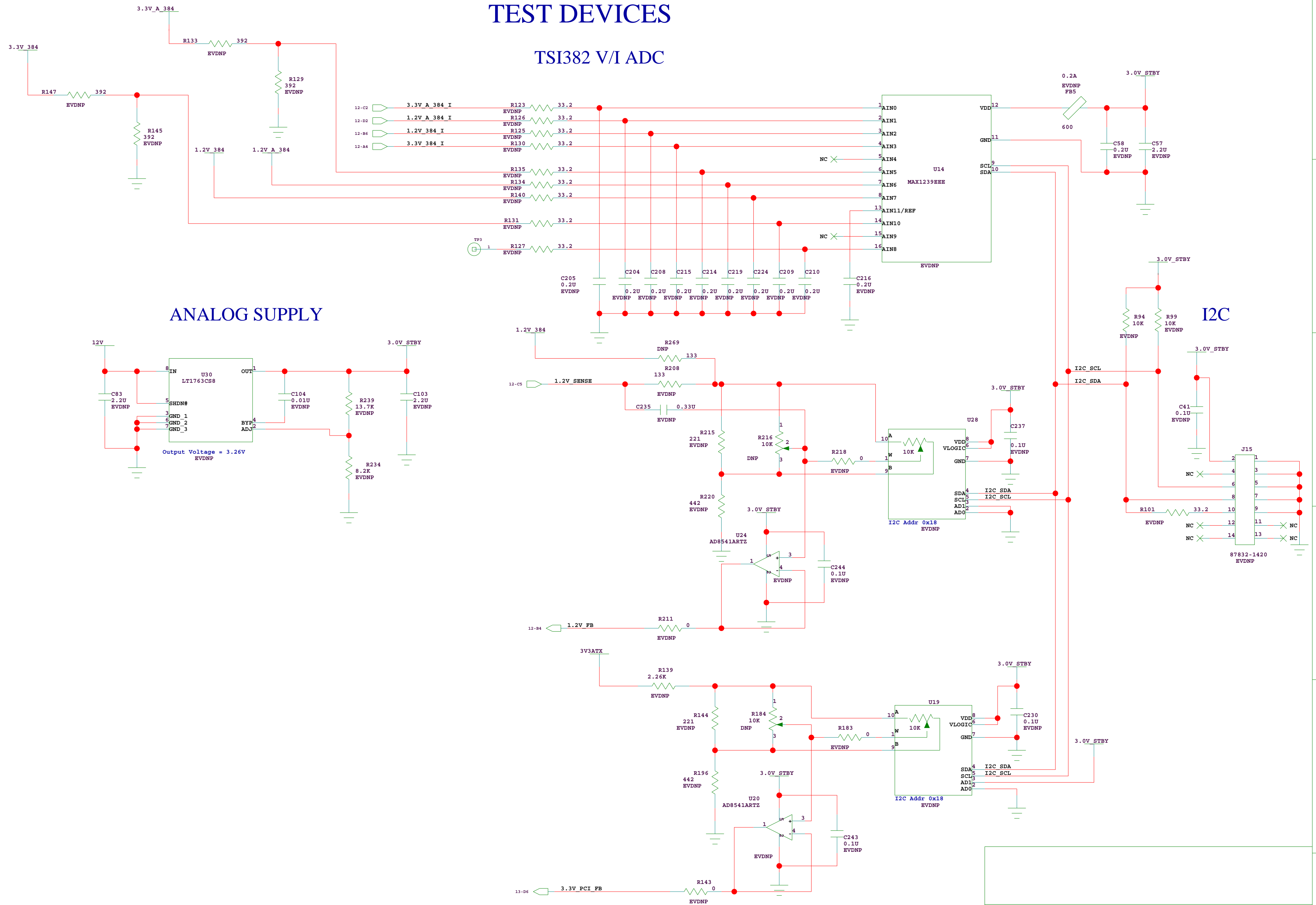
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# TEST DEVICES

## TSI382 V/I ADC

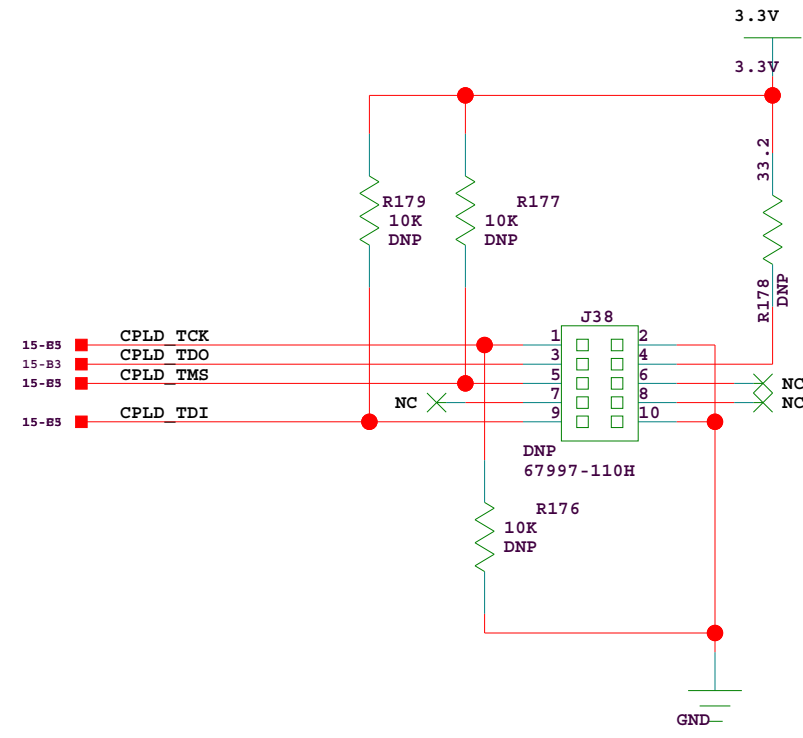
### ANALOG SUPPLY

### I2C

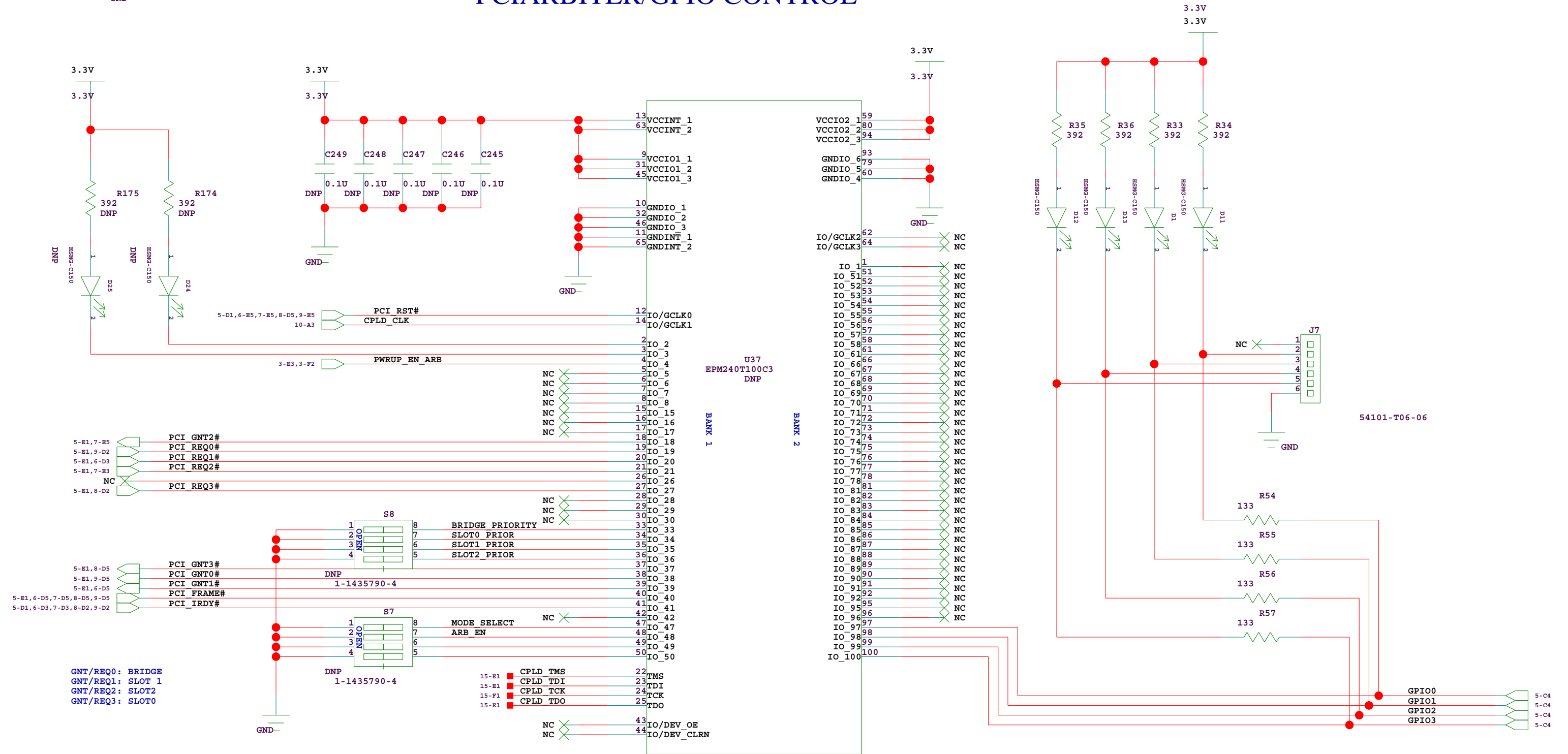


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<b>TEST DEVICES</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2020_SC001	1.0	PHILIP LAUZON
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# TEST DEVICES CONT'D



## PCIARBITER/GPIO CONTROL



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TEST DEVICES CONT'D			
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