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Title Page

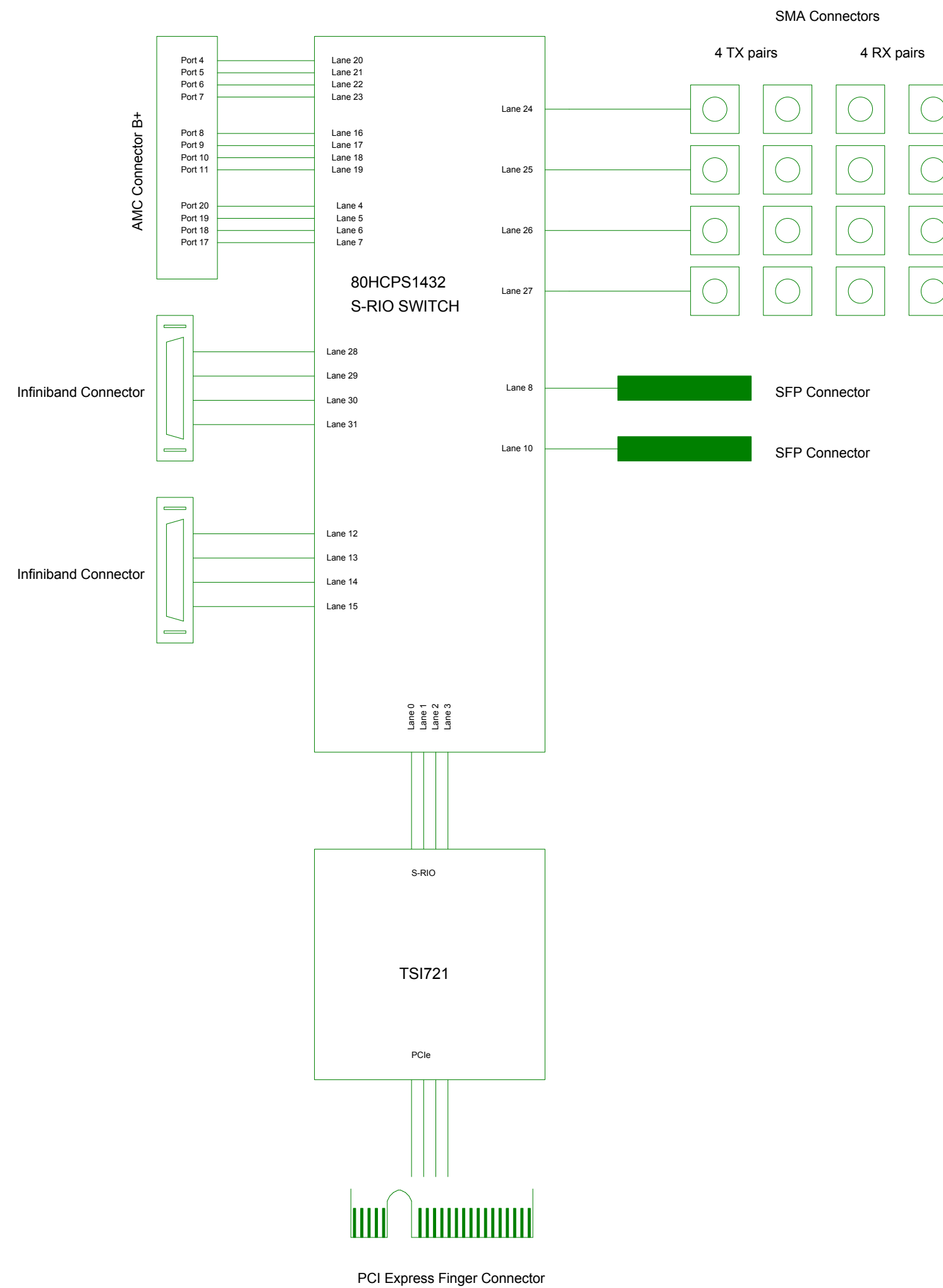
PCIe2 to S-RIO2 Bridging + Switching Evaluation Platform

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Block Diagram

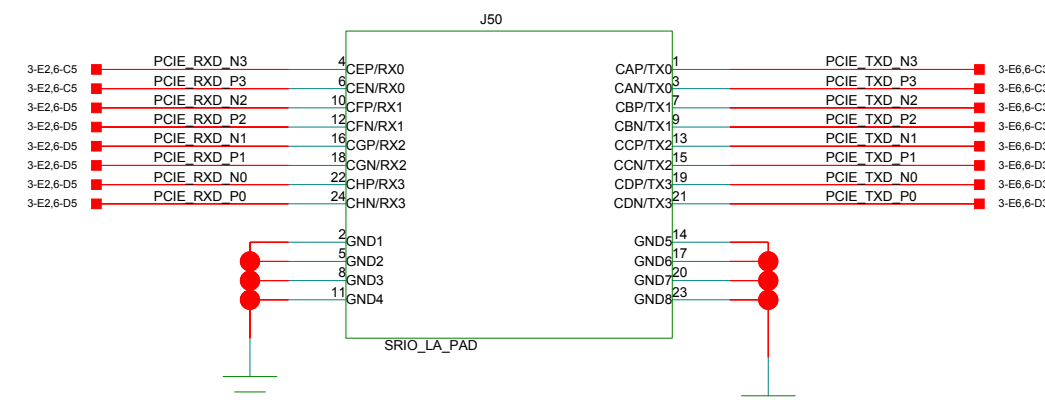
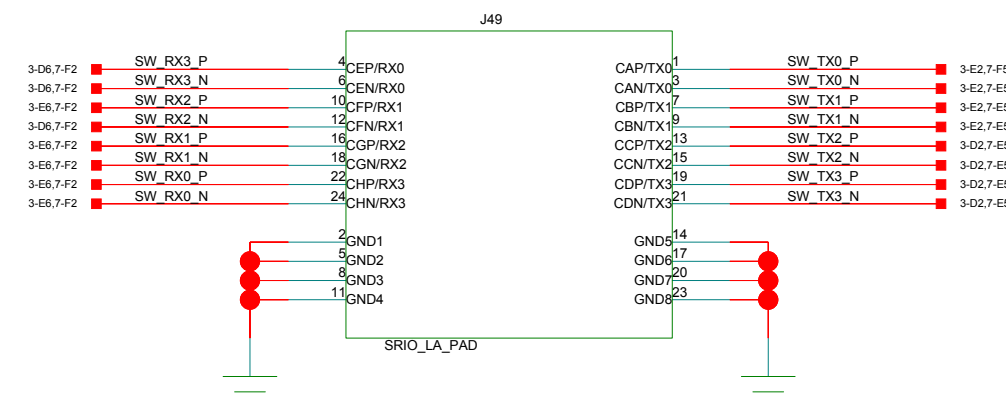
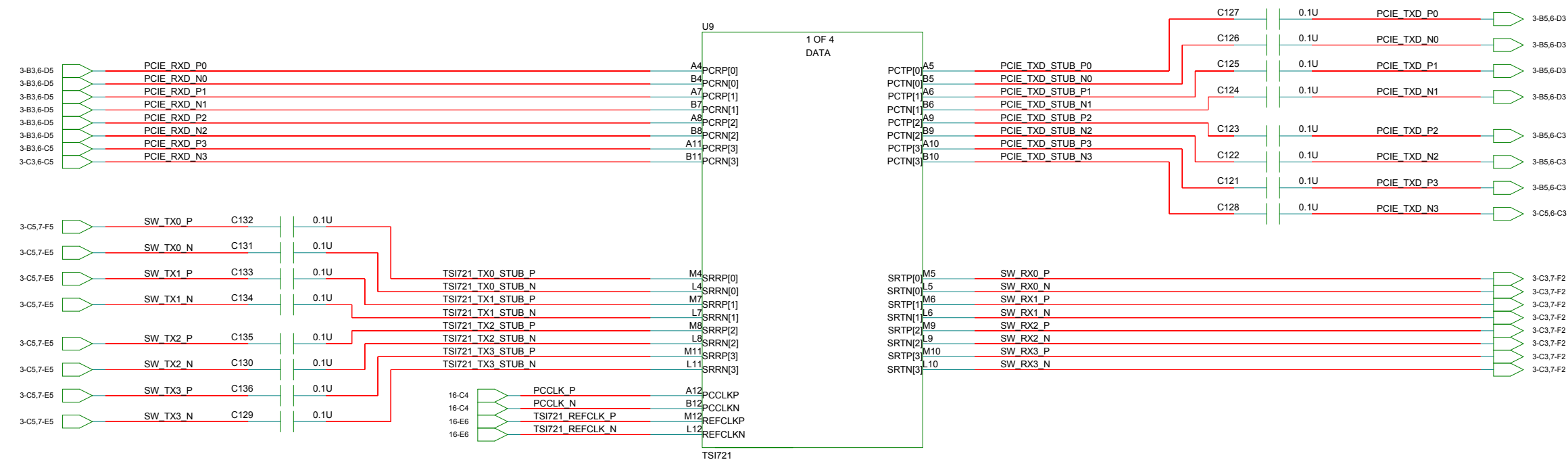


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Tsi721 Serial Links



TITLE :

TSI721 SERIAL LINKS

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DRAWING NUMBER :

Version:

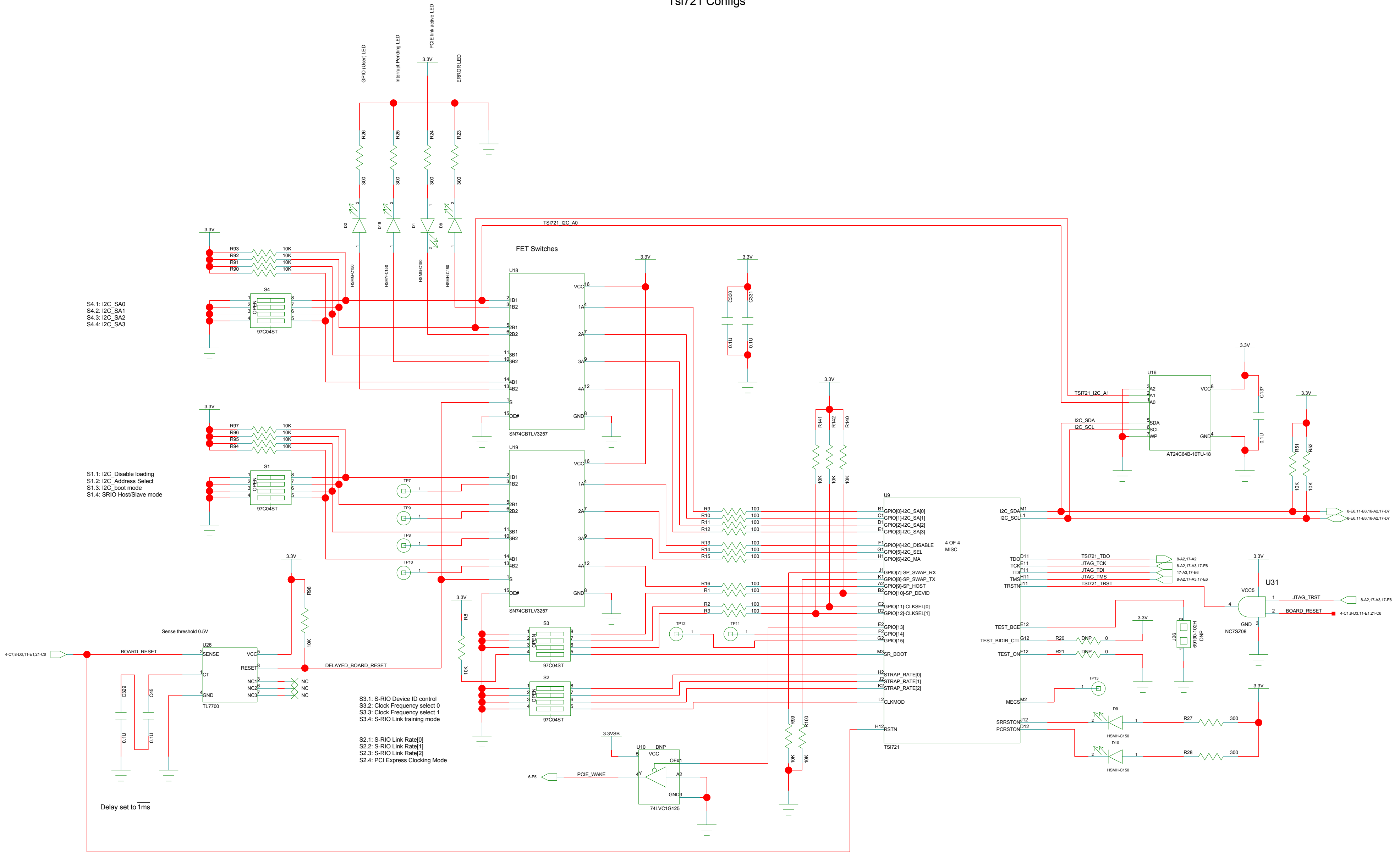
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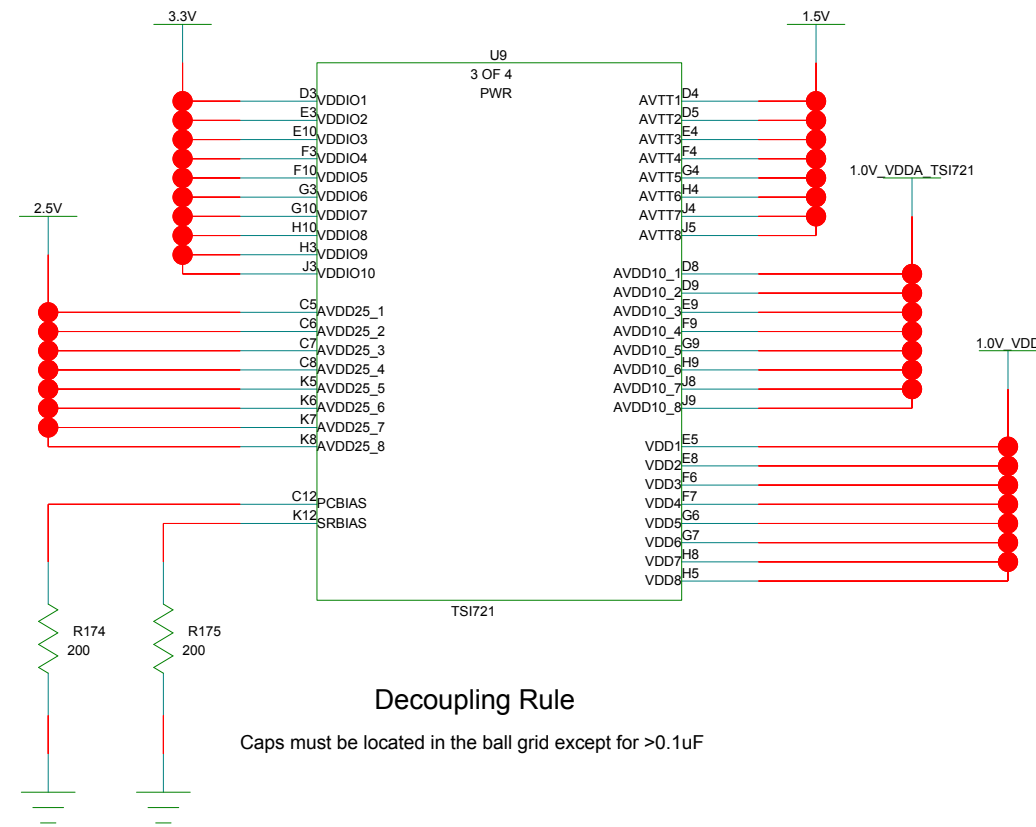
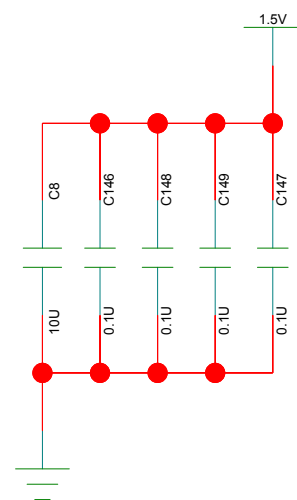
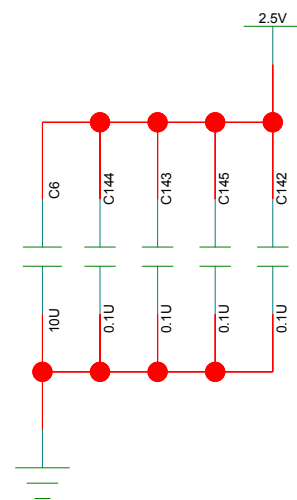
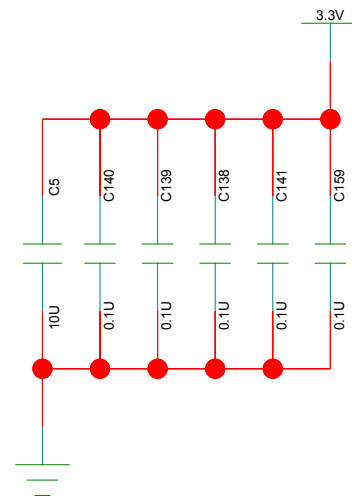
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Tsi721 Configs



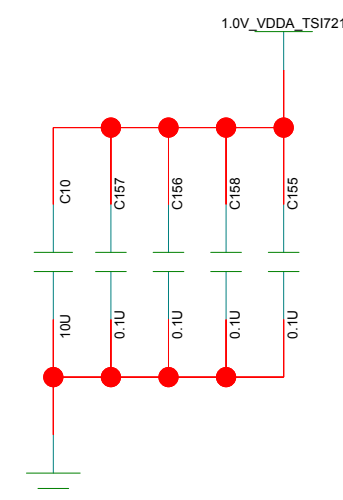
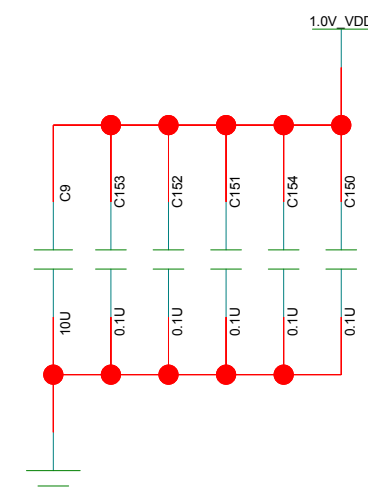
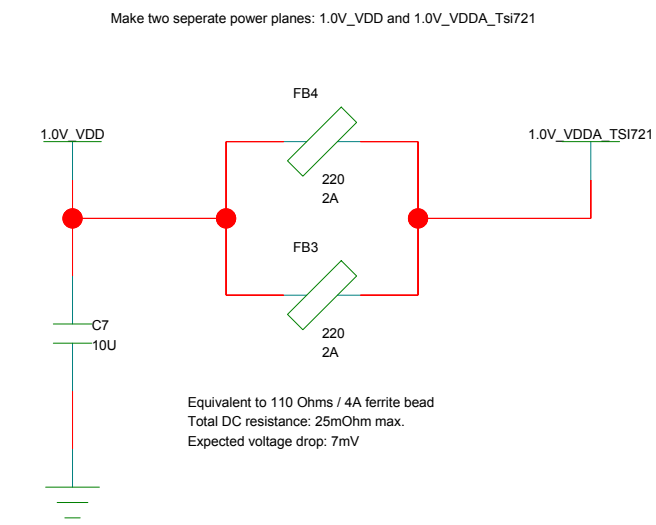
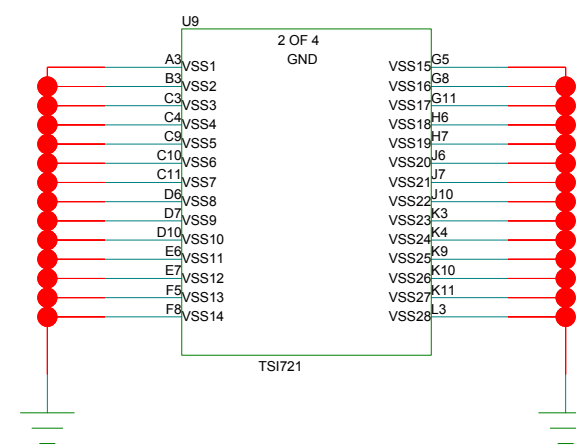
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SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 18-06-2012_10:12		SHEET 4 OF 21	

Tsi721 Power



Decoupling Rule

Caps must be located in the ball grid except for $>0.1\mu\text{F}$



TITLE :

TSI721 POWER

SIZE

DRAWING NUMBER :

Version:

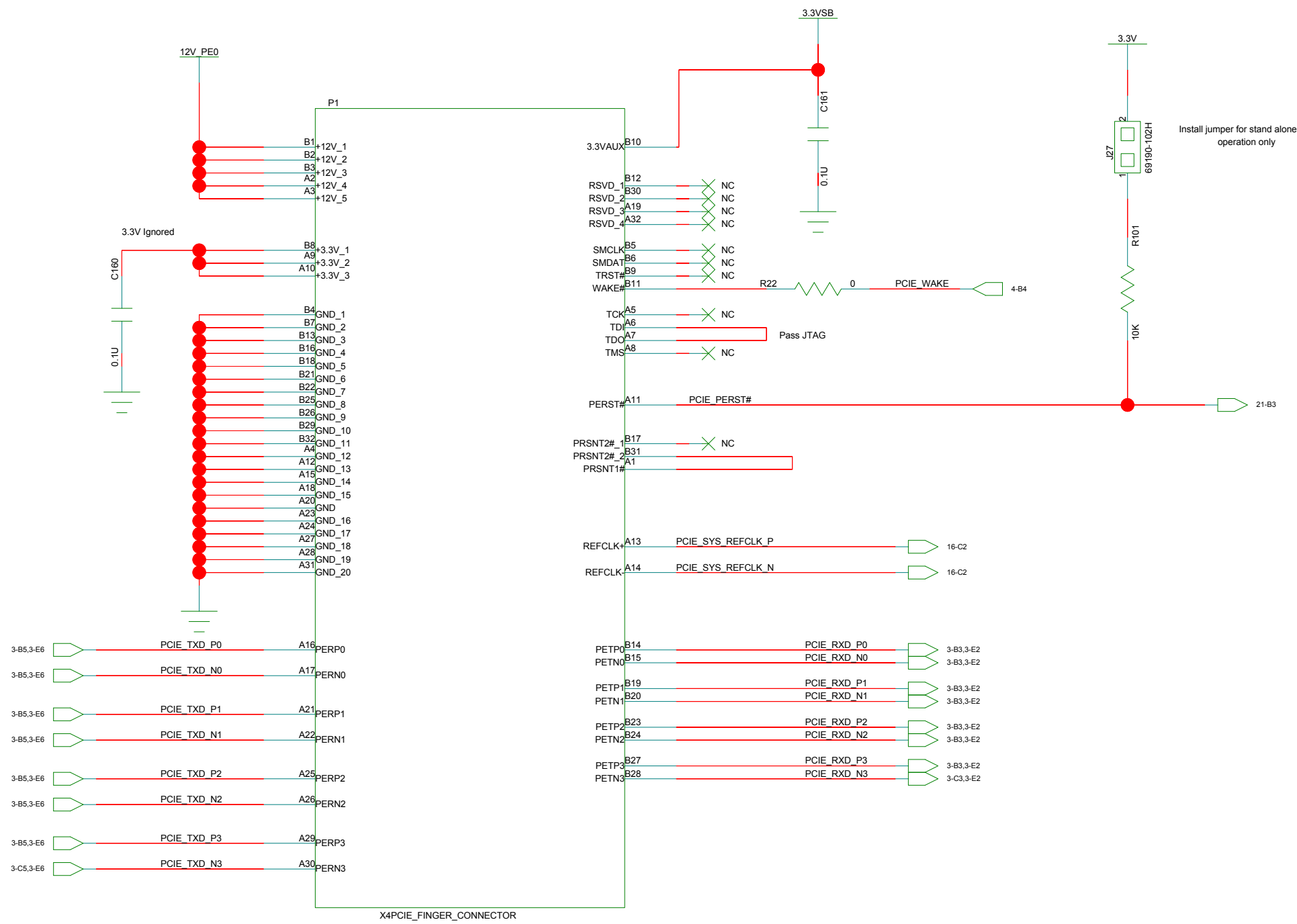
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LAST MODIFIED DATE :

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PCI Express Connector



TITLE : PCI EXPRESS CONNECTOR			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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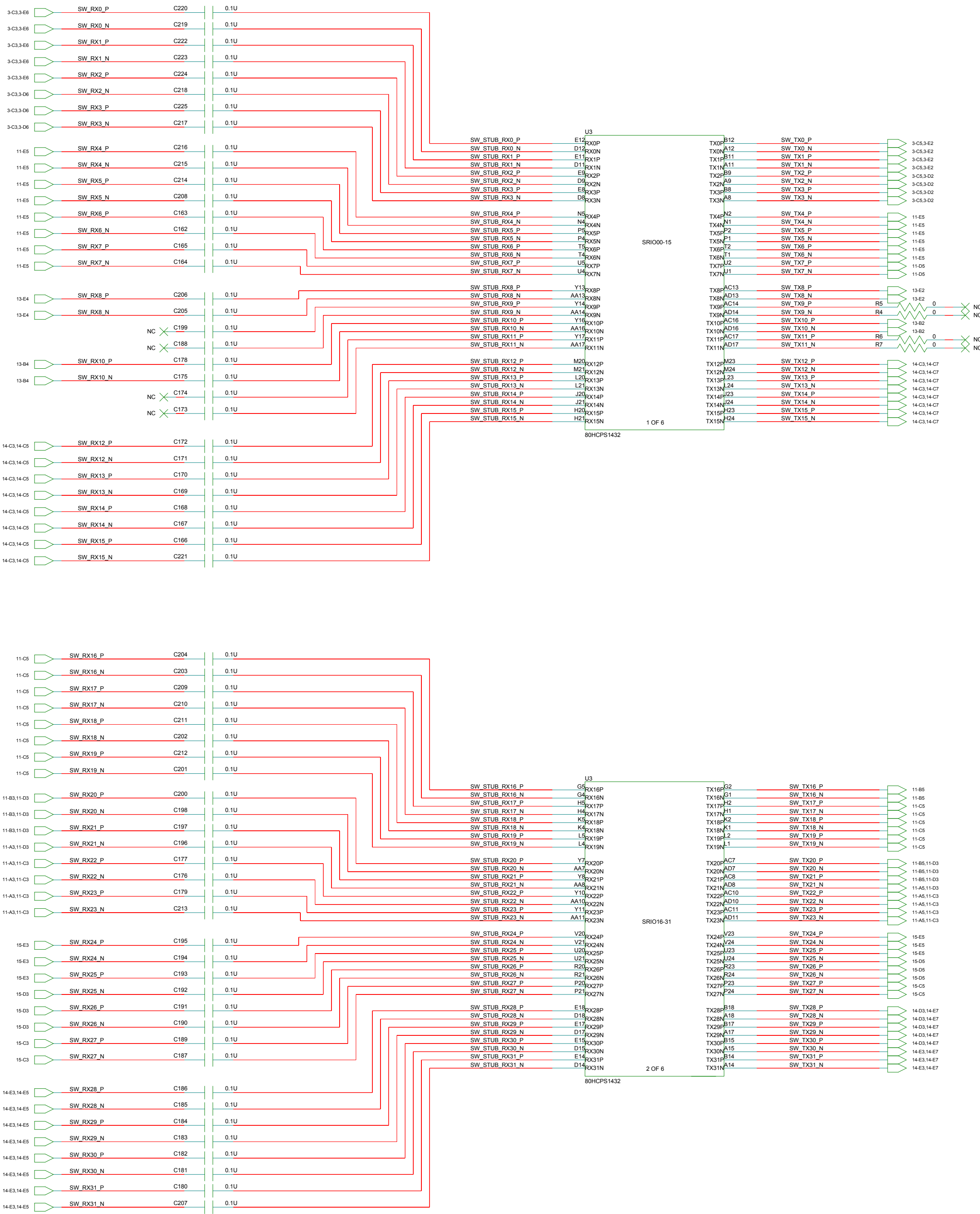
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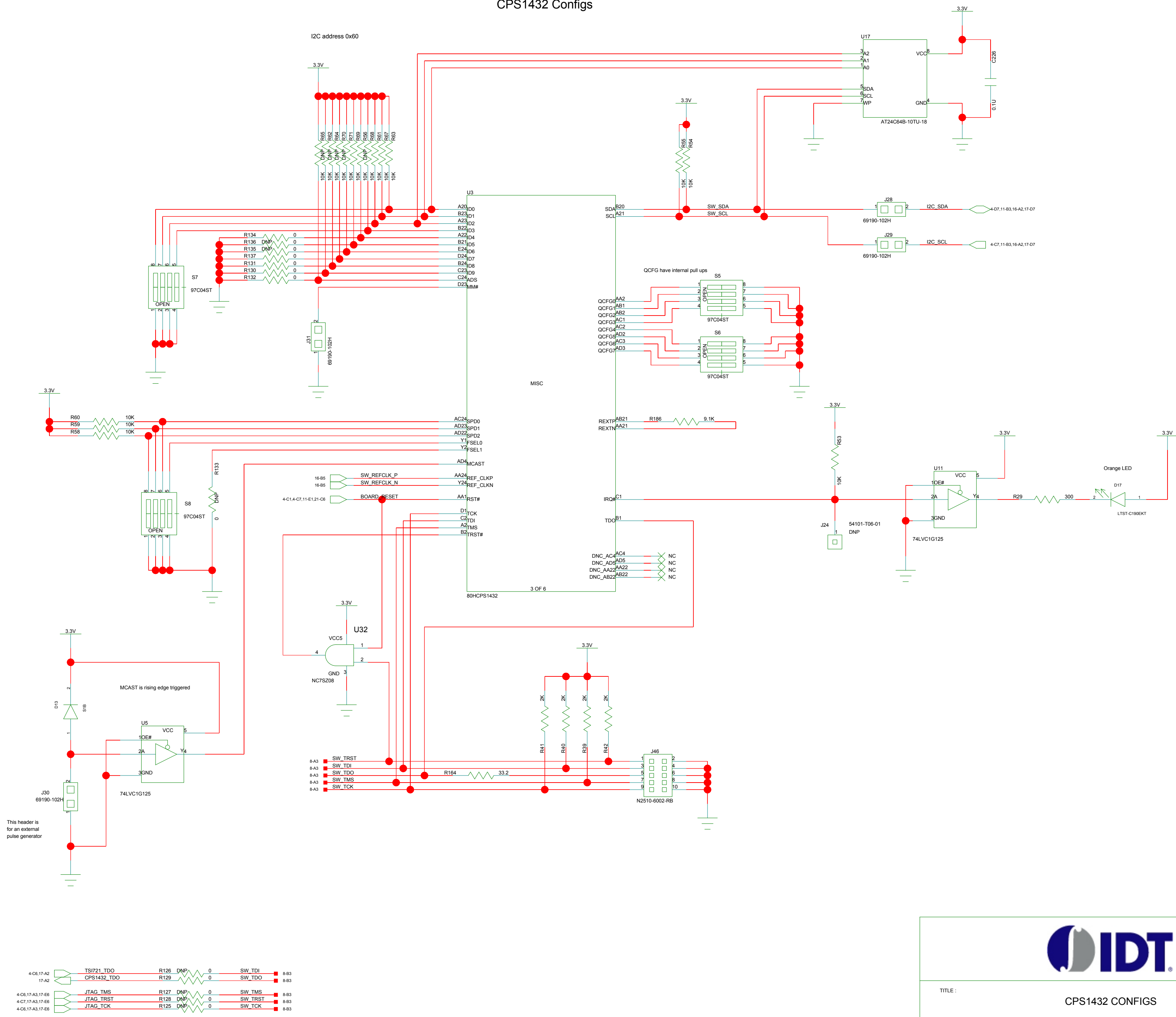
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CPS1432 Serial Links



TITLE : CPS1432 SERIAL LINKS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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CPS1432 Configs



TITLE : CPS1432 CONFIGS			
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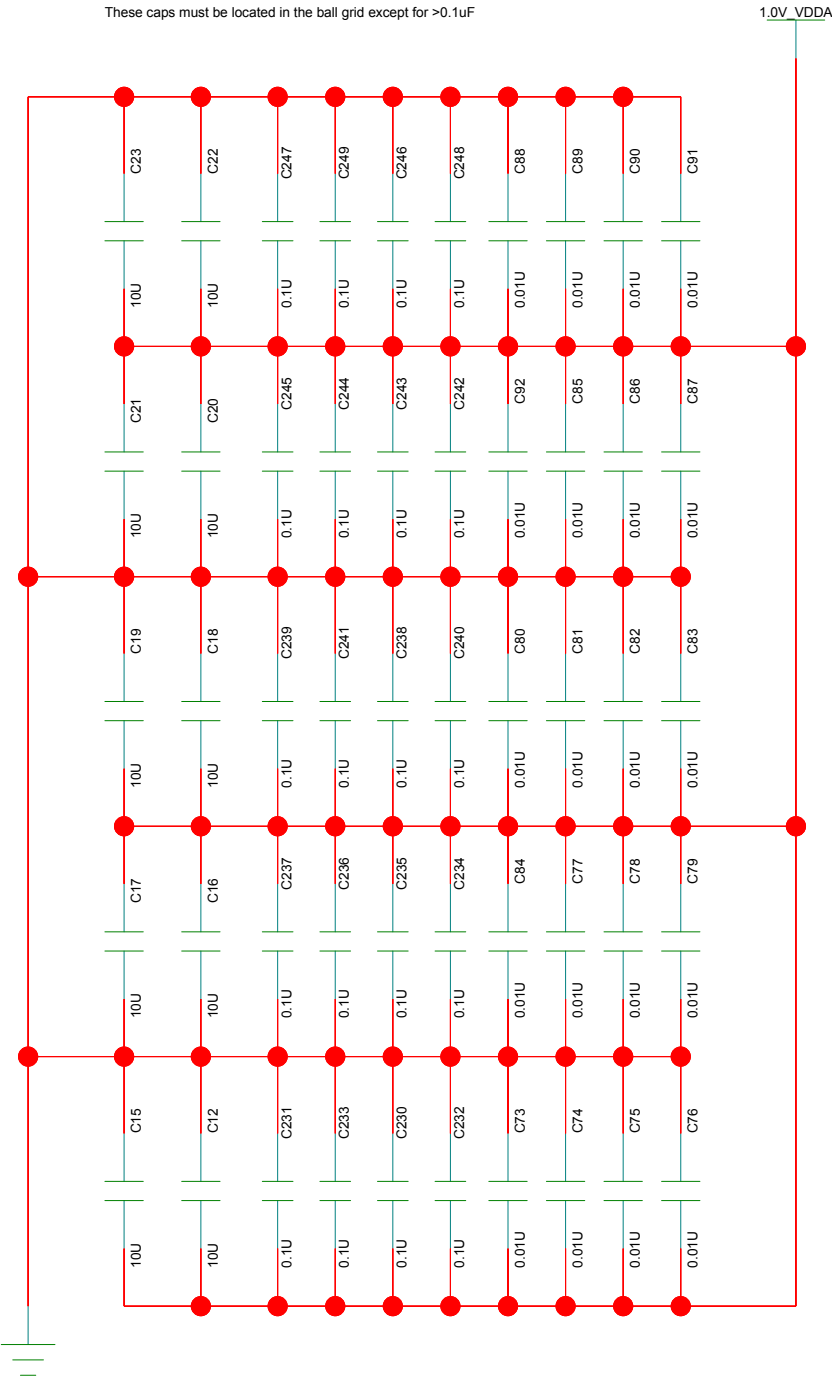
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CPS1432 Power

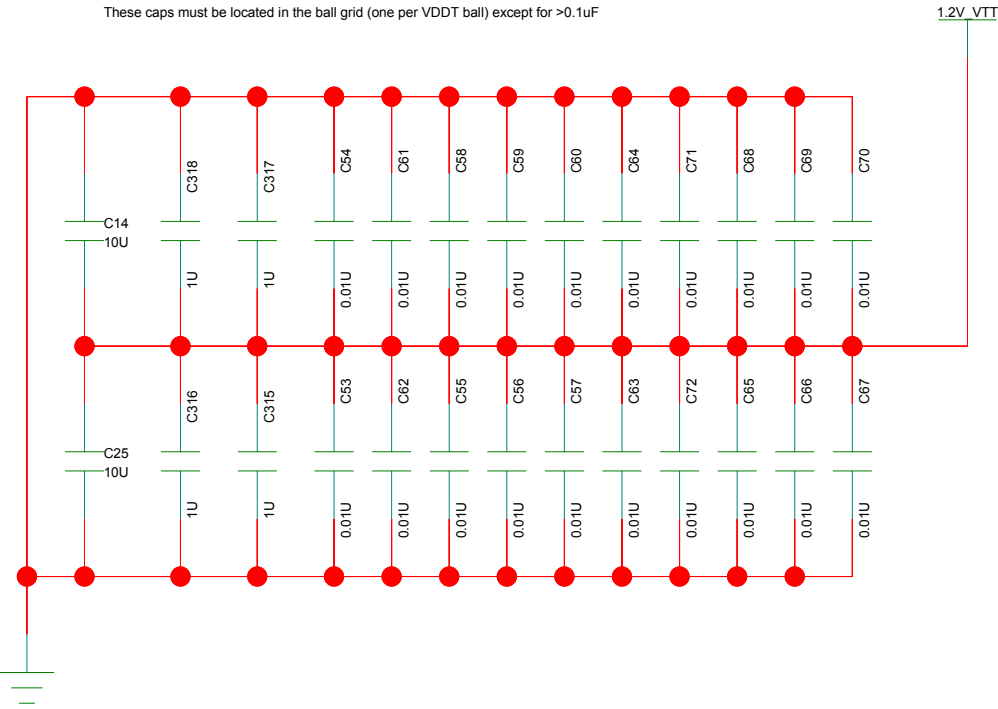
Decoupling 1.0V_VDDA

These caps must be located in the ball grid except for >0.1uF



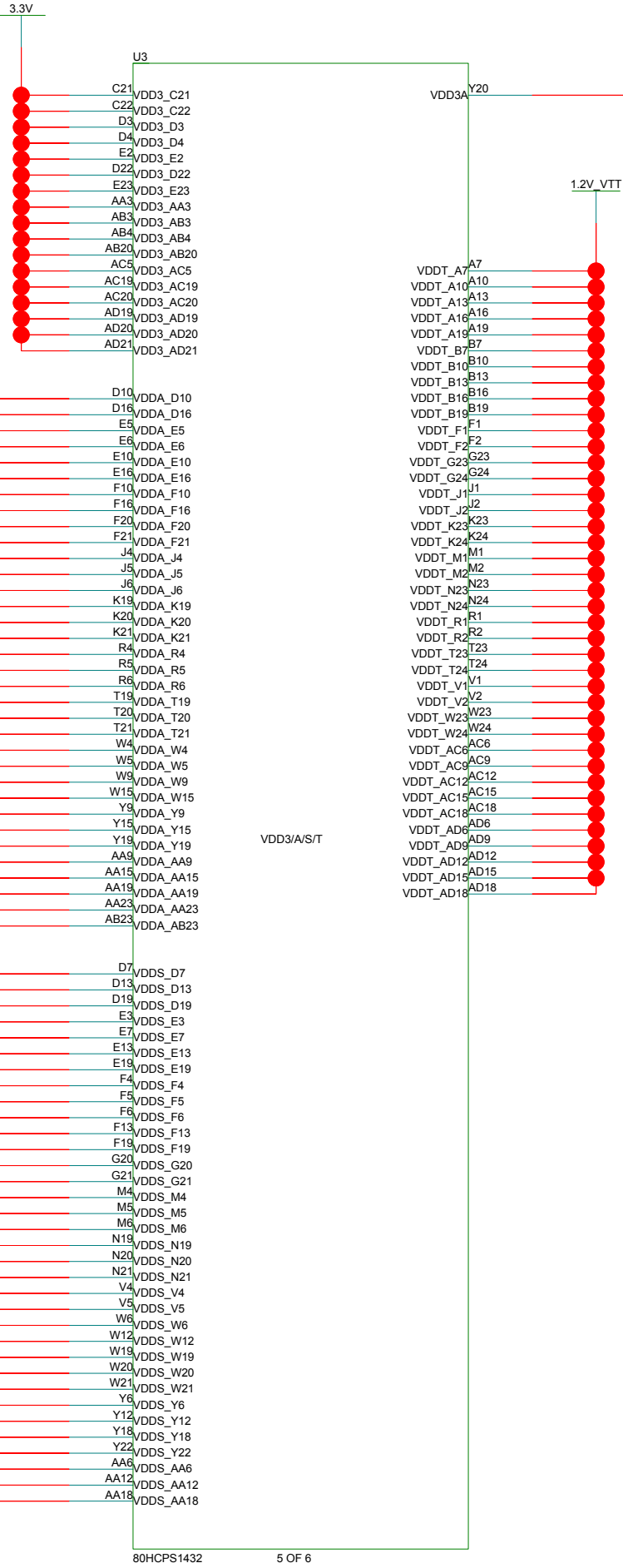
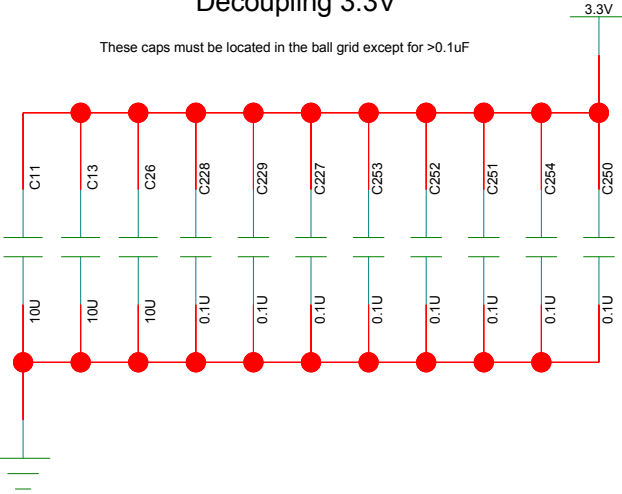
Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



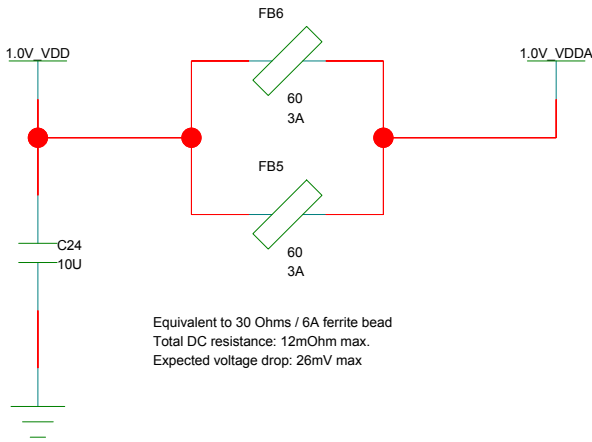
Decoupling 3.3V

These caps must be located in the ball grid except for >0.1uF



Board layout note:

Make two separate power planes: 1.0V_VDD and 1.0V_VDDA



Equivalent to 30 Ohms / 6A ferrite bead
Total DC resistance: 12mOhm max.
Expected voltage drop: 26mV max.



TITLE :

CPS1432 POWER

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Version:

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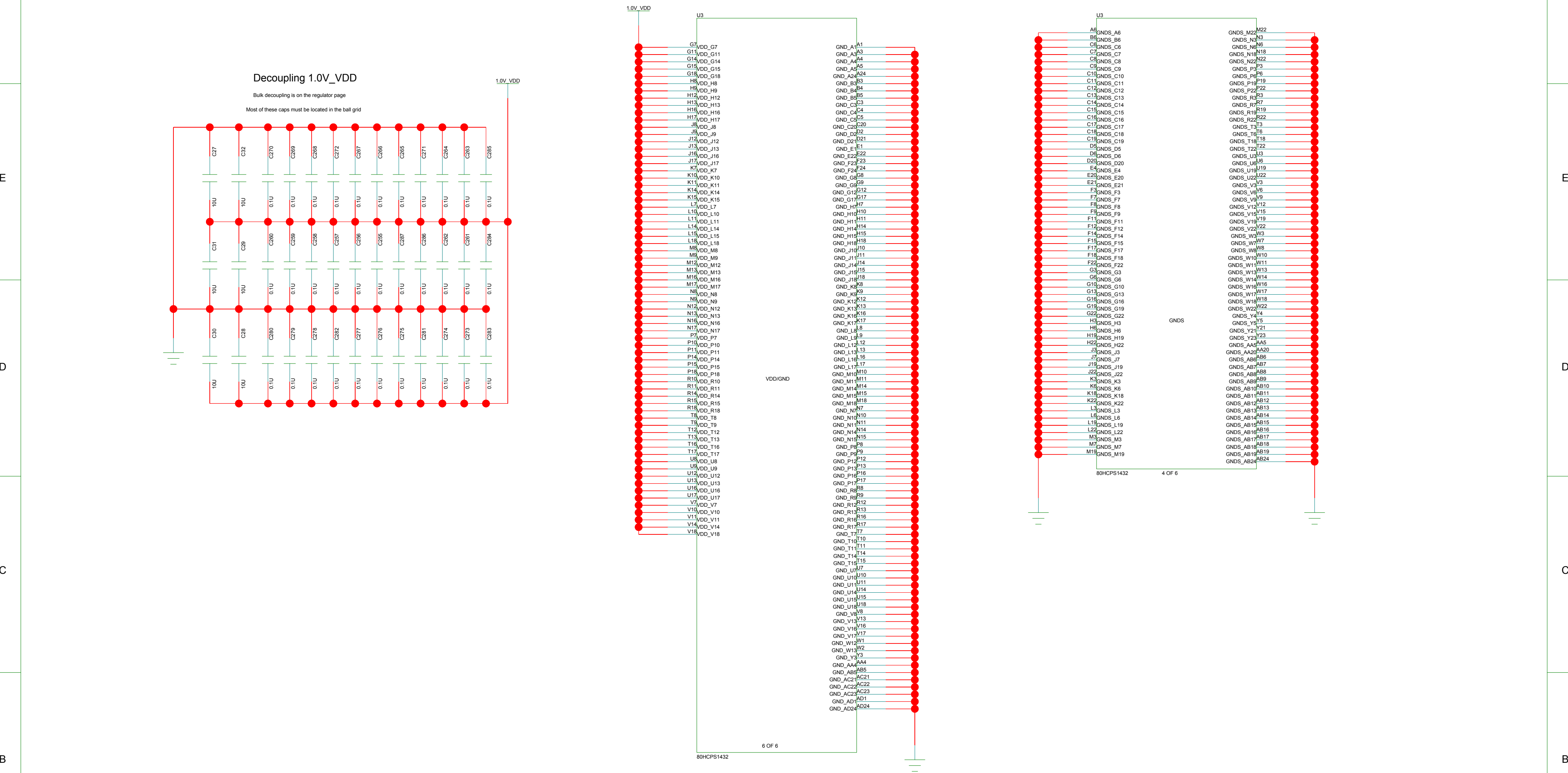
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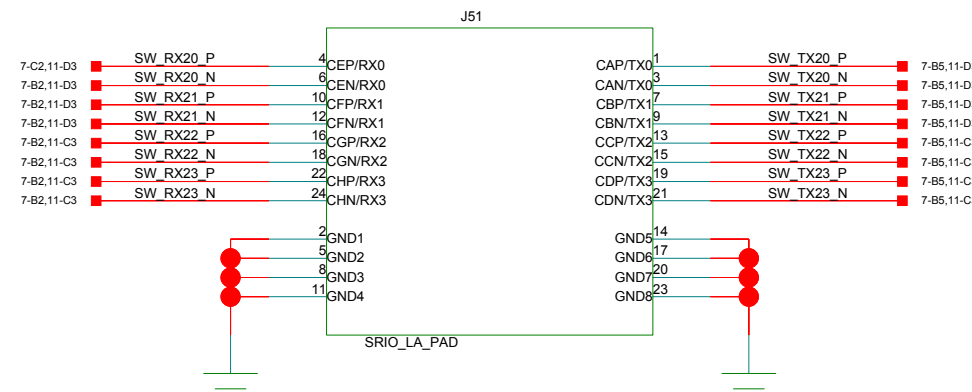
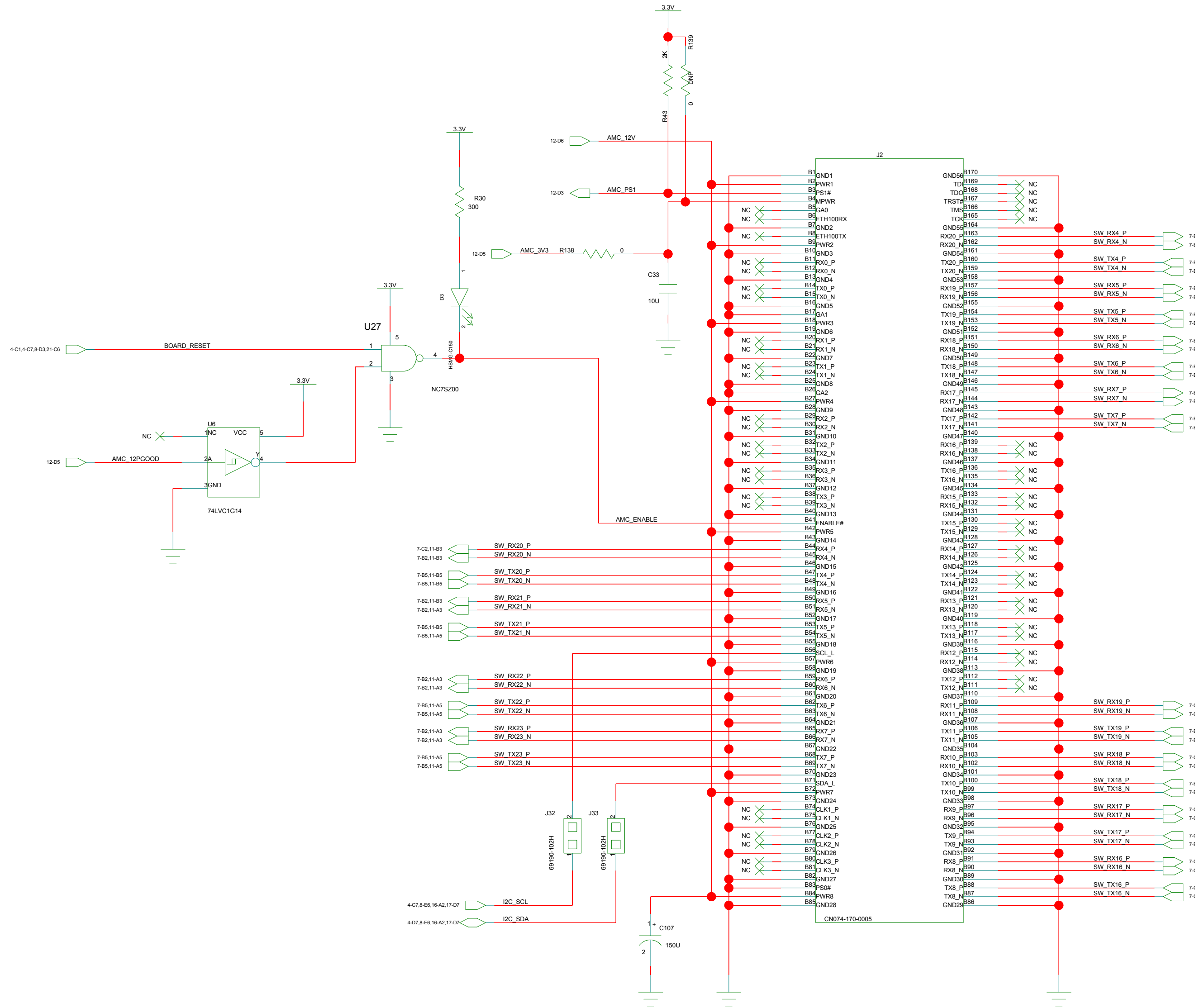
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CPS1432 Core Power & Ground



TITLE : CPS1432 CORE POWER & GROUND			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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AMC Connector



TITLE :

AMC CONNECTOR

SIZE

DRAWING NUMBER :

Version:

DESIGNER :

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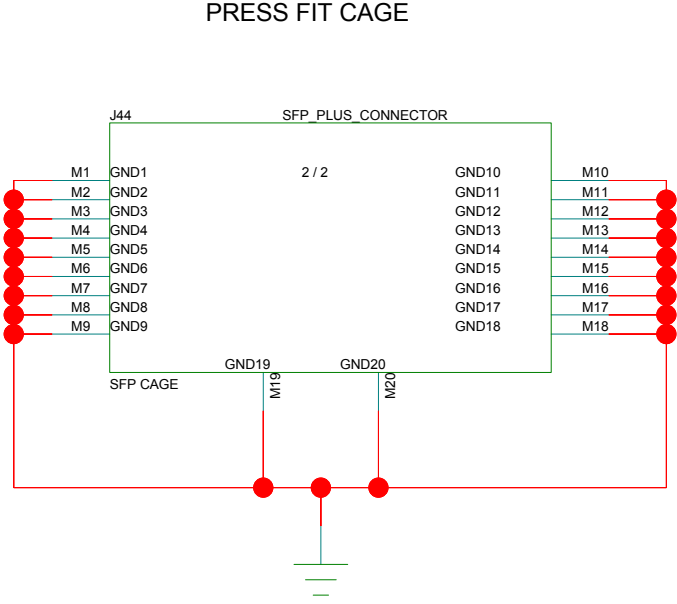
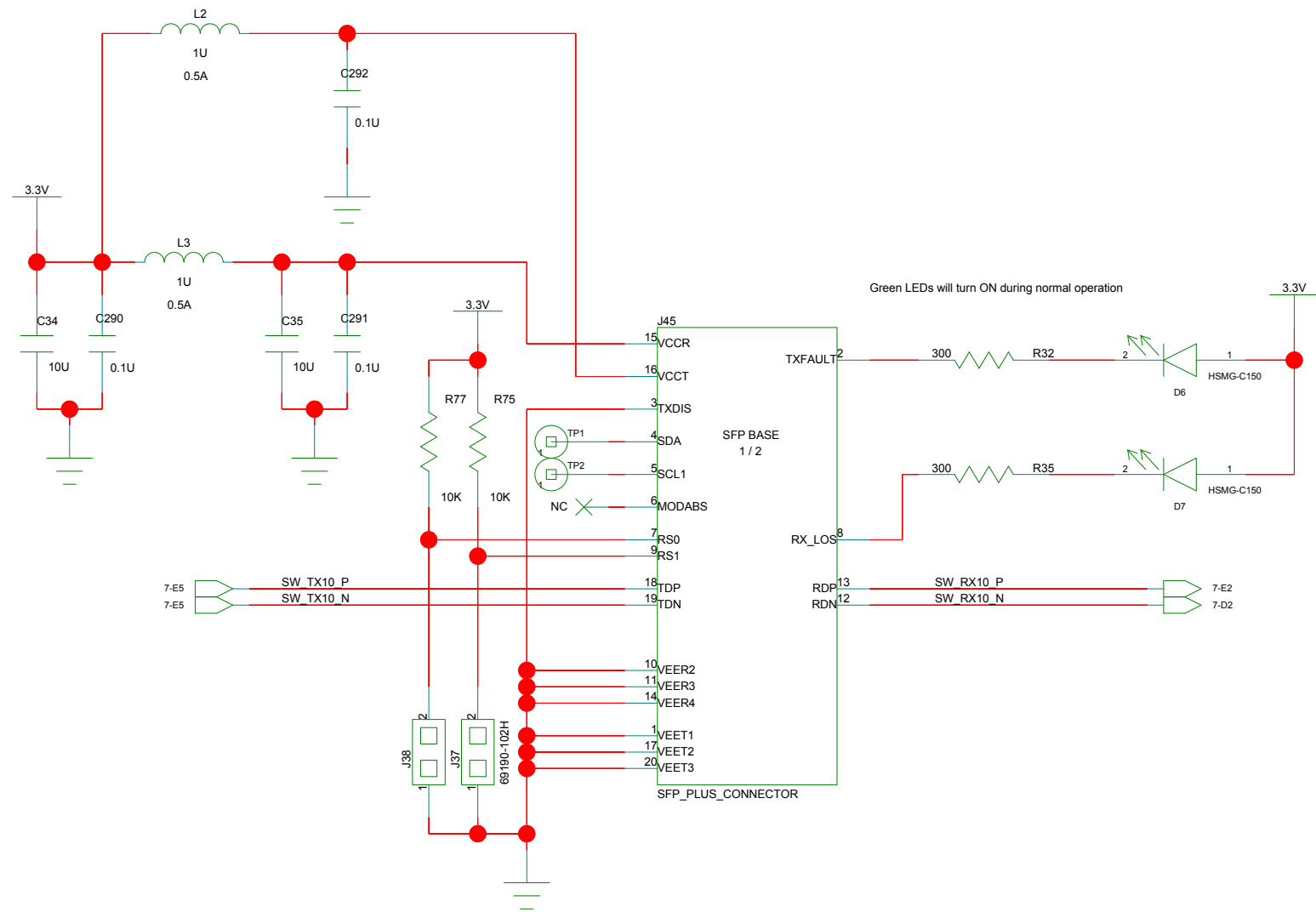
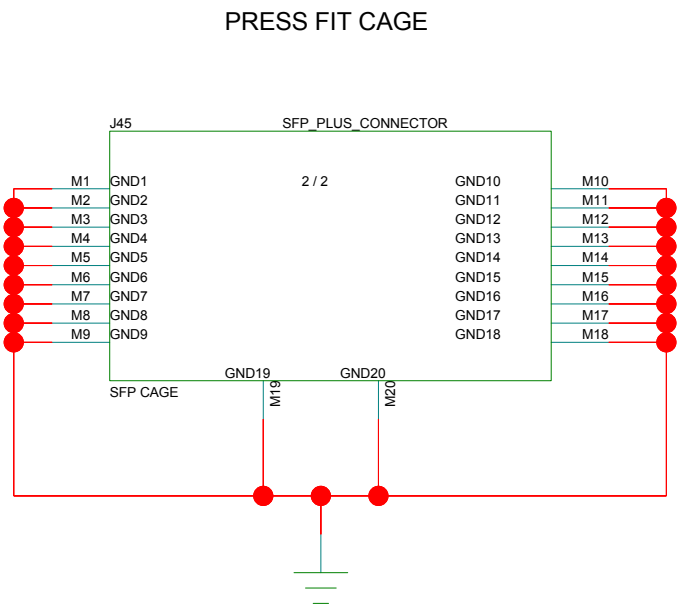
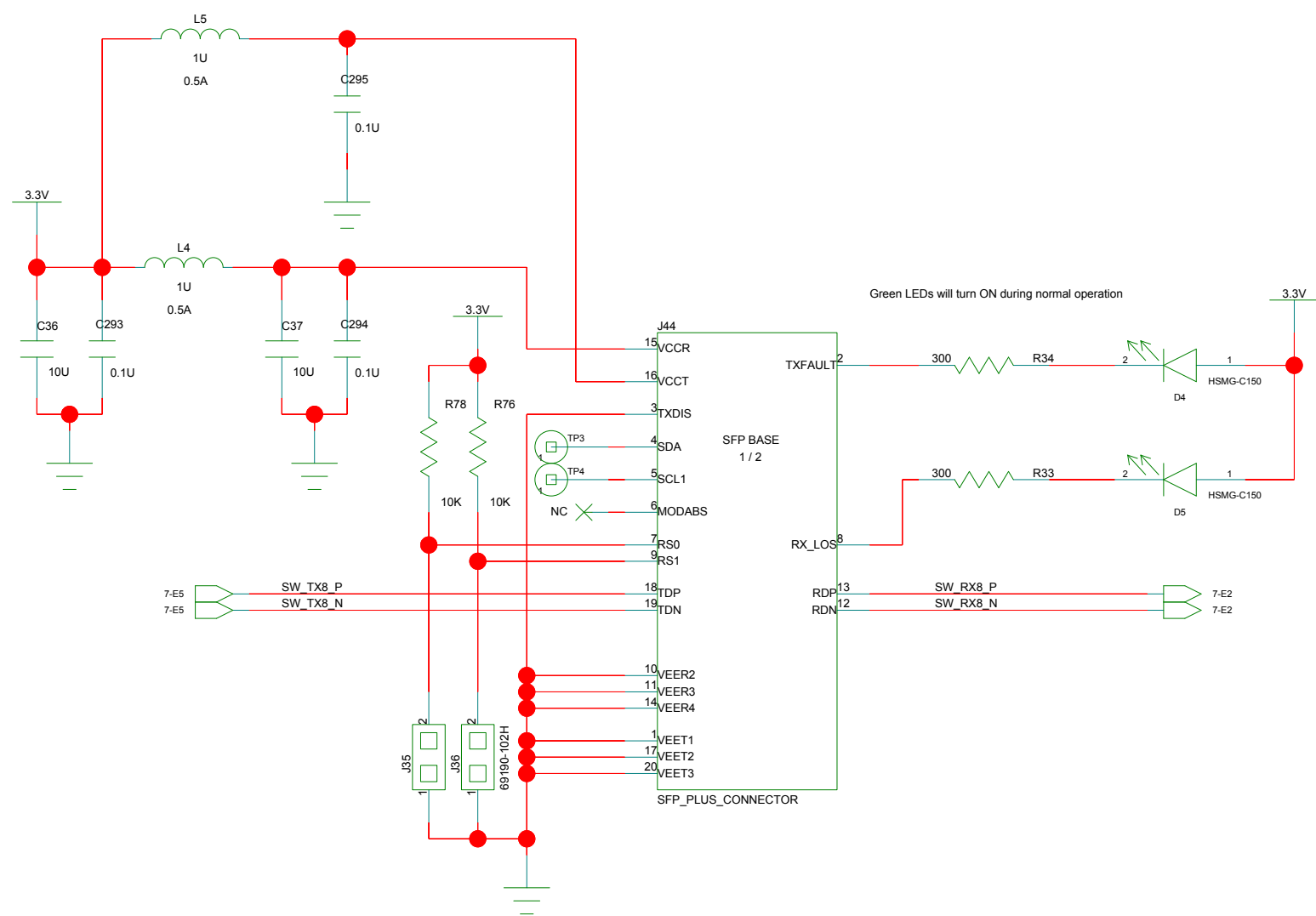
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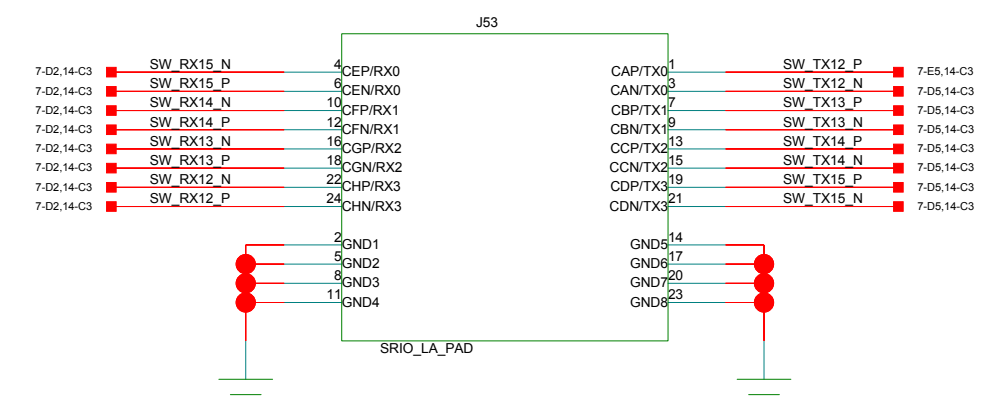
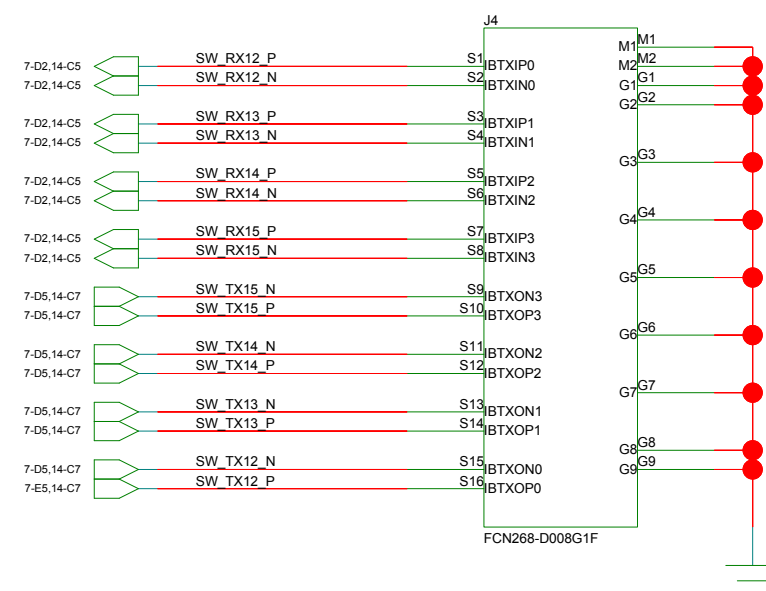
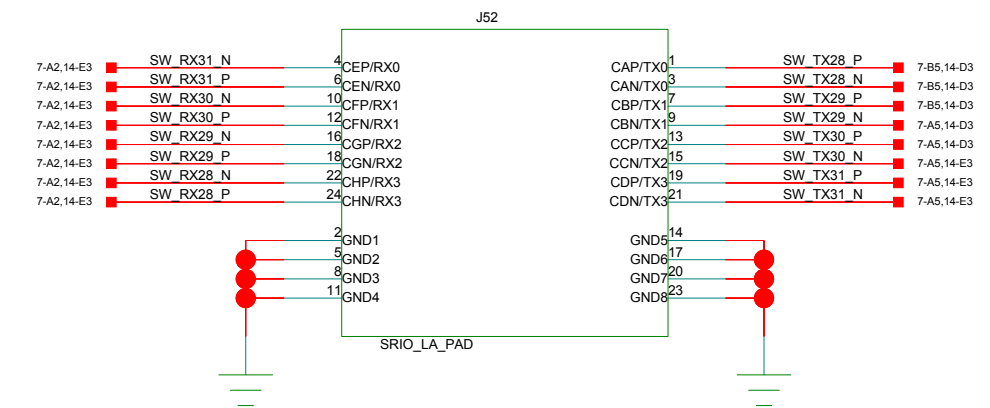
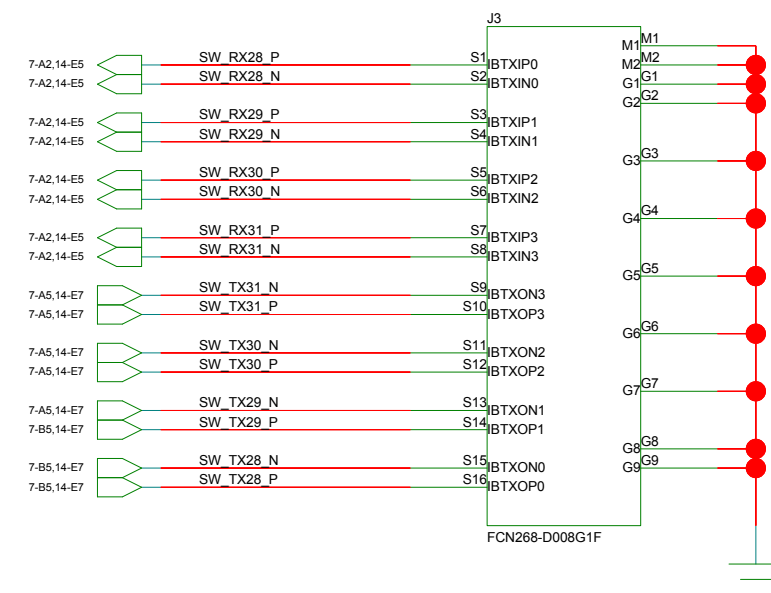
TITLE : AMC HOT PLUG / POWER CONTROLLER			
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LAST MODIFIED DATE : 07-09-2011_13:17		SHEET 12 OF 21	

SFP+ Connectors



TITLE :			
SFP+ CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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Infiniband Connectors

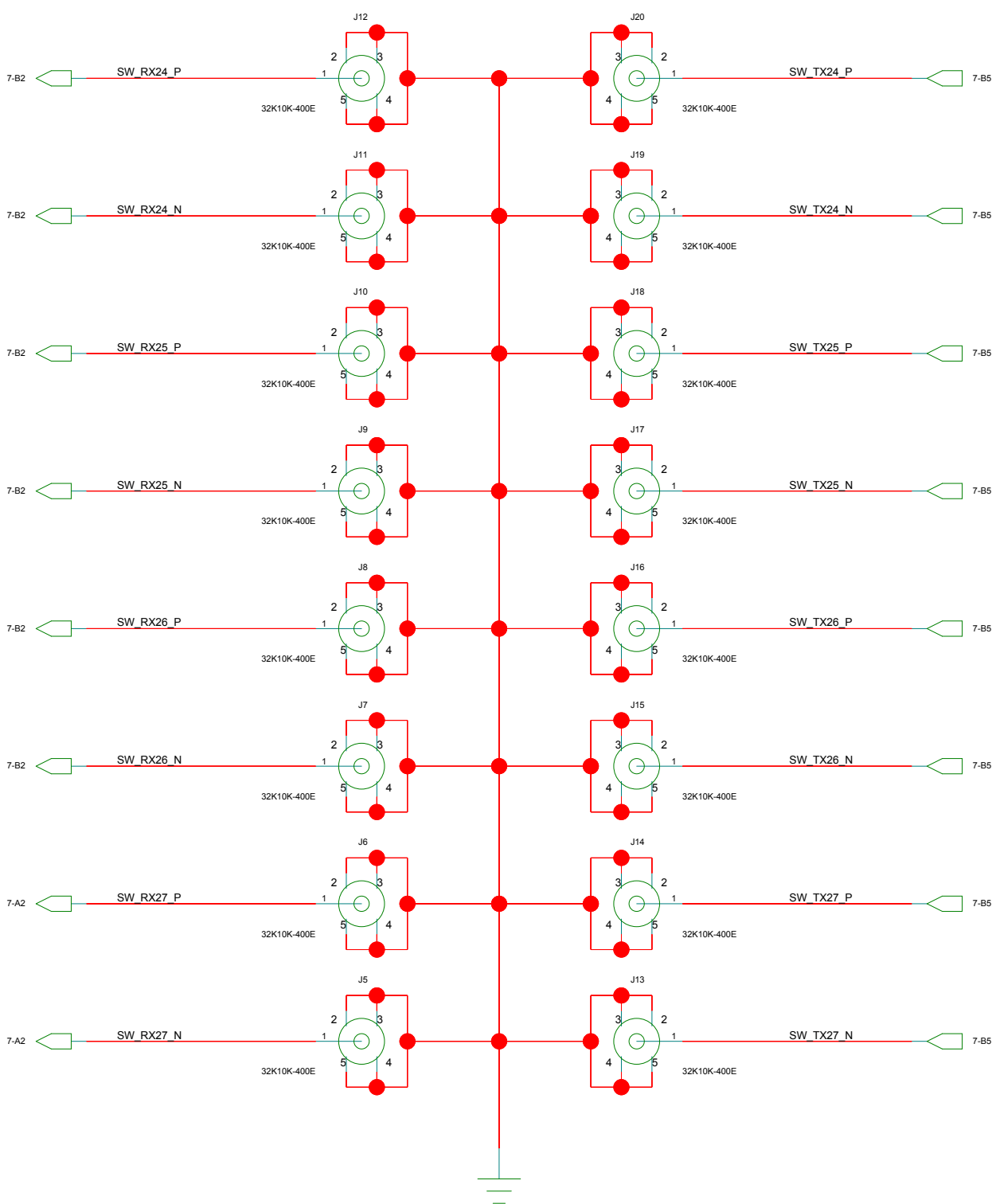


TITLE : INFINIBAND CONNECTORS

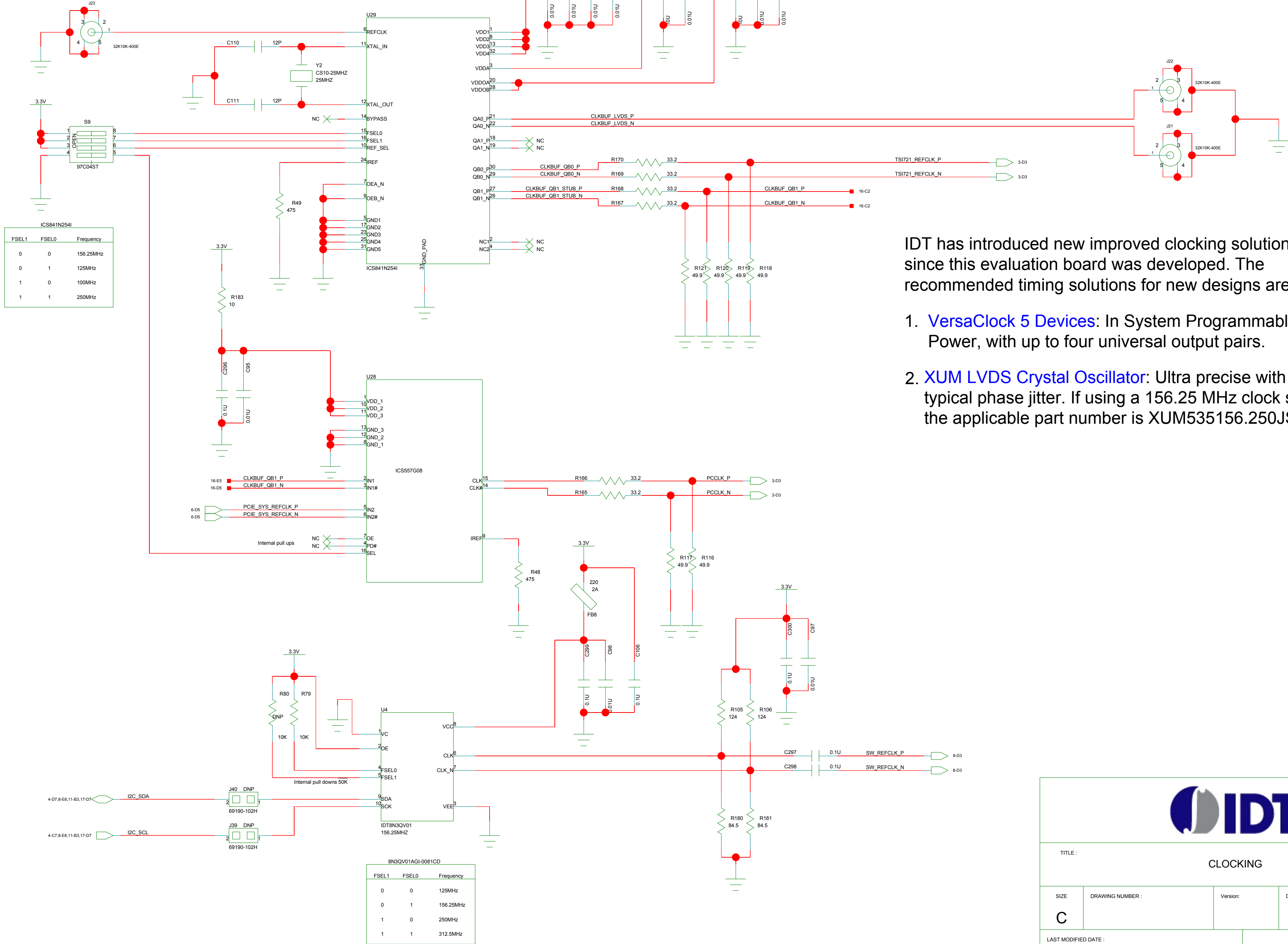
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SMA Connectors



TITLE : SMA CONNECTORS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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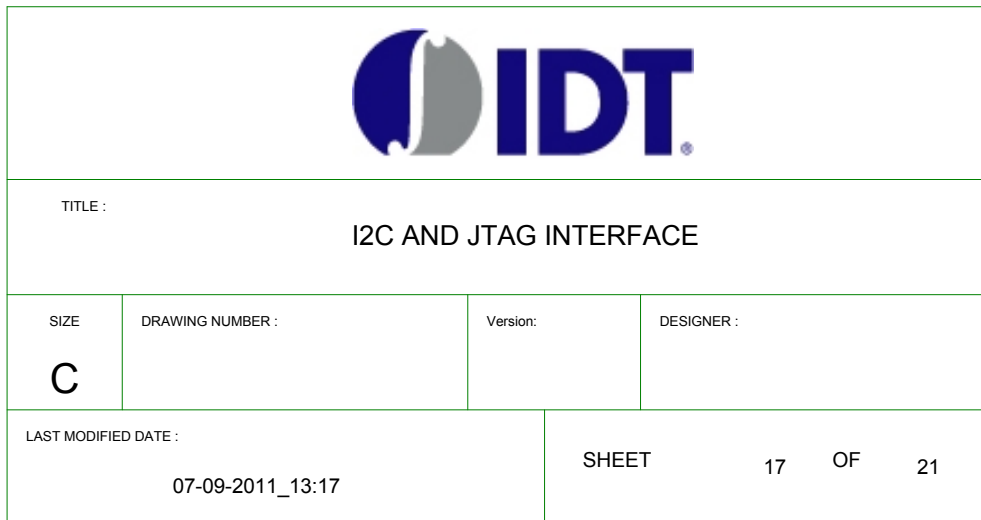
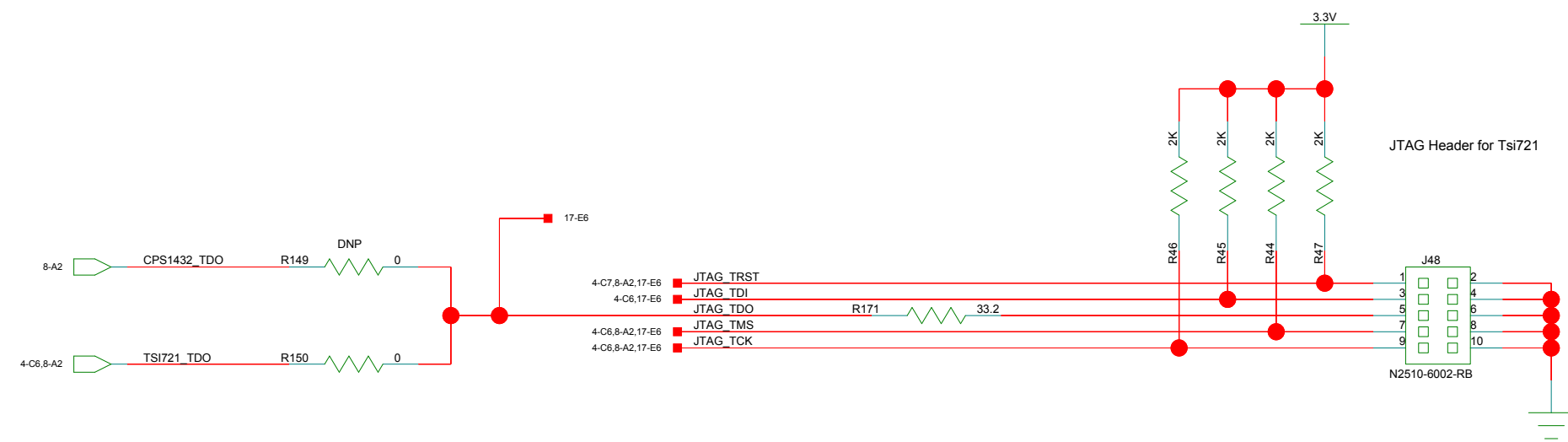


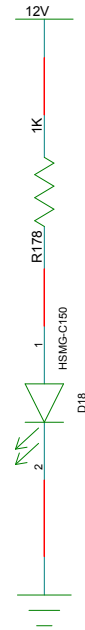
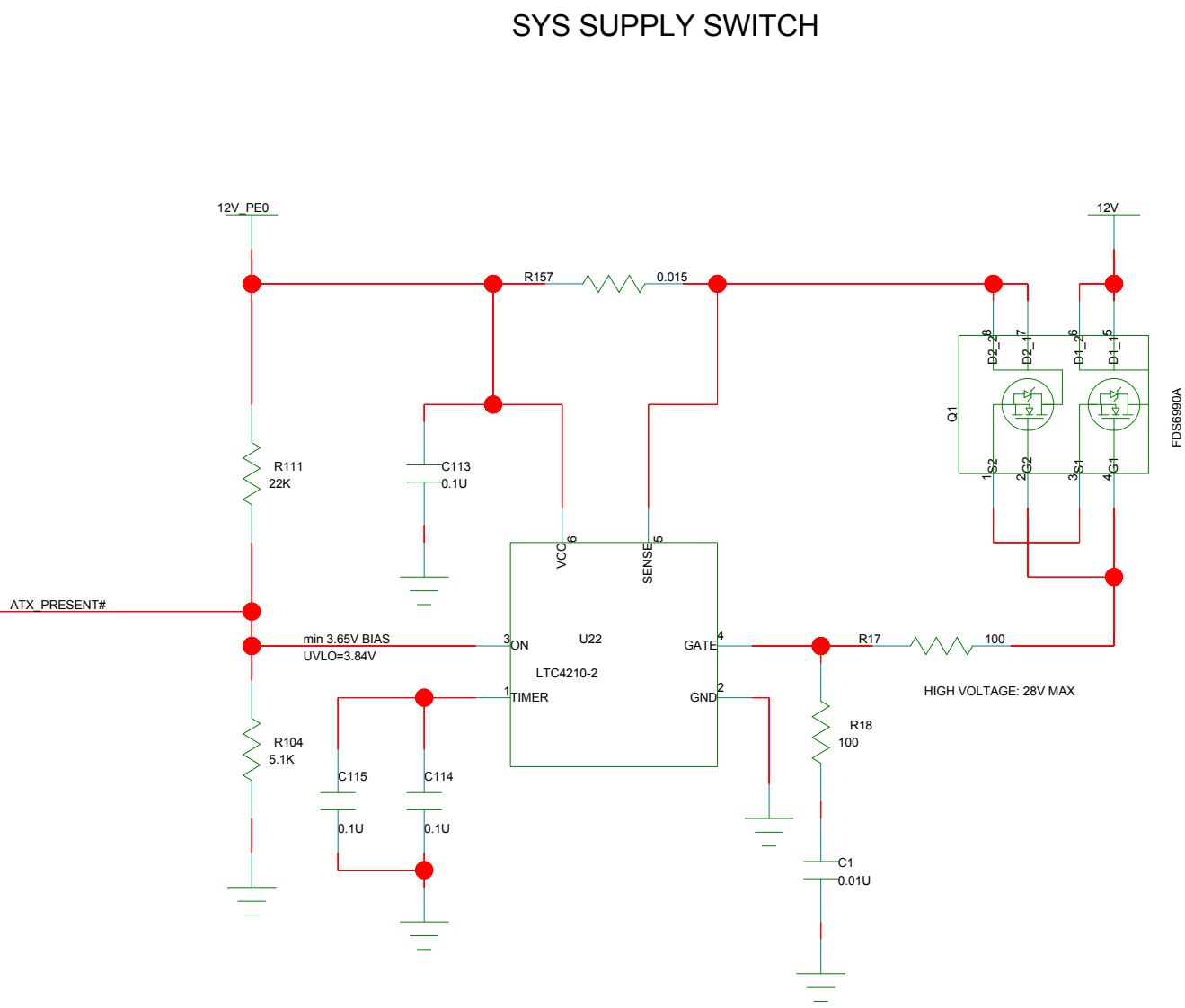
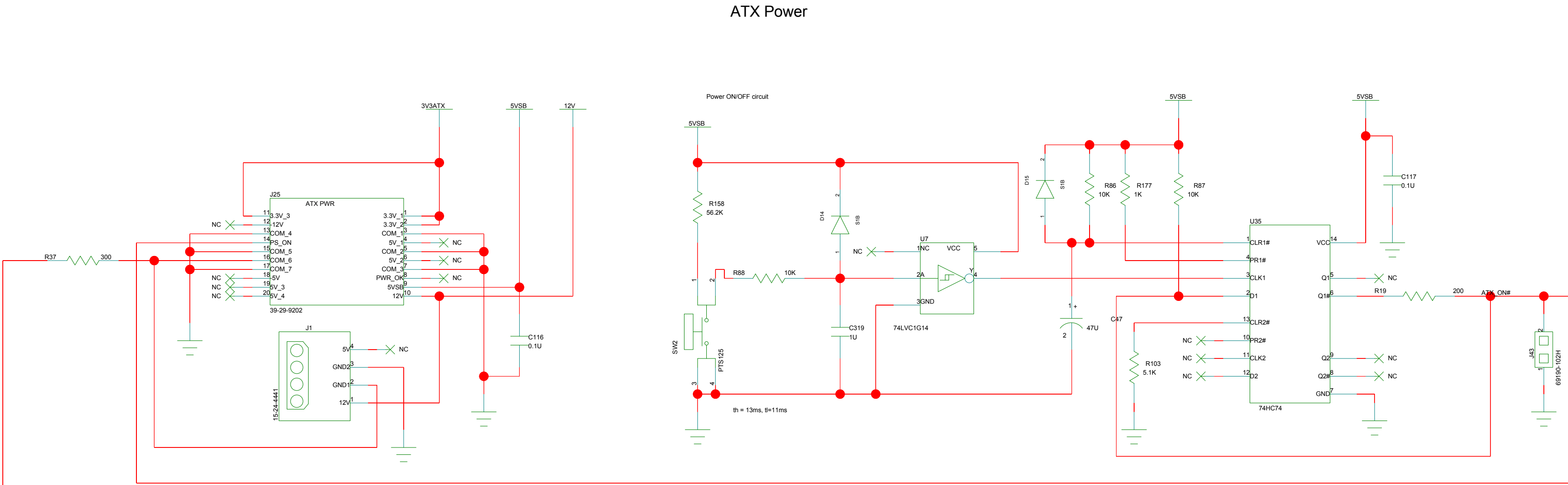
IDT has introduced new improved clocking solutions since this evaluation board was developed. The recommended timing solutions for new designs are:

- VersaClock 5 Devices:** In System Programmable, Very Low Power, with up to four universal output pairs.
- XUM LVDS Crystal Oscillator:** Ultra precise with only 300fs typical phase jitter. If using a 156.25 MHz clock source then the applicable part number is XUM535156.250JS6I8.



TITLE : CLOCKING			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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TITLE :
ATX POWER

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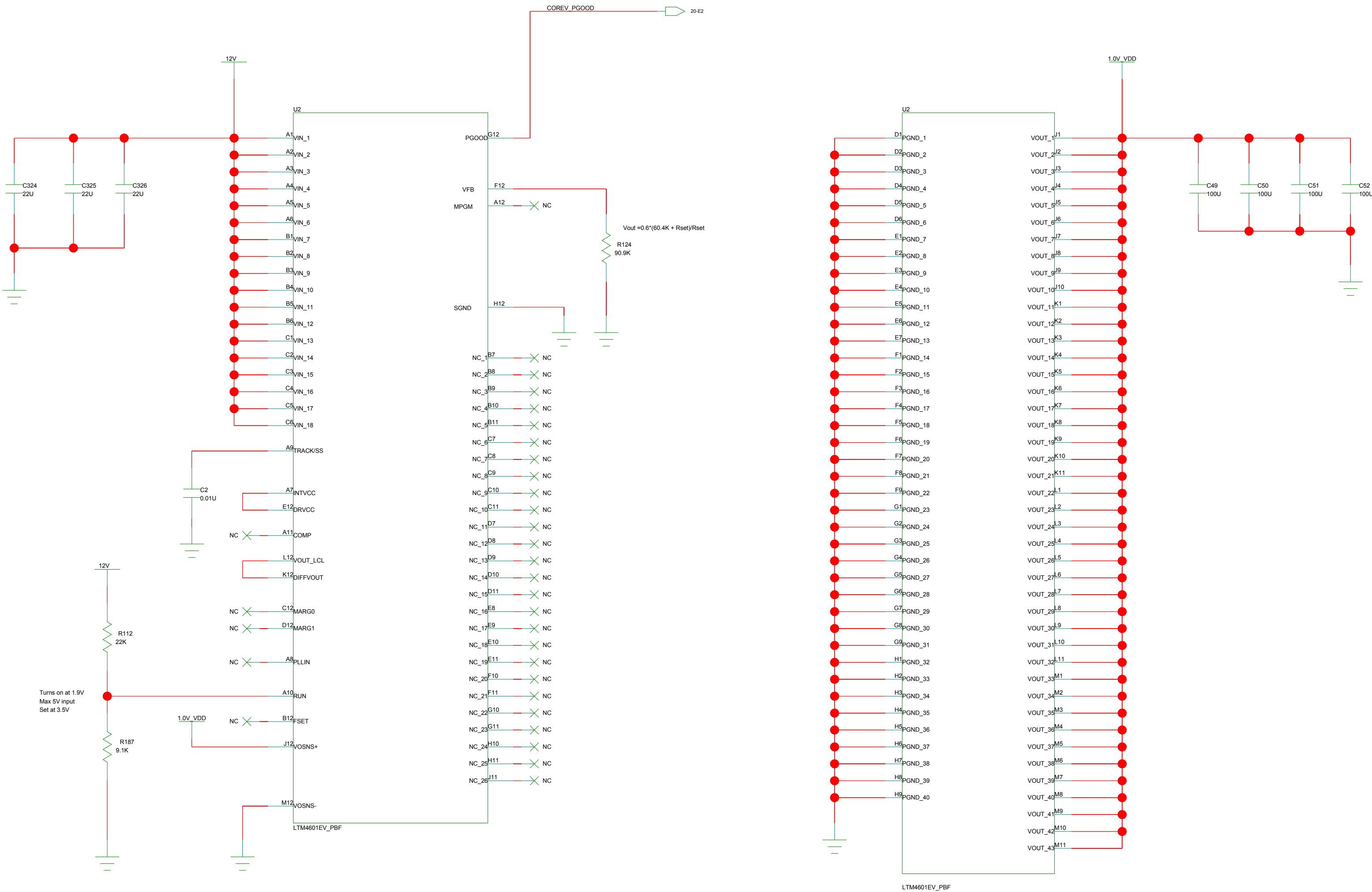
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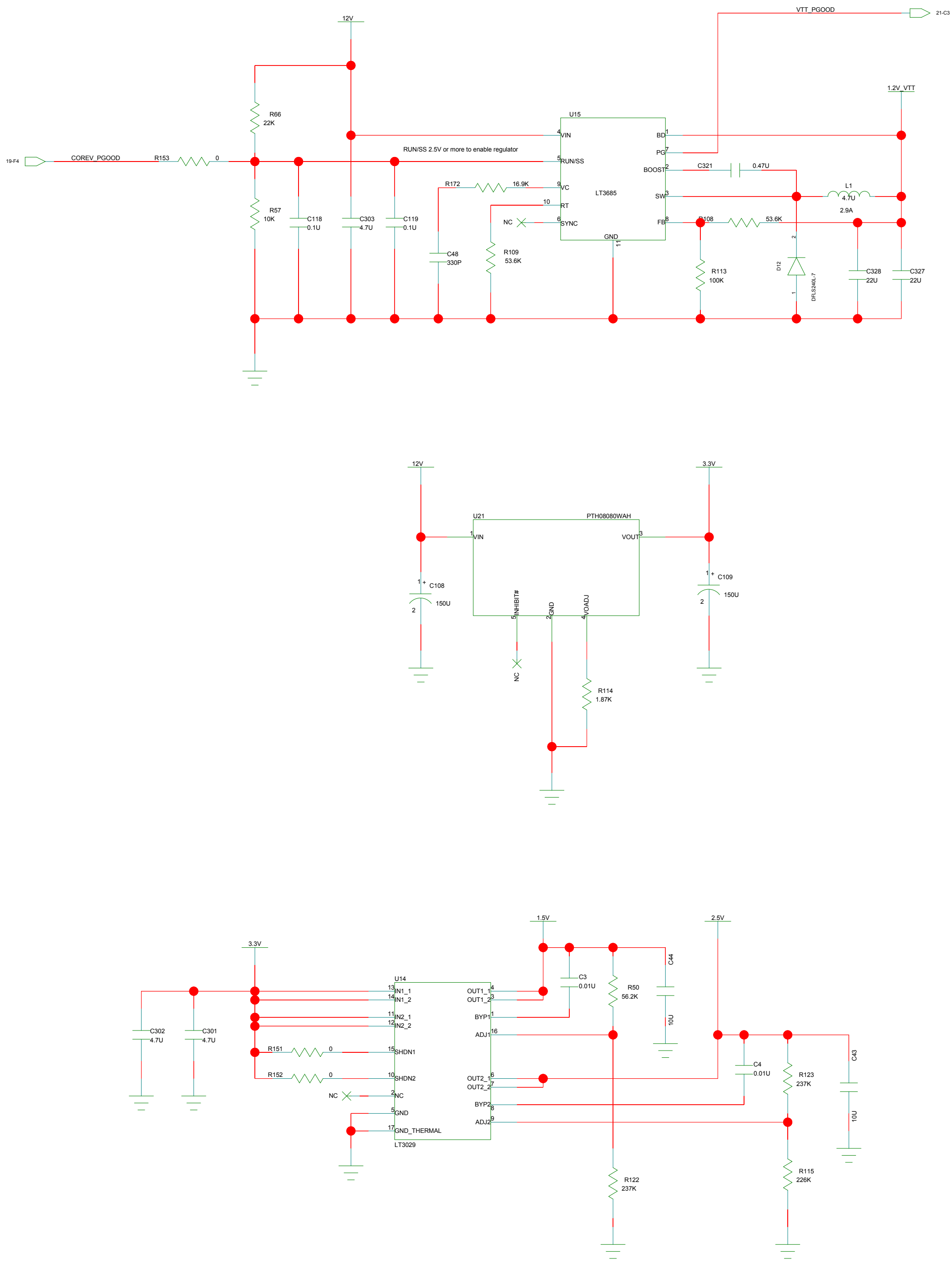
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Core Voltage Regulator



TITLE : CORE VOLTAGE REGULATOR			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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Voltage Regulators



TITLE : VOLTAGE REGULATORS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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Board Reset



TITLE

VOLTAGE MONITORS & BOARD RESET

SIZE

DRAWING NUMBER

Version

DESIGNER

LAST MODIFIED DATE

07-09-2011 13:17

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	1	2	3	4	5	6	7																				
F	Revision History							F																			
E	April 7, 2015 -- Added a note on page 16 on improving clocking solutions for S-RIO components. June 28, 2011 -- The following changes were made: * Sheet 4 - Added connections to ground on SP_SWAP_TX and SP_SWAP_RX * Sheet 4 - Added 10K pull up resistors to 3.3V on SP_DEVID, CLKSEL[0] and CLKSEL[1] * Sheet 4 - Added DNP attribute on U10 * Sheet 21 - Changed U13 to SN74AUP1G07 * Sheet 21 - Changed C320 to 0.1uF							E																			
D	April 11, 2011 -- First release of document.							D																			
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A						<table><tr><td colspan="4"></td></tr><tr><td colspan="4">TITLE : Revision History</td></tr><tr><td>SIZE C</td><td colspan="2">DRAWING NUMBER :</td><td>Version:</td><td colspan="2">DESIGNER :</td></tr><tr><td colspan="3">LAST MODIFIED DATE :</td><td colspan="2">SHEET</td></tr></table>						TITLE : Revision History				SIZE C	DRAWING NUMBER :		Version:	DESIGNER :		LAST MODIFIED DATE :			SHEET		A
																											
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