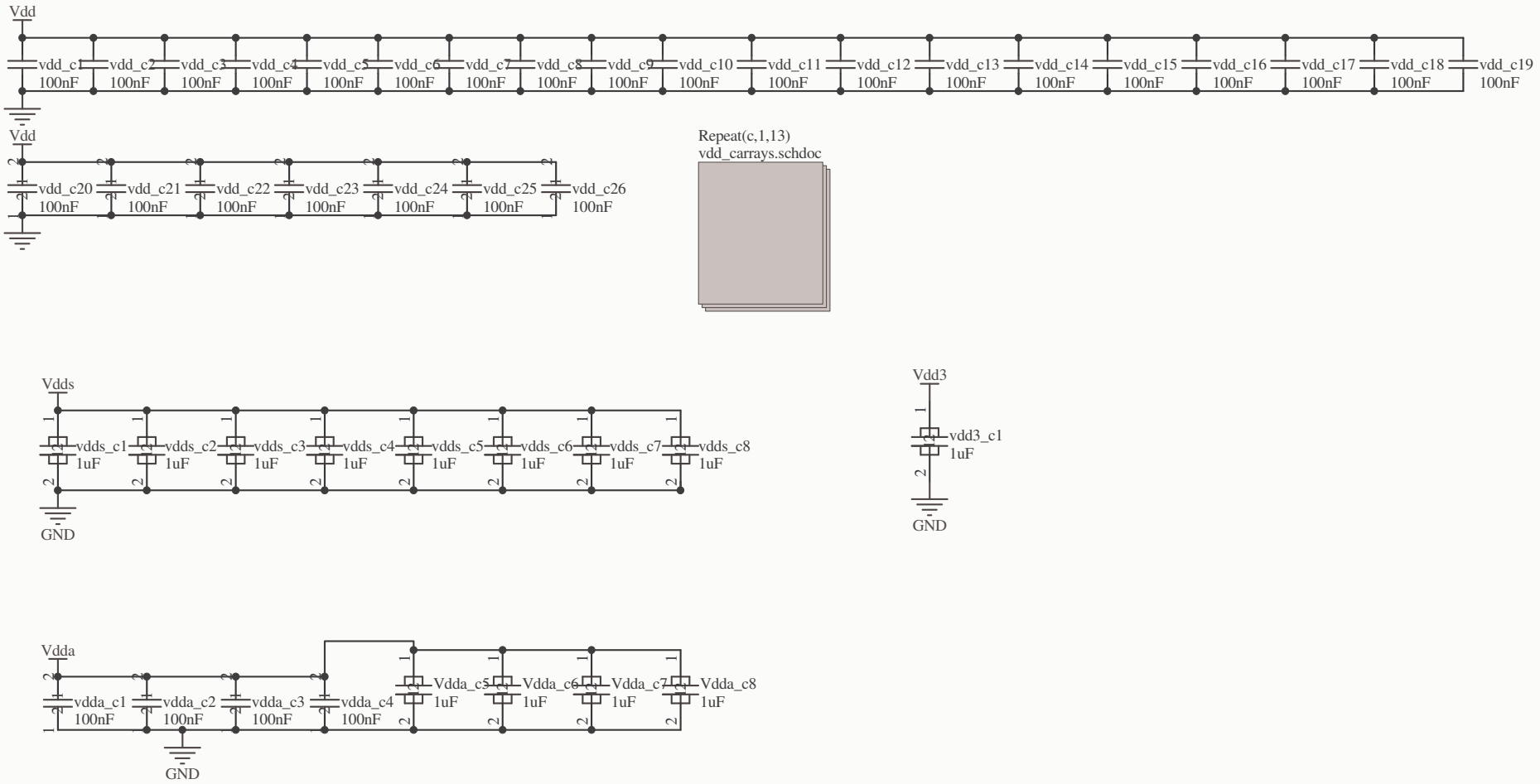

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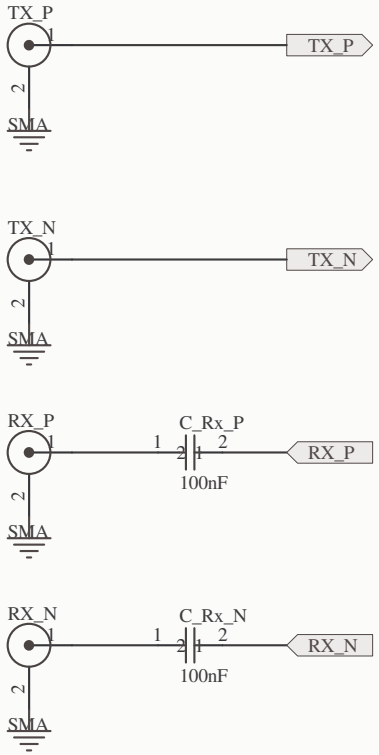
Date: 5/1/2007	Sheet of	
File: C:\Documents and Settings\..\Caps_jumps.SchDoc	Drawn By:	



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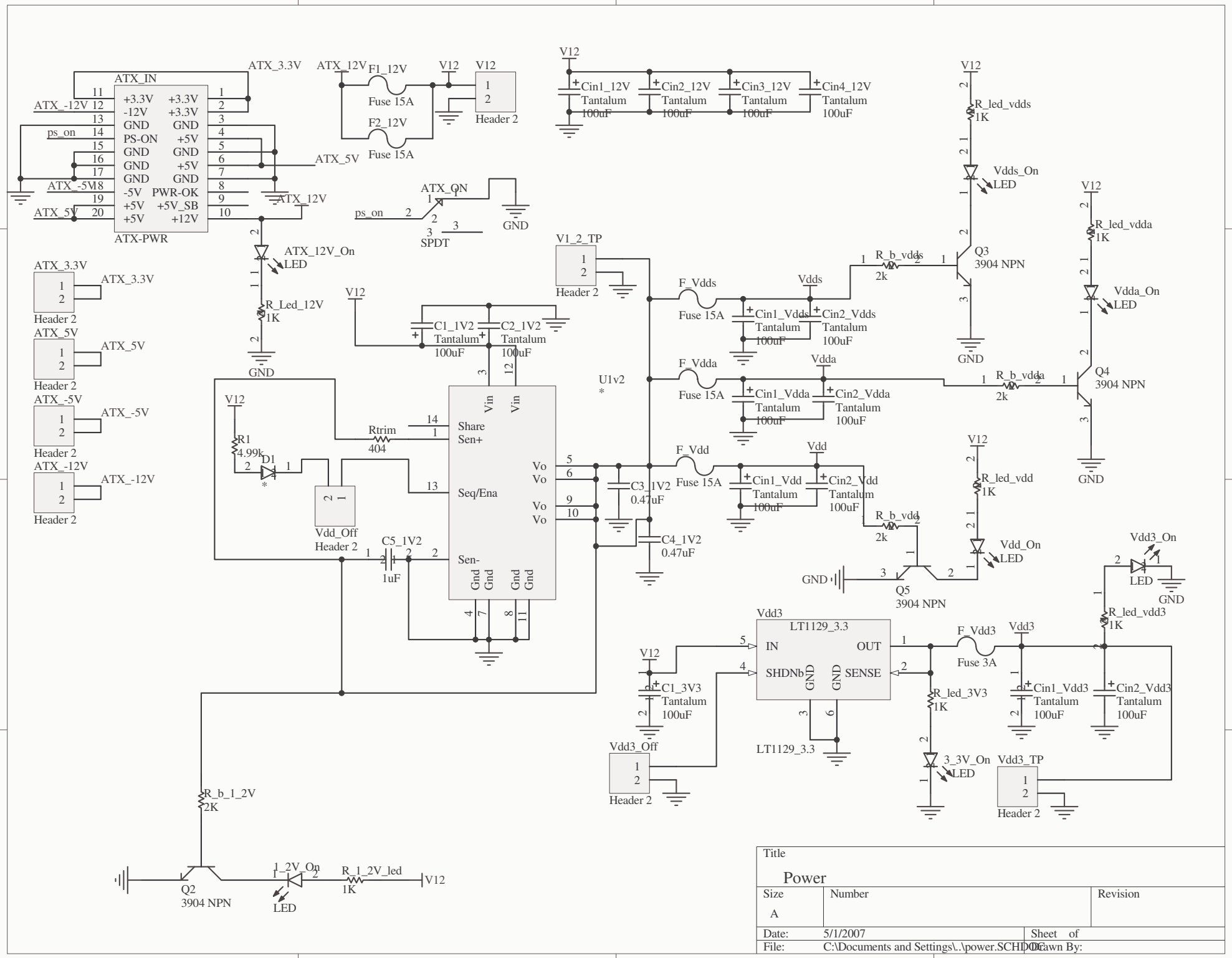
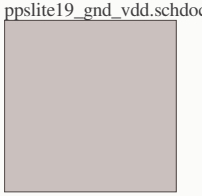
Date: 5/1/2007		Sheet of
File: C:\Documents and Settings\..\port.SchDoc		Drawn By:

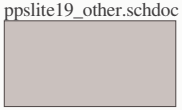

ATX_IN
ATX_3.3V
ATX_12V
F1_12V
F2_12V
Fuse 15A
Fuse 15A
Header 2
ATX_-12V
ps_on
ATX_5V
ATX_-5V
ATX_5V
ATX_12V
ATX-PWR
ATX_ON
SPDT
GND
ATX_12V_On
LED
R_Led_12V
1K
Cin1_12V
Cin2_12V
Cin3_12V
Cin4_12V
Tantalum
100uF
R_led_vdds
Vdds_On
R_led_vdda
Vdda_On
Q3
3904 NPN
Q4
3904 NPN
R_b_vdds
R_b_vdda
2k
V1_2_TP
F_Vdds
F_Vdda
F_Vdd
Vdds
Vdda
Vdd
Cin1_Vdds
Cin2_Vdds
Cin1_Vdda
Cin2_Vdda
Cin1_Vdd
Cin2_Vdd
C1_1V2
C2_1V2
U1v2
Rtrim
404
R1
4.99k
D1
Vdd_Off
C5_1V2
1uF
C3_1V2
0.47uF
C4_1V2
0.47uF
Share
Sen+
Seq/Ena
Sen-
Vin
Vo
Gnd
R_led_vdd
Vdd_On
Q5
3904 NPN
R_b_vdd
Vdd3_On
LED
LT1129_3.3
IN
OUT
SHDNb
GND
SENSE
F_Vdd3
Fuse 3A
Vdd3
C1_3V3
R_led_3V3
Cin1_Vdd3
Cin2_Vdd3
Vdd3_Off
3_3V_On
Vdd3_TP
R_led_vdd3
R_b_1_2V
2K
Q2
3904 NPN
1_2V_On
R_1_2V_led
Title
Power
Size
A
Number
Revision
Date:
5/1/2007
Sheet of
File:
C:\Documents and Settings\..\power.SCHDOC
Drawn By:

SRIO_LANES
srio_lanes.schdoc

PPSlite_vdd_gnd
ppslite19_gnd_vdd.schdoc



ppslite19_other
ppslite19_other.schdoc



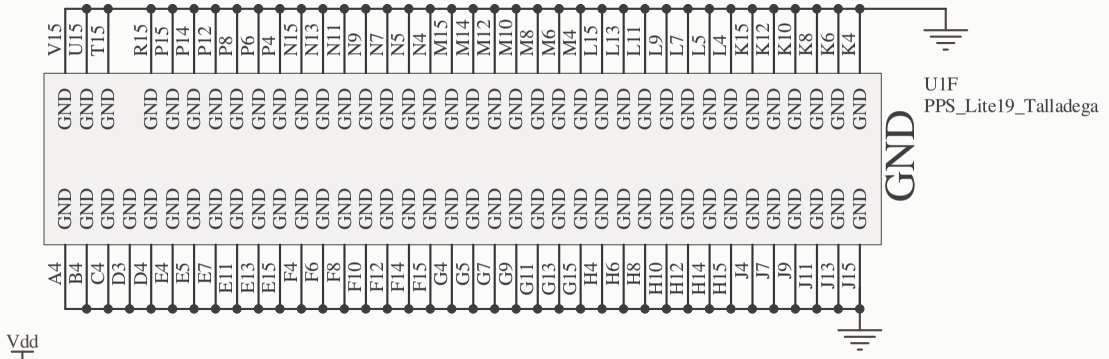
U1A

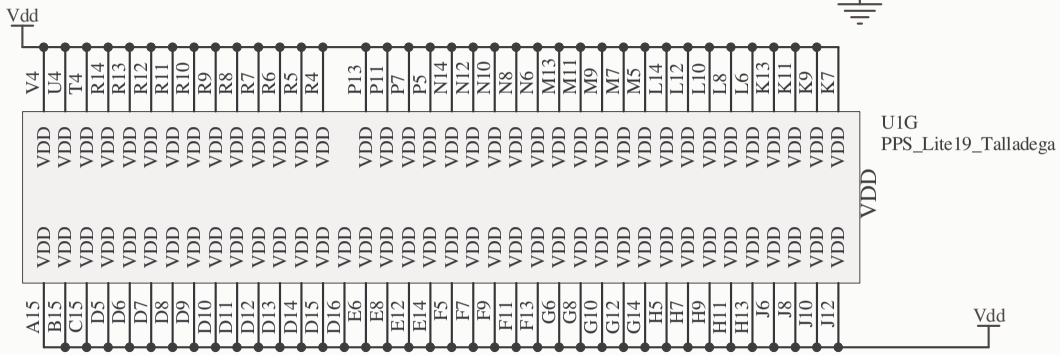
PPS_Lite19 / Talladega Top

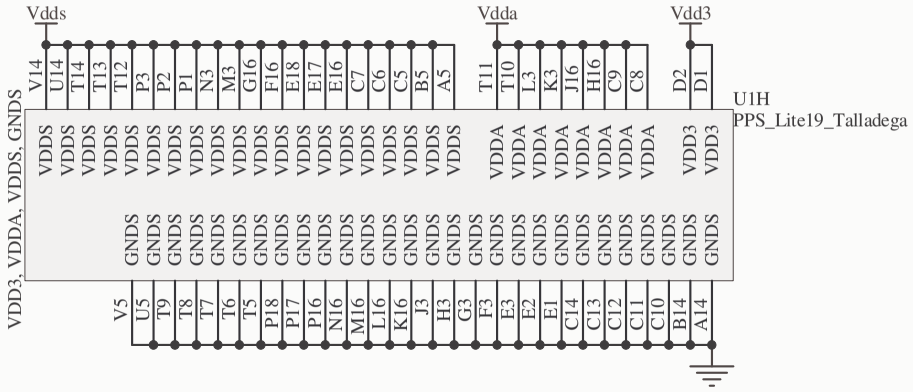
No Connect

PPS_Lite19_Talladega

Title	PPS_Lite/Talladega_Top		
Size: A	Number:		Revision:
Date:	5/1/2007	Sheet of	
File:	C:\Documents and Settings\..\ppslite19.SCHDOC	Drawn By:	



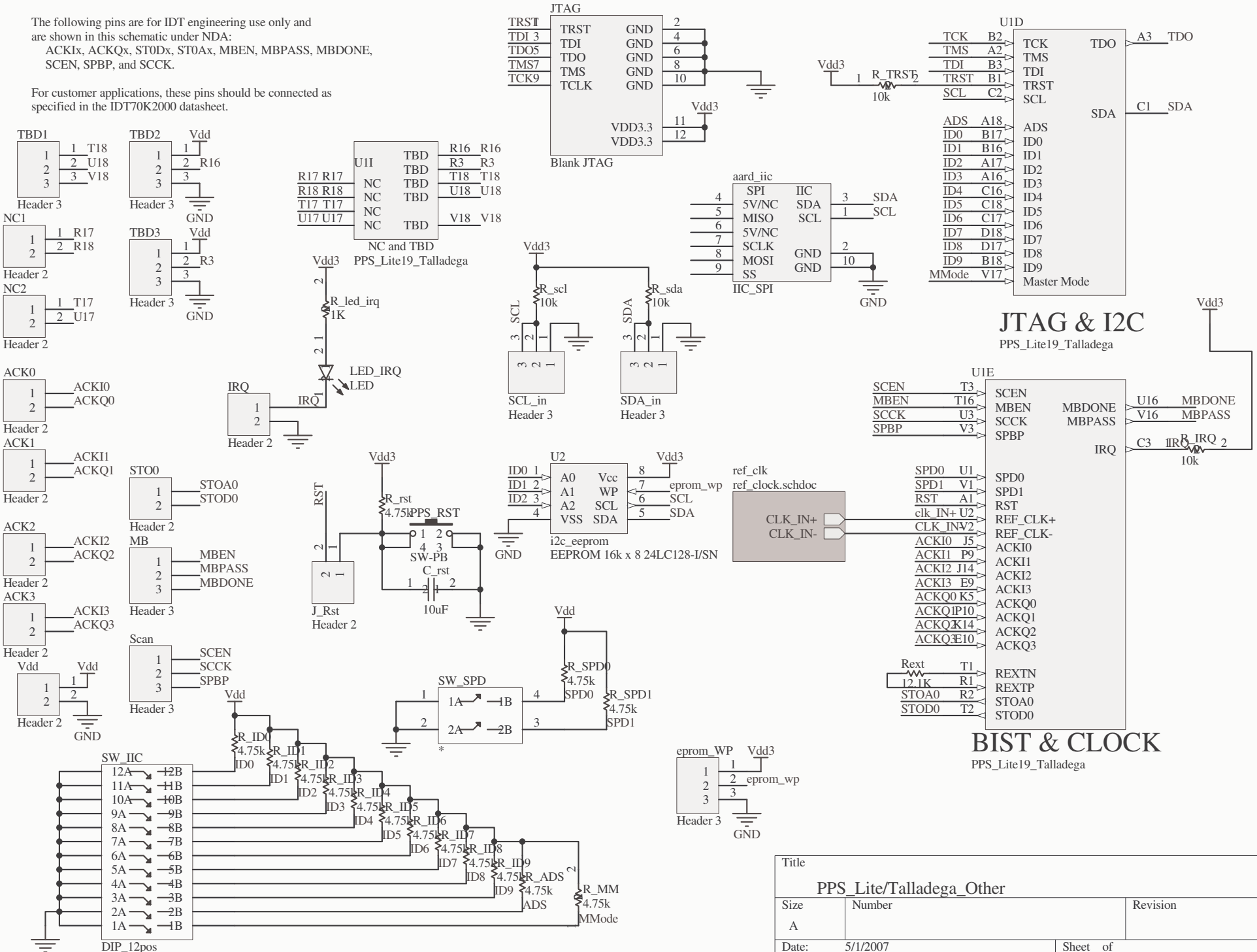




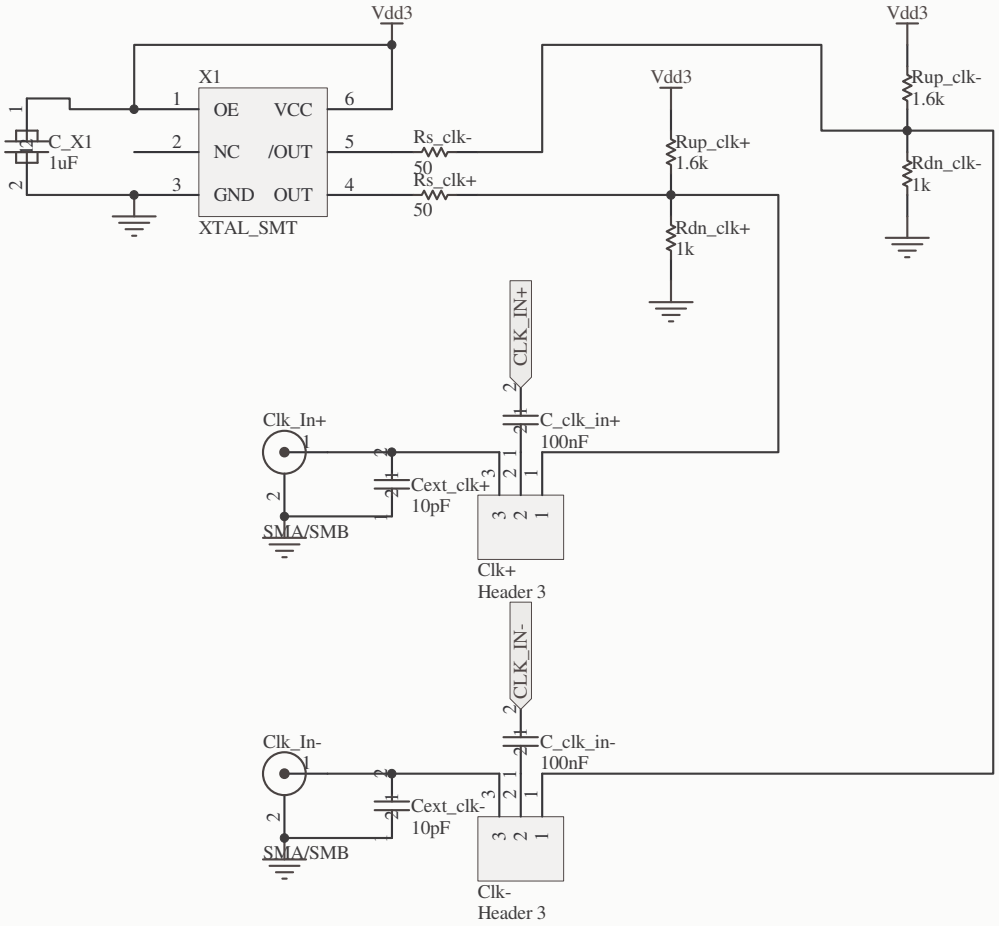
Title: PPS_Lite/Talladega_gnd_vdd		
Size: A	Number:	Revision:
Date: 5/1/2007	Sheet of	
File: C:\Documents and Settings\..\ppslite19_gnd_vdd.SCHDOC	Drawn By:	

The following pins are for IDT engineering use only and are shown in this schematic under NDA:
ACKIx, ACKQx, ST0Dx, ST0Ax, MBEN, MBPASS, MBDONE, SCEN, SPBP, and SCCK.

For customer applications, these pins should be connected as specified in the IDT70K2000 datasheet.

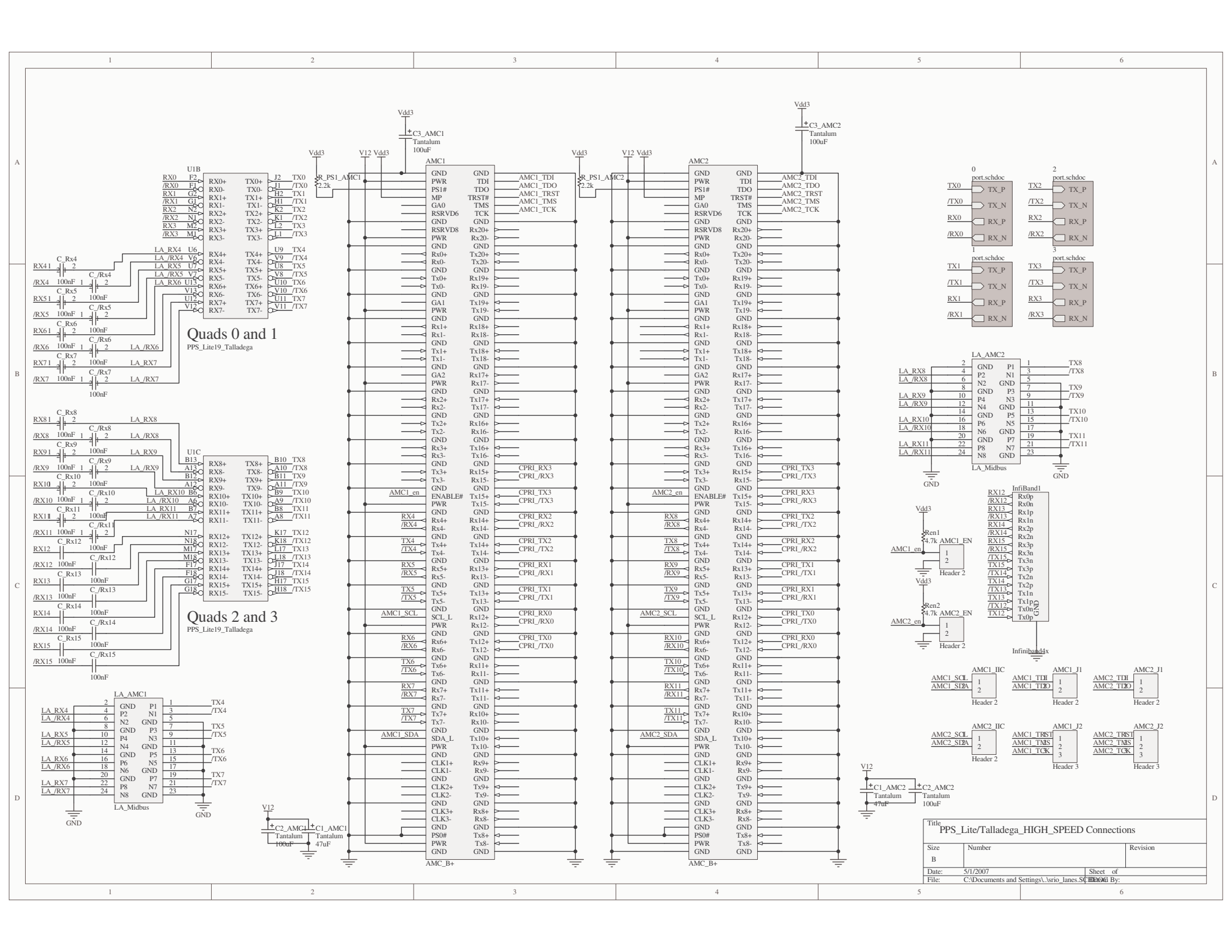


Title	PPS_Lite/Talladega_Other	
Size: A	Number	Revision
Date: 5/1/2007	Sheet of	
File: C:\Documents and Settings\..\ppslite19_other.SCHDOC	Drawn By:	

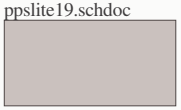


Clk Resistors for PECL oscillator.
For LVDS oscillator, do not populate Rup/Rdn
and replace Rs with 0 Ohm jumper

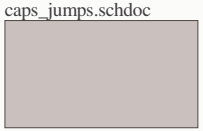
Title: Ref_Clock		
Size: A	Number:	Revision:
Date: 5/1/2007		Sheet of
File: C:\Documents and Settings\..\ref_clock.SCHDOC		Drawn By:


Quads 0 and 1
PPS_Lite19_Talladega
Quads 2 and 3
PPS_Lite19_Talladega
U1B
U1C
AMC1
AMC2
AMC_B+
LA_AMC1
LA_AMC2
LA_Midbus
GND
Vdd3
V12
C3_AMC1
C3_AMC2
Tantalum
100uF
R_PS1_AMC1
R_PS1_AMC2
2.2k
C_Rx4
C_Rx5
C_Rx6
C_Rx7
C_Rx8
C_Rx9
C_Rx10
C_Rx11
C_Rx12
C_Rx13
C_Rx14
C_Rx15
100nF
C1_AMC1
C2_AMC1
C1_AMC2
C2_AMC2
47uF
Ren1
Ren2
4.7k
AMC1_EN
AMC2_EN
Header 2
Header 3
InfiBand1
Infiniband4x
AMC1_IIC
AMC2_IIC
AMC1_J1
AMC2_J1
AMC1_J2
AMC2_J2
port.schdoc
TX_P
TX_N
RX_P
RX_N
Title
PPS_Lite/Talladega_HIGH_SPEED Connections
Size
B
Number
Revision
Date:
5/1/2007
Sheet of
File:
C:\Documents and Settings\..\srio_lanes.SCHDOC
By:

PPS_lite
ppslite19.schdoc

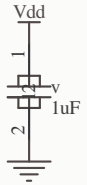


caps_jmps
caps_jumps.schdoc



PTB_power
power.schdoc

Title	Top		
Size A	Number		Revision
Date:	5/1/2007	Sheet of	
File:	C:\Documents and Settings\..\top.SCHDOC	Drawn By:	



Title	Vdd cap array		
Size: A	Number:		Revision:
Date:	5/1/2007	Sheet of	
File:	C:\Documents and Settings\..\vdd_carrays.SCHDOC	Drawn By:	