IDT80KSW0005/IDT80KSW0006 Evaluation Board User Guide

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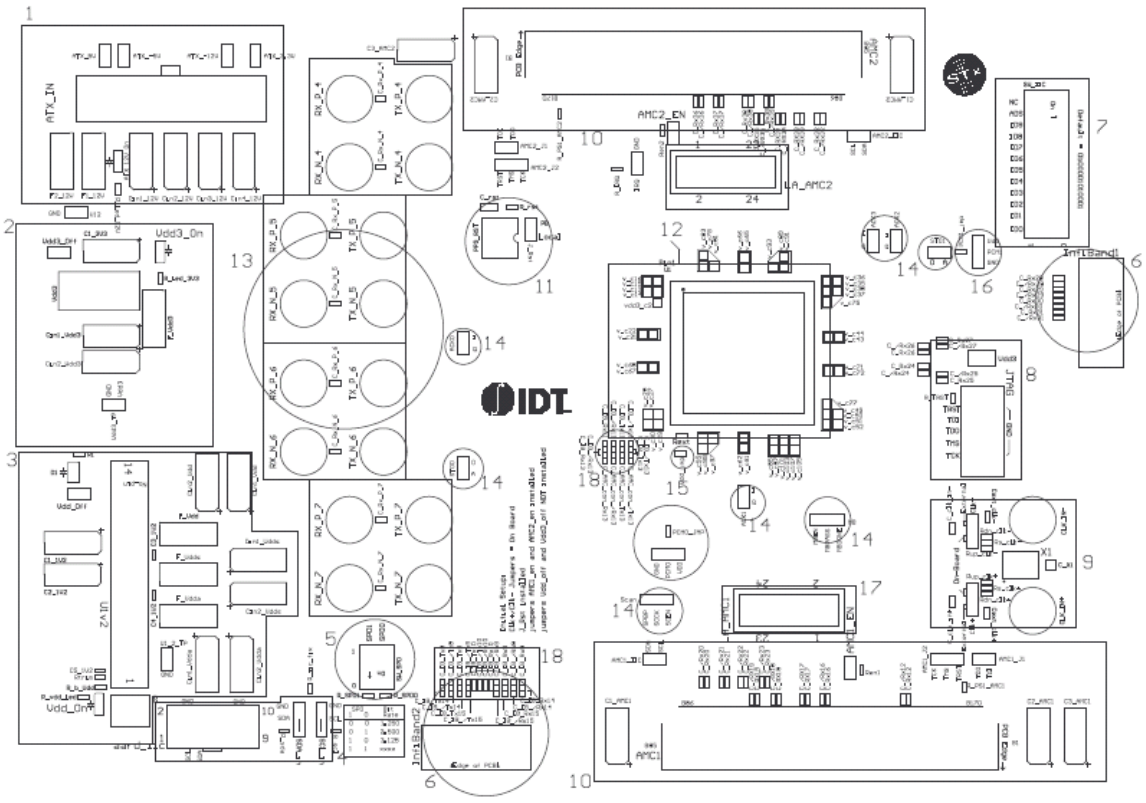
Revision History

Revision	Date	Author	Comments
0.5	September 6, 2006	Ryan Morley	Initial Draft.
1.5	April 5, 2007	Ryan Morley	Updated for board revision 1.5
1.6	July 25, 2008	Ryan Morley	Updated for board revision 1.5

Table of Contents

Introduction

This document is intended to provide an overview of the CPS-10Q/6Q Evaluation Board. Please note that lane numbers referenced in this document are referred to by the designator used for that physical location on the CPS-10Q/6Q. Ex: Lane 36 refers to the lane located at pins (A11, A12, B11, B12) on the package for both CPS-10Q/6Q and board applications.



CPS-10Q/6Q Evaluation Board Layout

CPS-10Q/6Q Eval Board Sections	
1	ATX power supply input
2	Vdd3 Power Supply
3	1.2 V power supply (Vdd, Vdda, and Vdds)
4	I2C input headers
5	CPS-10Q/6Q SPD Switches
6	Infiniband connectors
7	CPS-10Q/6Q I2C Address Switches
8	JTAG Inputs
9	Reference Clock
10	AMC connectors
11	CPS-10Q/6Q Reset Pushbutton
12	CPS-10Q/6Q
13	SRIO SMA connectors
14	CPS-10Q/6Q Logic Signal Headers
15	PCM0 jumper
16	PCM1 jumper
17	SRIO LA connections
18	CPS-10Q/6Q High Speed configuration jumpers

ATX Power Supply Input (1)

The CPS-10Q/6Q Evaluation Board is designed for use with a standard 20-pin ATX power supply. The evaluation board is powered by the 12V source on the ATX supply. Other Voltages from the ATX supply are not used by the evaluation board; however, these voltages can be accessed through the 0.100" headers included on the board.

The ATX supply should be able to provide approximately 150 Watts at 12V. This will allow for power supply margin under full load (2 AMC modules) condition.

Vdd3 Power Supply(2)

Component "Vdd3" is a 3.3V linear supply. Vdd3 is used to provide 3.3V power to the CPS-10Q/6Q, as well as to provide 3.3V management power to the AMC connectors. The output of Vdd3 is connected to the evaluation board by fuse F_Vdd3. When Vdd3 is enabled, LED Vdd3_On will be on. Vdd3 can be powered-down by installing jumper Vdd3_Off.

1.2V Power Supply (Vdd, Vdda, Vdds) (3)

The Voltage regulator U1v2 is used to provide 1.2V to the CPS-10Q/6Q supplies. U1v2 powers Vdd, Vdds, and Vdda. However, each of these Voltage domains are individually fused (F_Vddx) and distributed to the CPS-10Q/6Q through separate planes.

The output Voltage level of U1v2 is controlled by Rtrim. The default value of Rtrim, 402 Ohms, should provide an output of 1.2V. This level can be adjusted by changing the value of Rtrim.

When U1v2 is enabled, LED Vdd_On is on. U1v2 can be powered down by installing jumper Vdd_off.

I2C Input Headers (4)

The CPS-10Q/6Q I2C bus is connected to headers SDA_in and SCL_in. Resistor R_IIC_fix is a 100 Ohm series resistor on the CPS-10Q/6Q SDA signal. 10 pin header aard_iic is provided for connection to the Totalphase Aardvark™ I2C/SPI adapter.

CPS-10Q/6Q SPD Switches (5)

The CPS-10Q/6Q SPD pins are connected to DIP switch SW_SPD, and can be set to either 0 or 1. This controls the reset bit rate of the CPS-10Q/6Q SRIO ports.

Infiniband Connectors(6)

Two Infiniband 4x connectors are provided on the evaluation board. This is to allow for the connection of multiple evaluation boards. Please refer to Appendix A: High Speed Lane Mapping for lane mapping of the Infiniband connectors.

CPS-10Q/6Q I2C Address Switches (7)

SW_IIC is a 12-pos DIP switch for setting the CPS-10Q/6Q I2C address. Switch ADS selects 10-bit or 7-bit address mode. Switches ID9-ID0 set the CPS-10Q/6Q I2C address.

JTAG Inputs (8)

Connector JTAG provides access to the CPS-10Q/6Q JTAG pins. Connector JTAG is a 10 pin, 100 mil IDC header, which can be used with the Corelis JTAG controller.

Reference Clock (9)

The CPS-10Q/6Q is designed to operate with an AC coupled reference clock, at a frequency of 156.250 MHz. This can be implemented on the PTB using either an external clock source or the onboard crystal oscillator.

To use the onboard crystal oscillator, set Clk+ and Clk- jumpers to 'On_Board' setting.

To use an external clock source, set Clk+ and Clk- jumpers to 'External' setting, and connect a clock source to CLK_IN+ and CLK_IN- SMAs. 10pF shunt capacitors Cext_clk+ and Cext_clk- can be installed to slow the edge rate of the external clock signal when using equipment with very fast rise times. These are not installed in the default board setup.

The evaluation board is designed for use with PECL clock oscillators. For use of LVDS oscillators, remove Rdn_clk+/- and Rup_clk+/-, and replace 50 Ohm Rs_clk+/- with 0-Ohm resistors.

AMC Connectors(10)

Two AMC B+ connectors are provided on the evaluation board for use with AMC modules. These connectors do not implement full AMC functionality.

PS1# and PS0# pins are tied to proper levels. However, they are not used to control ENABLE#.

ENABLE# is held low by jumper AMCx_en. To disable the AMC module, remove jumper AMCx_en.

GA0-2 pins are floating (NC).

AMC JTAG and I2C pins are floating; header access is provided to these pins, if needed.

CLK1-3 are not implemented.

Please refer to Appendix A: High Speed Lane Mapping for lane mapping of the AMC connectors.

CPS-10Q/6Q Reset Pushbutton (11)

Pushbutton CPS-10Q/6Q_RST is used to hard-reset the CPS-10Q/6Q. Jumper J_Rst must be installed. Direct access to the CPS-10Q/6Q RST pin is available at the 'Local' pin of header J_Rst.

CPS-10Q/6Q (12)

The CPS-10Q/6Q Evaluation Board is designed for either solder-down or socketed use of the CPS-10Q/6Q. For socketed applications, use Ironwood Electronics C6204 GHz BGA socket.

SRIO SMA Connectors (13)

Lanes 4 – 7 of the CPS-10Q/6Q can be accessed through SMA connectors. AC-coupling capacitors are placed on the receiver paths.

If connecting the SMA outputs to test equipment (50 Ohm – Gnd termination), SMA – SMA DC – Blocks should be used. It is important to note that this board is not designed for parametric measurements, and the outputs when viewed on a scope are not an accurate measure of transmitter performance.

CPS-10Q/6Q Logic Signal Headers (14)

Access to the CPS-10Q/6Q logic and test pins is available at headers located near the CPS-10Q/6Q.

PCM0 Jumper (15) and PCM1 Jumper (16)

No use in CPS-10Q/6Q

SRIO LA Connections

Compression style logic analyzer connections are provided for functional probing SRIO traffic. Please refer to Appendix A: High Speed Lane Mapping for signal availability on the SRIO LA connections.

CPS-10Q/6Q High Speed Configuration Jumpers

To allow for use with both the CPS-10Qand CPS-6Q, the evaluation board includes jumper capability on certain SRIO lanes, so that lane to connector mapping can be optimized for the DUT. These jumpers are series 0402 capacitors on the high speed signals. Please refer to Appendix A: High Speed Lane Mapping for a detailed description of port configurability using jumpers.

Appendix A: High Speed Lane Mapping

The following table outlines the high speed lane mapping of the CPS-10Q/6Q Evaluation board for both CPS-10Q and CPS6Q applications.

CPS-10Q Lane number		CPS-6Q Lane number		
0		0		
1		1		
2		2		
3	Quad 0 / Standard	3	Quad 0 / Standard	No Connect
4				
5				
6				
7	Quad 1 / Standard		N/A	SMA
8		4		
9		5		
10		6		
11	Quad 2 / Standard	7	Quad 1 / Standard	Inifiniband Connector2
12				
13				
14				
15	Quad 3 / Standard		N/A	AMC1 Control Port
16		8		
17		9		
18		10		
19	Quad 4 / Enhanced	11	Quad 2 / Enhanced	AMC1 Fat Pipes Region ports 4-7
20		12		
21		13		
22		14		AMC1 Fat Pipes Region ports 8-11;
23	Quad 5 / Standard	15	Quad 3 / Standard	LA_AMC1
24				
25				
26				
27	Quad 6 / Standard		N/A	Loopback
28		16		
29		17		
30		18		
31	Quad 7 / Standard	19	Quad 4 / Standard	Inifiniband Connector1
32				
33				
34				
35	Quad 8 / Standard		N/A	AMC2 fat pipes region ports 8-11
36		20		
37		21		
38		22		AMC2 Fat Pipes Region ports 4-7;
39	Quad 9 / Enhanced	23	Quad 5 / Enhanced	LA_AMC2