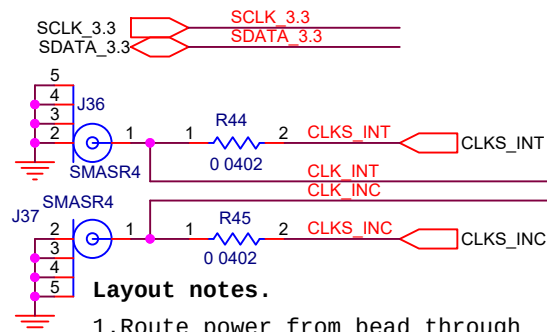


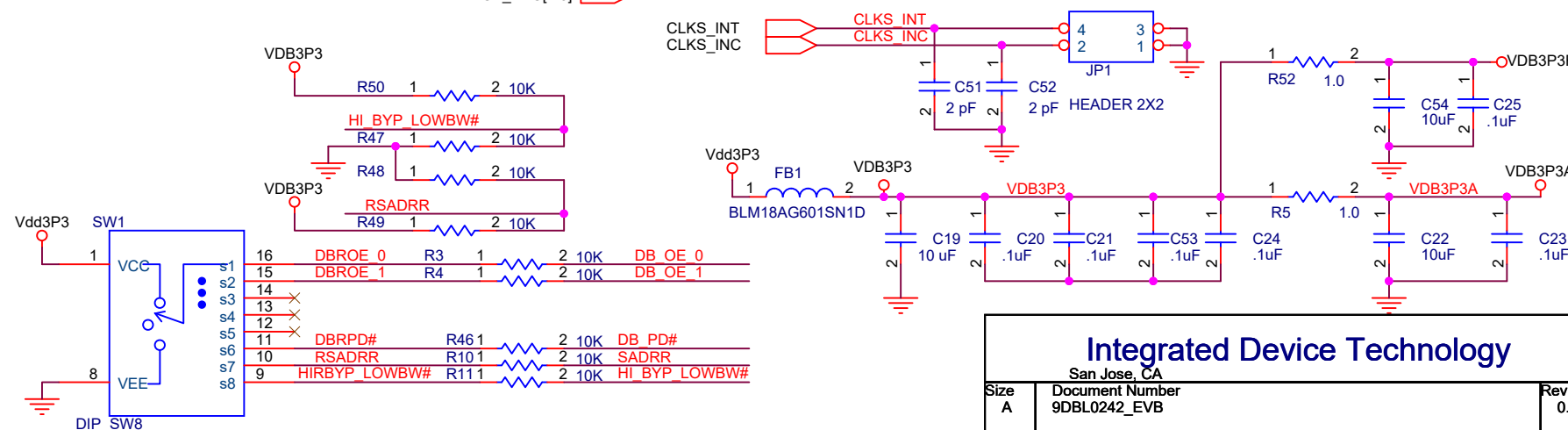
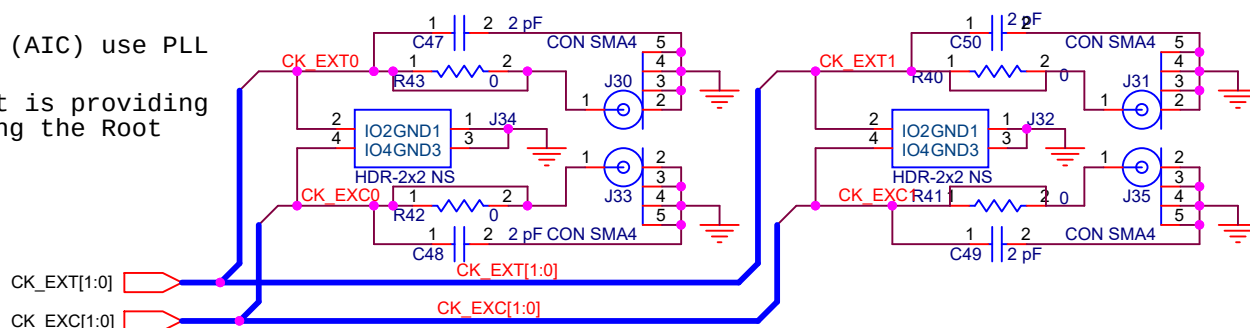
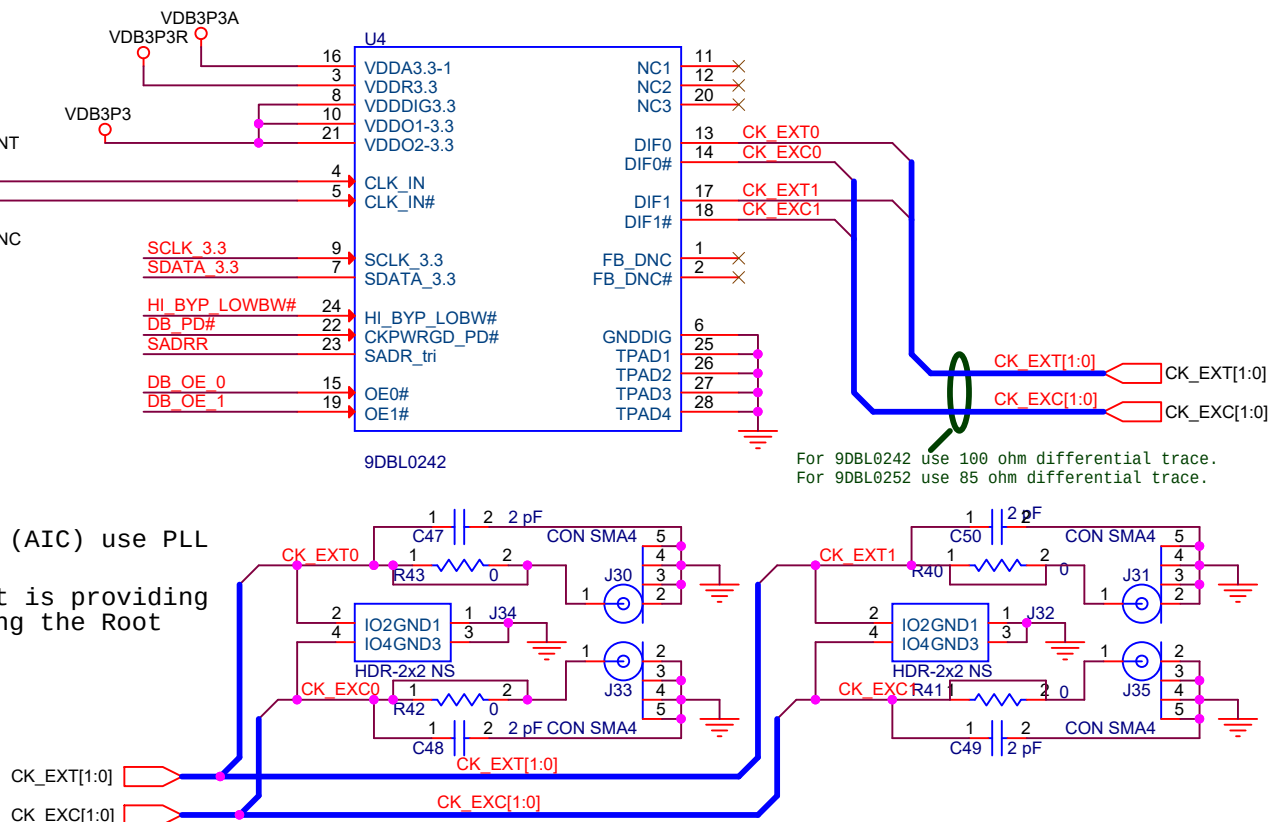


Layout notes.

- 1.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
- 2.Do not share ground vias. One ground pin one ground via.
- 3.Exposed pad should be grounded but is not required.

Bandwidth setting

1. If the ZDB is on an Add-In-Card (AIC) use PLL bypass mode.
2. If it is motherboard down and it is providing clocks to all PCIe devices including the Root Complex use High Bandwidth.



Integrated Device Technology

San Jose, CA

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