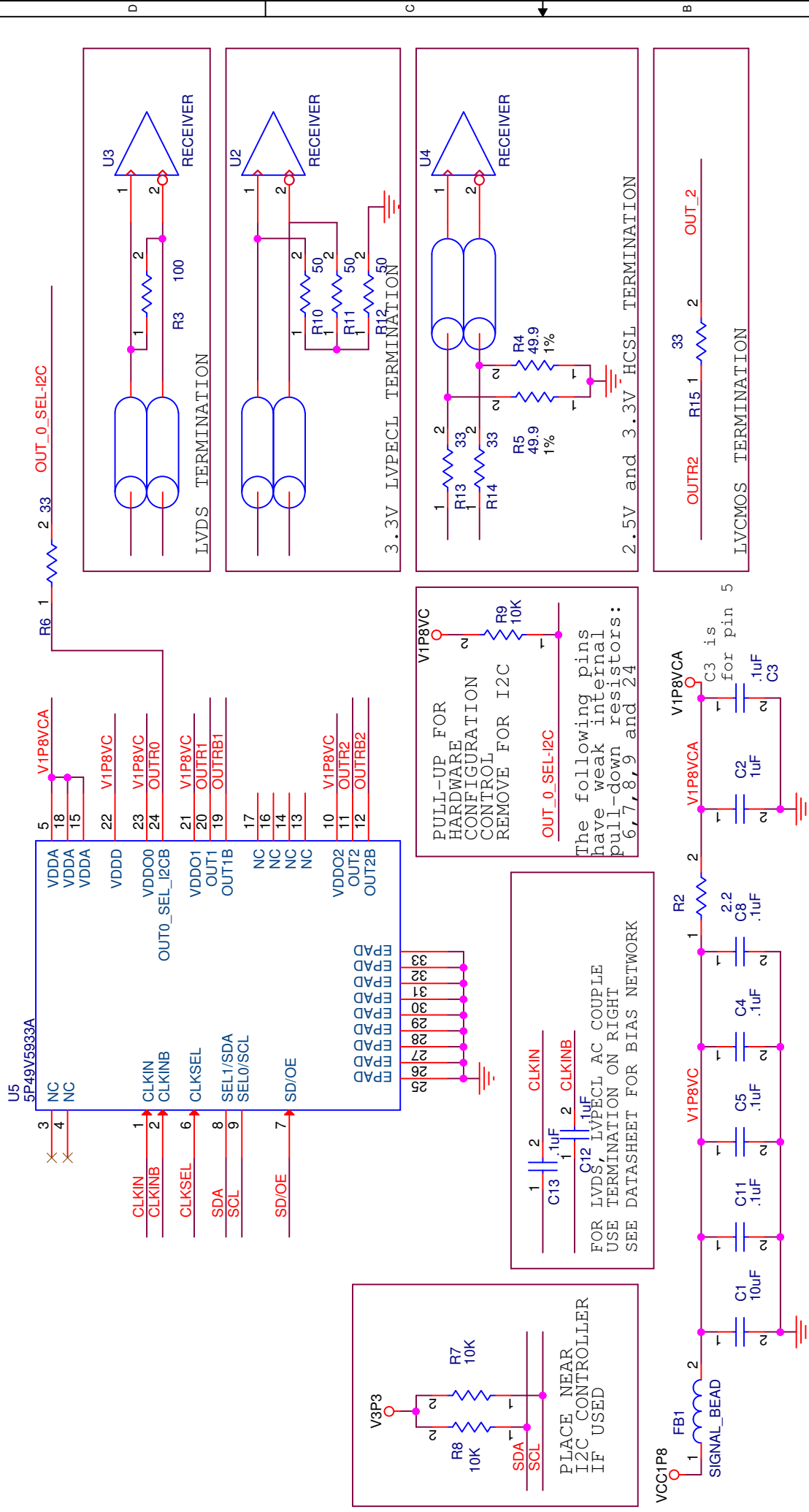




Layout notes:

- 1 Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
- 2 Do not share ground vias. One ground pin one ground via.

| NOTE:FERRITE BEAD = | Zq100MHz      | PkgSz | DC res. | Current (Ma) |
|---------------------|---------------|-------|---------|--------------|
| Manufacture         | 120           | 0402  | 0.5     | 200          |
| Fair-Rite           | 2504021217Y0  | 240   | 0.18    | 200          |
| TDK                 | MMZ1005S241A  | 0402  | 0.35    | 300          |
| muRata              | BLM15AG221SN1 | 0402  | 0.35    | 300          |
| muRata              | BLM15BB121SN1 | 0402  | 0.3     | 300          |
| TFCSTAR             | TB4532153121  | 0402  | 0.3     | 300          |

Revision history

|     |            |                    |
|-----|------------|--------------------|
| 0.1 | 03/26/2015 | First publication  |
| 0.2 | 04/25/16   | pin out correction |

# Integrated Device Technology

San Jose, CA

|       |                        |              |
|-------|------------------------|--------------|
| Size  | Document Number        | Rev          |
| A     | 5P49V5933A_SCH         | 0.1          |
| Date: | Monday, April 25, 2016 | Sheet 1 of 1 |