Smart Configurator for RX V2.7.0

Release Note

R20UT4487ES0271
Rev.2.71
Oct.30.20

Introduction

Thank you for using the Smart Configurator for RX.
This document describes the restrictions and points for caution. Read this document before using the product.

Contents

1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

1.1 System requirements

The operating environment is as follows.

1.1.1 PC

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-bit Windows requires 2 GB or more)
- Hard disk capacity: 200 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to Windows OS: Java Runtime Environment

1.1.2 Development Environments

- Renesas electronics Compiler for RX [CC-RX] V3.01.00 or later
- GCC for Renesas 4.8.4.201902 or later
- IAR Embedded Workbench 4.12.1 or later

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RX V2.7.0.

Table 2-1 Support Devices

Group (HW Manual number)	PIN	Device name
RX110 Group (R01UH0421EJ0120)	36pin	R5F5110HAxLM, R5F5110JAxLM, R5F51101AxLM, R5F51103AxLM
	40pin	R5F51101AxNF, R5F51103AxNF, R5F5110HAxNF, R5F5110JAxNF
	48pin	R5F51101AxNE, R5F51103AxNE, R5F51104AxNE, R5F51105AxNE, R5F5110JAxNE, R5F51101AxFL, R5F51103AxFL, R5F51104AxFL, R5F51105AxFL, R5F5110JAxFL
	64pin	R5F51101AxLF, R5F51103AxLF, R5F51104AxLF, R5F51105AxLF, R5F5110JAxLF, R5F51101AxFK, R5F51103AxFK, R5F51104AxFK, R5F51105AxFK, R5F5110JAxFK, R5F51101AxFM, R5F51103AxFM, R5F51104AxFM, R5F51105AxFM, R5F5110JAxFM
RX111 Group (R01UH0365EJ0130)	36pin	R5F51111AxLM, R5F51113AxLM, R5F5111JAxLM
	40pin	R5F51111AxNF, R5F51113AxNF, R5F5111JAxNF
	48pin	R5F51111AxFL, R5F51113AxFL, R5F51114AxFL, R5F51115AxFL, R5F51116AxFL, R5F51117AxFL, R5F51118AxFL, R5F5111JAxFL, R5F51111AxNE, R5F51113AxNE, R5F51114AxNE, R5F51115AxNE, R5F51116AxNE, R5F51117AxNE, R5F51118AxNE, R5F5111JAxNE
	64pin	R5F51111AxFM, R5F51113AxFM, R5F51114AxFM, R5F51115AxFM, R5F51116AxFM, R5F51117AxFM, R5F51118AxFM, R5F5111JAxFM, R5F51111AxFK, R5F51113AxFK, R5F51114AxFK, R5F51115AxFK, R5F51116AxFK, R5F51117AxFK, R5F51118AxFK, R5F5111JAxFK, R5F51111AxLF, R5F51113AxLF, R5F51114AxLF, R5F51115AxLF, R5F51116AxLF, R5F51117AxLF, R5F51118AxLF, R5F5111JAxLF
RX113 Group (R01UH0448EJ0110)	64pin	R5F51135AxFM, R5F51136AxFM, R5F51137AxFM, R5F51138AxFM
	100pin	R5F51135AxLJ, R5F51136AxLJ, R5F51137AxLJ, R5F51138AxLJ, R5F51135AxFP, R5F51136AxFP, R5F51137AxFP, R5F51138AxFP
RX130 Group (R01UH0560EJ0200)	48pin	R5F51303AxFL, R5F51305AxFL, R5F51303AxNE, R5F51305AxNE, R5F51306AxNE, R5F51306AxFL, R5F51307AxNE, R5F51307AxFL, R5F51308AxNE, R5F51308AxFL, R5F51306BxFL
	64pin	R5F51303AxFM, R5F51305AxFM, R5F51303AxFK, R5F51305AxFK, R5F51306AxFK, R5F51306AxFM, R5F51307AxFK, R5F51307AxFM, R5F51308AxFK, R5F51308AxFM R5F51308AxFK, R5F51308AxFM, R5F51306BxFK, R5F51306BxFM
	80pin	R5F51303AxFN, R5F51305AxFN, R5F51306AxFN, R5F51306BxFN
	100pin	R5F51305AxFP, R5F51306AxFP, R5F51307AxFP, R5F51308AxFP, R5F51305BxFP, R5F51306BxFP
RX13T Group (R01UH0822EJ0100)	32pin	R5F513T3AxFJ, R5F513T5AxFJ, R5F513T3AxNH, R5F513T5AxNH
	48pin	R5F513T5AxFL, R5F513T3AxFL, R5F513T5AxNE, R5F513T3AxNE
RX230 Group (R01UH0496EJ0110)	48pin	R5F52305AxNE, R5F52306AxNE, R5F52305AxFL, R5F52306AxFL
	64pin	R5F52305AxND, R5F52306AxND, R5F52305AxFM, R5F52306AxFM, R5F52305AxLF, R5F52306AxLF
	100pin	R5F52305AxLA, R5F52306AxLA, R5F52305AxFP, R5F52306AxFP

Table 2-2 Support Devices

Group (HW Manual number)	PIN	Device name
RX231 Group (R01UH0496EJ0110)	48pin	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64pin	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, R5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, R5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100pin	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23E-A Group (R01UH0801EJ0100)	40pin	R5F523E5AxNF, R5F523E6AxNF, R5F523E5SxNF, R5F523E6SxNF
	48pin	R5F523E5AxFL, R5F523E6AxFL, R5F523E5SxFL, R5F523E6SxFL
RX23T Group (R01UH0520EJ0110)	48pin	R5F523T3AxFL, R5F523T5AxFL
	52pin	R5F523T5AxFD, R5F523T3AxFD
	64pin	R5F523T5AxFM, R5F523T3AxFM
RX23W Group (R01UH0823EJ0100)	56pin	R5F523W8BxNG, R5F523W8AxNG, R5F523W7BxNG, R5F523W7AxNG
	83pin	R5F523W8CxLN, R5F523W8DxLN
	85pin	R5F523W7AxBL, R5F523W8AxBL, R5F523W8BxBL, R5F523W7BxBL
RX24T Group (R01UH0576EJ0200)	64pin	R5F524TAAxFM, R5F524T8AxFM, R5F524TAAxFK, R5F524T8AxFK
	80pin	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100pin	R5F524TCAxFP, R5F524T8AxFP, R5F524TBAxFP, R5F524TEAxFP, R5F524TAAxFP
RX24U Group (R01UH0658EJ0100)	100pin	R5F524UEAxFP, R5F524UCAxFP, R5F524UBAxFP
	144pin	R5F524UEAxFB, R5F524UBAxFB, R5F524UCAxFB
RX64M Group (R01UH0377EJ0110)	100pin	R5F564MFCxFP, R5F564MFCxLJ, R5F564MFDxFP, R5F564MFDxLJ, R5F564MGCxFP, R5F564MGCxLJ, R5F564MGDxFP, R5F564MGDxLJ, R5F564MJCxFP, R5F564MJCxLJ, R5F564MJDxFP, R5F564MJDxLJ, R5F564MLCxFP, R5F564MLCxLJ, R5F564MLDxFP, R5F564MLDxLJ
	144/145pin	R5F564MFCxFB, R5F564MFCxLK, R5F564MFDxFB, R5F564MFDxLK, R5F564MGCxFB, R5F564MGCxLK, R5F564MGDxFB, R5F564MGDxLK, R5F564MJCxFB, R5F564MJCxLK, R5F564MJDxFB, R5F564MJDxLK, R5F564MLCxFB, R5F564MLCxLK, R5F564MLDxFB, R5F564MLDxLK
	176/177pin	R5F564MFDxFC, R5F564MFDxBG, R5F564MFDxLC, R5F564MFCxFC, R5F564MFCxBG, R5F564MFCxLC, R5F564MGDxFC, R5F564MGDxBG, R5F564MGDxLC, R5F564MGCxFC, R5F564MGCxBG, R5F564MGCxLC, R5F564MJDxFC, R5F564MJDxBG, R5F564MJDxLC, R5F564MJCxFC, R5F564MJCxBG, R5F564MJCxLC, R5F564MLDxFC, R5F564MLDxBG, R5F564MLDxLC, R5F564MLCxFC, R5F564MLCxBG, R5F564MLCxLC

Table 2-3 Support Devices

Group (HW Manual number)	PIN	Device name
RX65N Group (R01UH0590EJ0210)	100pin	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP, R5F565NCHxLJ, R5F565NCDxLJ, R5F565NEHxLJ, R5F565NEDxLJ, R5F565NCHxFP, R5F565NCDxFP, R5F565NEHxFP, R5F565NEDxFP
	144/145pin	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565NCHxFB, R5F565NCDxFB, R5F565NEHxFB, R5F565NEDxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK, R5F565NCHxLK, R5F565NCDxLK, R5F565NEHxLK, R5F565NEDxLK
	176/177pin	R5F565NCHxBG, R5F565NCDxBG, R5F565NEHxBG, R5F565NEDxBG, R5F565NCHxFC, R5F565NCDxFC, R5F565NEHxFC, R5F565NEDxFC, R5F565NCHxLC, R5F565NCDxLC, R5F565NEHxLC, R5F565NEDxLC
RX651 Group (R01UH0590EJ0210)	64pin	R5F5651CHxFM,R5F56514FxFM, R5F5651EHxFM, R5F5651CDxFM, R5F56514FxBP, R5F56514BxFM, R5F56519FxBP, R5F5651CDxBP, R5F5651EDxBP, R5F5651EDxFM, R5F56517BxBP, R5F5651EHxBP, R5F56519BxBP, R5F56517FxBP, R5F5651CHxBP, R5F56519FxFM, R5F56517BxFM, R5F56514BxBP, R5F56519BxFM, R5F56517FxFM
	100pin	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145pin	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F5651CDxFB, R5F5651CHxFB, R5F5651EDxFB, R5F5651EHxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK, R5F5651CDxLK, R5F5651CHxLK, R5F5651EDxLK, R5F5651EHxLK
	176/177pin	R5F5651CDxBG, R5F5651CDxFC, R5F5651CHxBG, R5F5651CHxFC, R5F5651EDxBG, R5F5651EDxFC, R5F5651EHxBG, R5F5651EHxFC, R5F5651CDxLC, R5F5651CHxLC, R5F5651EDxLC, R5F5651EHxLC
RX66N Group (R01UH0825EJ0100)	100pin	R5F566NNDxFP, R5F566NNHxFP, R5F566NDDxFP, R5F566NDHxFP
	144pin	R5F566NNDxFB, R5F566NNHxFB, R5F566NDDxFB, R5F566NDHxFB
	145pin	R5F566NNDxLK, R5F566NNHxLK, R5F566NDDxLK, R5F566NDHxLK
	176pin	R5F566NNDxFC, R5F566NNHxFC, R5F566NDDxFC, R5F566NDHxFC, R5F566NNDxBG, R5F566NNHxBG, R5F566NDDxBG, R5F566NDHxBG
	244pin	R5F566NNDxBD, R5F566NNHxBD, R5F566NDDxBD, R5F566NDHxBD

Table 2-4 Support Devices

Group (HW Manual number)	PIN	Device name
RX66T Group (R01UH0749EJ0100)	64pin	R5F566TAAxFM, R5F566TAExDFM, R5F566TEAxFM, R5F566TEExFM
	80pin	R5F566TAAxFF, R5F566TAExFF, R5F566TEAxFF, R5F566TEExFF, R5F566TAAxFN, R5F566TAExFN, R5F566TEAxFN, R5F566TEExFN
	100pin	R5F566TKCxFP, R5F566TAExFP, R5F566TFFxFP, R5F566TFCxFP, R5F566TFExFP, R5F566TFBxFP, R5F566TFAxFP, R5F566TABxFP, R5F566TAFxFP, R5F566TEFxFP, R5F566TKFxFP, R5F566TKGxFP, R5F566TKAxFP, R5F566TKExFP, R5F566TKBxFP, R5F566TEBxFP, R5F566TEExFP, R5F566TEAxFP, R5F566TAAxFP, R5F566TFGxFP
	112pin	R5F566TAAxFH, R5F566TAExFH, R5F566TEExFH, R5F566TEAxFH
	144pin	R5F566TKCxFB, R5F566TFGxFB, R5F566TFCxFB, R5F566TKGxFB
RX71M Group (R01UH0493EJ0110)	100pin	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145pin	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLK, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177pin	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG
RX72M Group (R01UH0804EJ0100)	176pin	R5F572MNHxFC, R5F572MDDxBG, R5F572MNDxFC, R5F572MDHxBG, R5F572MDDxFC, R5F572MNHxBG, R5F572MNDxBG, R5F572MDHxFC
	224pin	R5F572MDDxBD, R5F572MDHxBD, R5F572MNHxBD, R5F572MNDxBD
RX72N Group (R01UH0824EJ0100)	100pin	R5F572NNDxFP, R5F572NNHxFP, R5F572NDDxFP, R5F572NDHxFP
	144pin	R5F572NNDxFB, R5F572NNHxFB, R5F572NDDxFB, R5F572NDHxFB
	145pin	R5F572NNDxLK, R5F572NNHxLK, R5F572NDDxLK, R5F572NDHxLK
	176pin	R5F572NNDxFC, R5F572NNHxFC, R5F572NDDxFC, R5F572NDHxFC, R5F572NNDxBG, R5F572NNHxBG, R5F572NDDxBG, R5F572NDHxBG
	224pin	R5F572NNDxBD, R5F572NNHxBD, R5F572NDDxBD, R5F572NDHxBD

Table 2-5 Support Devices

Group (HW Manual number)	PIN	Device name
RX72T Group (R01UH0803EJ0100)	100pin	R5F572TKExFP, R5F572TFFxFP, R5F572TKFxFP, R5F572TFGxFP, R5F572TKCxFP, R5F572TFBxFP, R5F572TFExFP, R5F572TFCxFP, R5F572TFAxFP, R5F572TKAxFP, R5F572TKBxFP, R5F572TKGxFP
	144pin	R5F572TKGxFB, R5F572TKCxFB, R5F572TFGxFB, R5F572TFCxFB

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RX V2.7.0.

Table 2-6 Support Components (RX100, RX200 family) **○: Support, /: Non-support**

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	8-Bit Timer	-	/	/	○	○	/	○	○	○	○	○	
2	CRC Calculator	-	○	○	○	○	○	○	○	○	○	○	
3	D/A Converter	-	/	○	○	○	○	○	/	○	○	○	
4	DMA Controller	-	/	/	/	/	/	○	○	/	○	/	
5	I2C Slave Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	
6	I2C Master Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	
7	LCD Controller		/	/	○	/	/	/	/	/	/	/	
8	PWM Mode Timer	PWM mode 1	○	○	○	○	○	○	○	○	○	○	
		PWM mode 2	○	○	○	○	○	○	○	○	○	○	
9	SCI/SCIF Clock Synchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	Note 1, 2
		Reception	○	○	○	○	○	○	○	○	○	○	Note 1, 2
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	Note 1, 2
10	SCI/SCIF Asynchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	Note 1
		Reception	○	○	○	○	○	○	○	○	○	○	Note 1
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Transmission	○	○	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Reception	○	○	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Transmission/Reception	○	○	○	○	○	○	○	○	○	○	Note 1
11	SPI Clock Synchronous Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	
12	SPI Operation Mode	Slave transmit/receive	○	○	○	○	/	○	○	○	○	○	
		Slave transmit only	○	○	○	○	/	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	/	○	○	○	○	○	
		Master transmit only	○	○	○	○	/	○	○	○	○	○	
		Multi-master transmit/receive	○	○	○	○	/	○	○	○	○	○	
		Multi-master transmit only	○	○	○	○	/	○	○	○	○	○	
13	Event Link Controller	-	/	○	○	○	/	○	○	/	○	/	
14	Watchdog Timer	-	○	○	○	○	/	○	○	○	○	○	
15	Clock Frequency Accuracy Measurement Circuit	-	○	○	○	○	○	○	○	○	○	○	

Note 1. Refer to No 2, 3 in Table 6-2
Note 2. Refer to No 4 in Table 6-2

Table 2-7 Support Components (RX100, RX200 family) **○: Support, /: Non-support**

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
16	Group Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	
17	Comparator	-	/	/	○	○	○	○	/	/	○	/	
18	Compare Match Timer	-	○	○	○	○	○	○	○	○	○	○	
19	Single Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	
20	Smart Card Interface Mode	Transmission	○	○	○	○	○	○	○	○	○	○	
		Reception	○	○	○	○	○	○	○	○	○	○	
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	
21	Dead-time Compensation Counter	-	○	○	○	○	○	○	○	○	/	○	
22	Data Transfer Controller	-	○	○	○	○	○	○	○	○	○	○	Note 3
23	Data Operation Circuit	-	○	○	○	○	○	○	○	○	○	○	
24	Normal Mode Timer		○	○	○	○	○	○	○	○	○	○	
25	Buses	-	○	○	○	○	○	○	○	○	○	○	
26	Programmable Pulse Generator	-	/	/	/	/	/	/	/	/	/	/	
27	Ports	-	○	○	○	○	○	○	○	○	○	○	
28	Port Output Enable	-	/	○	○	○	○	○	○	○	○	○	
29	Real Time Clock	Binary	○	○	○	○	/	○	/	/	○	/	
		Calendar	○	○	○	○	/	○	/	/	○	/	
30	Remote Control Signal Receiver	-	/	/	/	○	/	/	/	/	/	/	
31	Low-Power Timer	-	/	/	○	○	/	○	○	/	○	/	
32	Phase Counting Mode Timer	-	○	○	○	○	○	○	○	○	○	○	
33	Interrupt Controller	-	○	○	○	○	○	○	○	○	○	○	
34	General PWM Timer	Saw-wave PWM mode	/	/	/	/	/	/	/	○	/	○	Note 4
		Saw-wave one-shot pulse mode	/	/	/	/	/	/	/	○	/	○	Note 4
		Triangle-wave PWM mode 1	/	/	/	/	/	/	/	○	/	○	Note 4
		Triangle-wave PWM mode 2	/	/	/	/	/	/	/	○	/	○	Note 4
		Triangle-wave PWM mode 3	/	/	/	/	/	/	/	○	/	○	Note 4
35	Low Power Consumption	-	○	○	○	○	○	○	○	○	○	○	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	/	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 2	/	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 3	/	○	○	○	○	○	○	○	○	○	
37	Continuous Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	

Note 3. Refer to No 8 in Table 6-1
Note 4. Refer to No 1 in Table 6-1

Table 2-8 Support Components (RX100, RX200 family) **○: Support, /: Non-support**

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
38	Voltage Detection Circuit	-	○	○	○	○	○	○	○	○	○	○	
39	Delta-Sigma Modulator Interface	Master	/	/	/	/	/	/	/	/	/	/	
		Slave	/	/	/	/	/	/	/	/	/	/	
40	Single Scan Mode DSAD	-	/	/	/	/	/	/	○	/	/	/	
41	Continuous Scan Mode DSAD	-	/	/	/	/	/	/	○	/	/	/	
42	Analog Front End	-	/	/	/	/	/	/	○	/	/	/	
43	Motor	3-Phase Brushless DC Motor	/	/	/	/	○	/	/	○	/	○	
		2-Phase Stepping Motor (Fast Decay)	/	/	/	/	○	/	/	○	/	○	
		2-Phase Stepping Motor (Slow Decay)	/	/	/	/	○	/	/	○	/	○	

Table 2-9 Support Components (RX600, RX700 family) ○: Support, /: Non-support

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
1	8-Bit Timer	-	○	○	○	○	○	○	○	○	
2	CRC Calculator	-	○	○	○	○	○	○	○	○	
3	D/A Converter	-	○	○	○	○	○	○	○	○	
4	DMA Controller	-	○	○	○	○	○	○	○	○	
5	I2C Slave Mode	I2C mode	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	
6	I2C Master Mode	I2C mode	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	
7	LCD Controller		/	/	/	/	/	/	/	/	
8	PWM Mode Timer	PWM mode 1	○	○	○	○	○	○	○	○	
		PWM mode 2	○	○	○	○	○	○	○	○	
9	SCI/SCIF Clock Synchronous Mode	Transmission	○	○	○	○	○	○	○	○	Note 1, 2
		Reception	○	○	○	○	○	○	○	○	Note 1, 2
		Transmission/Reception	○	○	○	○	○	○	○	○	Note 1, 2
10	SCI/SCIF Asynchronous Mode	Transmission	○	○	○	○	○	○	○	○	Note 1
		Reception	○	○	○	○	○	○	○	○	Note 1
		Transmission/Reception	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Transmission	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Reception	○	○	○	○	○	○	○	○	Note 1
		Multi-processor Transmission/Reception	○	○	○	○	○	○	○	○	Note 1
11	SPI Clock Synchronous Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	
12	SPI Operation Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	
		Multi-master transmit/receive	○	○	○	○	○	○	○	○	
		Multi-master transmit only	○	○	○	○	○	○	○	○	
13	Event Link Controller	-	○	○	○	○	○	○	○	○	
14	Watchdog Timer	-	○	○	○	○	○	○	○	○	
15	Clock Frequency Accuracy Measurement Circuit	-	○	○	○	○	○	○	○	○	

Note 1. Refer to No 2, 3 in Table 6-2
Note 2. Refer to No 4 in Table 6-2

Table 2-10 Support Components (RX600, RX700 family) **○: Support, /: Non-support**

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
16	Group Scan Mode S12AD	-	○	○	○	○	○	○	○	○	
17	Comparator	-	/	/	/	○	/	○	/	○	
18	Compare Match Timer	-	○	○	○	○	○	○	○	○	
19	Single Scan Mode S12AD	-	○	○	○	○	○	○	○	○	
20	Smart Card Interface Mode	Transmission	○	○	○	○	○	○	○	○	
		Reception	○	○	○	○	○	○	○	○	
		Transmission/Reception	○	○	○	○	○	○	○	○	
21	Dead-time Compensation Counter	-	○	○	○	○	○	○	○	○	
22	Data Transfer Controller	-	○	○	○	○	○	○	○	○	Note 3
23	Data Operation Circuit	-	○	○	○	○	○	○	○	○	
24	Normal Mode Timer		○	○	○	○	○	○	○	○	
25	Buses	-	○	○	○	○	○	○	○	○	
26	Programmable Pulse Generator	-	○	○	○	/	○	/	○	/	
27	Ports	-	○	○	○	○	○	○	○	○	
28	Port Output Enable	-	○	○	○	○	○	○	○	○	
29	Real Time Clock	Binary	○	○	○	/	○	/	○	/	
		Calendar	○	○	○	/	○	/	○	/	
30	Remote Control Signal Receiver	-	/	/	/	/	/	/	/	/	
31	Low-Power Timer	-	/	/	/	/	/	/	/	/	
32	Phase Counting Mode Timer	-	○	○	○	○	○	○	○	○	
33	Interrupt Controller	-	○	○	○	○	○	○	○	○	
34	General PWM Timer	Saw-wave PWM mode	○	/	○	○	○	○	○	○	Note 4
		Saw-wave one-shot pulse mode	○	/	○	○	○	○	○	○	Note 4
		Triangle-wave PWM mode 1	○	/	○	○	○	○	○	○	Note 4
		Triangle-wave PWM mode 2	○	/	○	○	○	○	○	○	Note 4
		Triangle-wave PWM mode 3	○	/	○	○	○	○	○	○	Note 4
35	Low Power Consumption	-	○	○	○	○	○	○	○	○	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	○	○	○	○	○	○	○	○	
		Complementary PWM mode 2	○	○	○	○	○	○	○	○	
		Complementary PWM mode 3	○	○	○	○	○	○	○	○	
37	Continuous Scan Mode S12AD	-	○	○	○	○	○	○		○	

Note 3. Refer to No 8 in Table 6-1
Note 4. Refer to No 1 in Table 6-1

Table 2-11 Support Components (RX600, RX700 family) **○: Support, /: Non-support**

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
38	Voltage Detection Circuit	-	○	○	○	○	○	○	○	○	
39	Delta-Sigma Modulator Interface	Master	/	/	/	/	/	○	/	/	
		Slave	/	/	/	/	/	○	/	/	
40	Single Scan Mode DSAD	-	/	/	/	/	/	/	/	/	
41	Continuous Scan Mode DSAD	-	/	/	/	/	/	/	/	/	
42	Analog Front End	-	/	/	/	/	/	/	/	/	
43	Motor	3-Phase Brushless DC Motor	/	/	/	○	/	○	/	○	
		2-Phase Stepping Motor (Fast Decay)	/	/	/	○	/	○	/	○	
		2-Phase Stepping Motor (Slow Decay)	/	/	/	○	/	○	/	○	

2.3 New support

2.3.1 New device support

From Smart Configurator for RX V2.7.0, new device packages as below are supported.

- R5F513T3AxNE
- R5F513T5AxNE
- R5F513T3AxNH
- R5F513T5AxNH
- R5F523W8CxLN
- R5F523W8DxLN
- R5F523E5SxFL
- R5F523E6SxFL
- R5F523E5SxNF
- R5F523E6SxNF

2.3.2 The functions (e.g. work mode) selected in the 'New component' wizard page can be displayed after creating configuration

From Smart Configurator for RX V2.7.0, the functions (e.g. work mode, resource) selected in the 'New component' wizard can be displayed after creating configuration, the information will be shown when mouse hovers on the information icon located on the top-right corner of configuration area, meanwhile from this version, component name can be printed into the Smart Configurator report (configuration section).

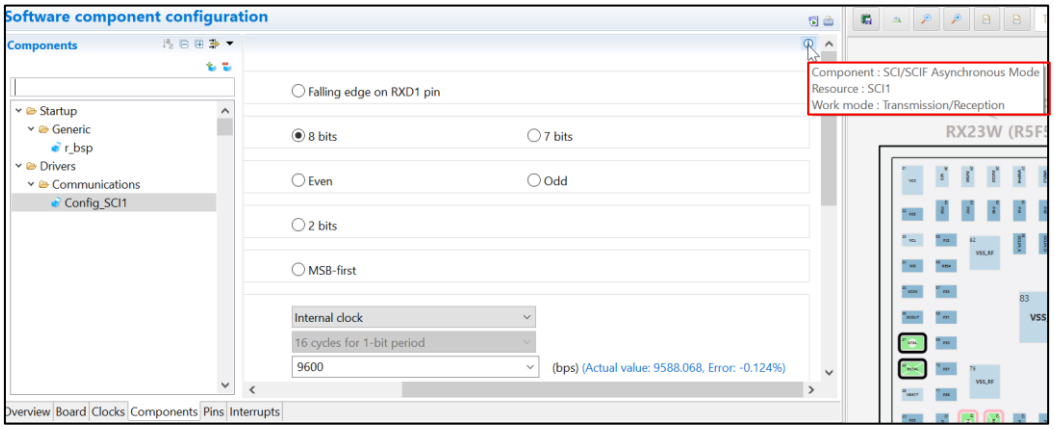
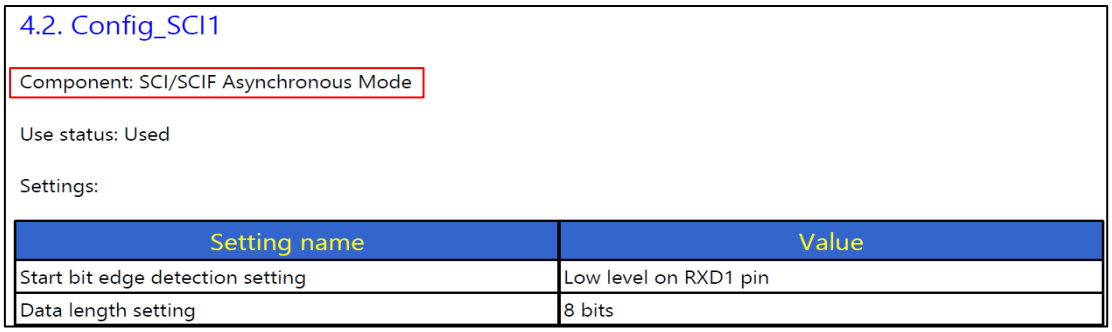


Figure 2-1: Information icon tip displays the function selected in the 'New component' wizard



4.2. Config_SCI1

Component: SCI/SCIF Asynchronous Mode

Use status: Used

Settings:

Setting name	Value
Start bit edge detection setting	Low level on RXD1 pin
Data length setting	8 bits

Figure 2-2: Component name is printed out in the report

2.3.3 Peripheral information can be displayed via tool tips for each output clock on the clock page

From Smart Configurator for RX V2.7.0, the peripheral information related to each output clock on the clock page can be displayed via tool tips when mouse hovers on the output clock textbox.

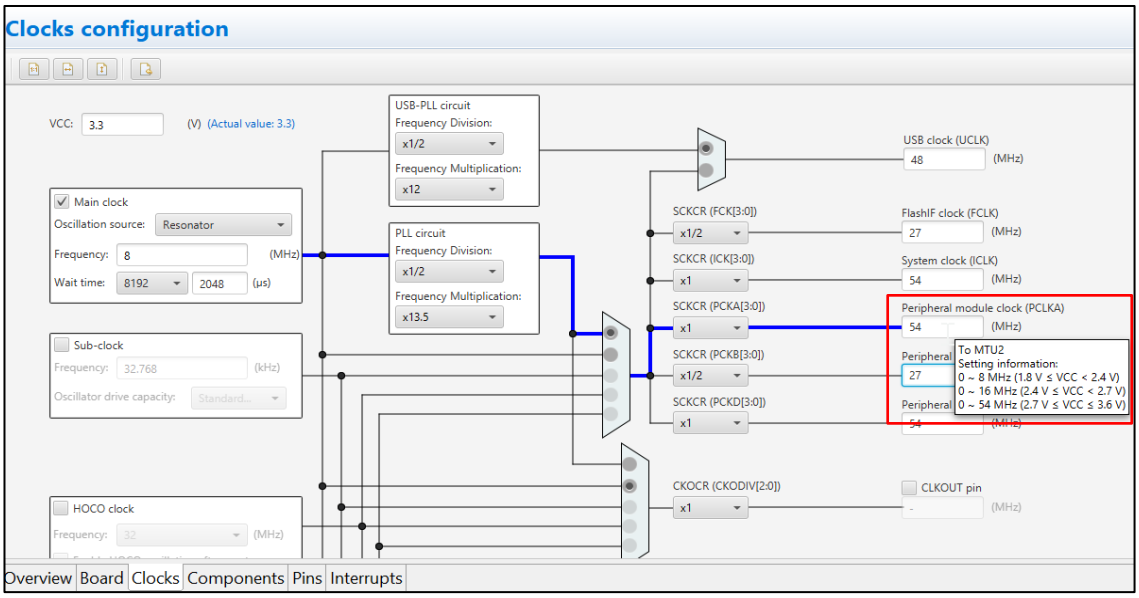


Figure 2-3: Peripheral information that was displayed with tool tips for PCLKA on RX23W

2.3.4 New send/receive APIs have been added for 8-bits and 16-bits buffer access width respectively in the SPI components

From Smart Configurator for RX V2.7.0, two new send/receive APIs will be generated out for 8-bits and 16-bits buffer access width respectively in the SPI synchronous mode component and SPI operation mode component as below:

- Buffer access width: 8bits

  *MD_STATUS R_<Config_RSPI0>_Send_Receive (uint8_t * const tx_buf, uint16_t tx_num, uint8_t * const rx_buf)*

- Buffer access width:16bits

  *MD_STATUS R_<Config_RSPI0>_Send_Receive (uint16_t * const tx_buf, uint16_t tx_num, uint16_t * const rx_buf)*

2.3.5 A "Download additional boards..." link is added to the Project Generator to allow the downloading of supported board information for Smart Configurator

From Smart Configurator for RX V2.7.0, A "Download additional boards..." link is added to the e² studio Project Generator to allow the downloading of supported board information for Smart Configurator.

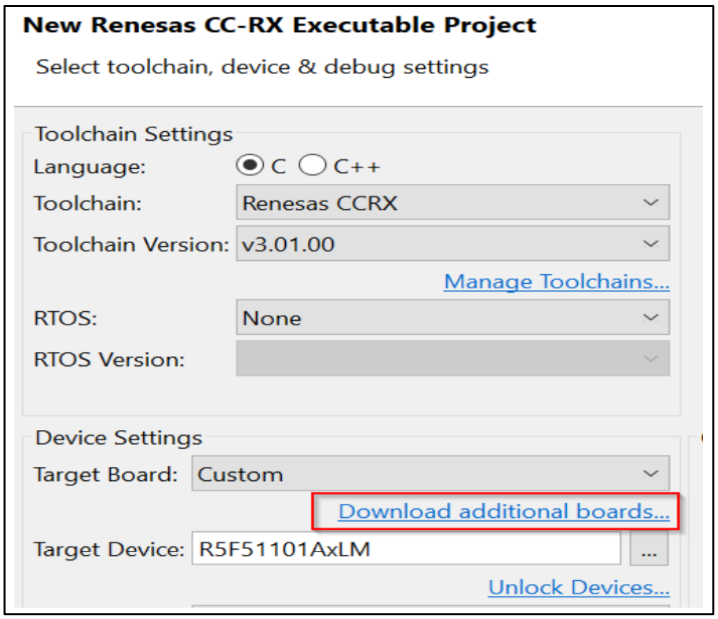


Figure 2-4: "Download additional boards..." link on the e² studio Project Generator

2.3.6 Motor driver component support

From Smart Configurator for RX V2.7.0, A “Motor” driver component has been supported for RX13T, RX23T, RX24T, RX24U, RX66T, RX72T and RX72M devices, user can add this component from the “New component” dialog (**Figure 2-5**).

This new driver component is designed for making configurations with MTU and S12AD peripherals, then generates corresponding driver codes for controlling the basic motor functionalities.

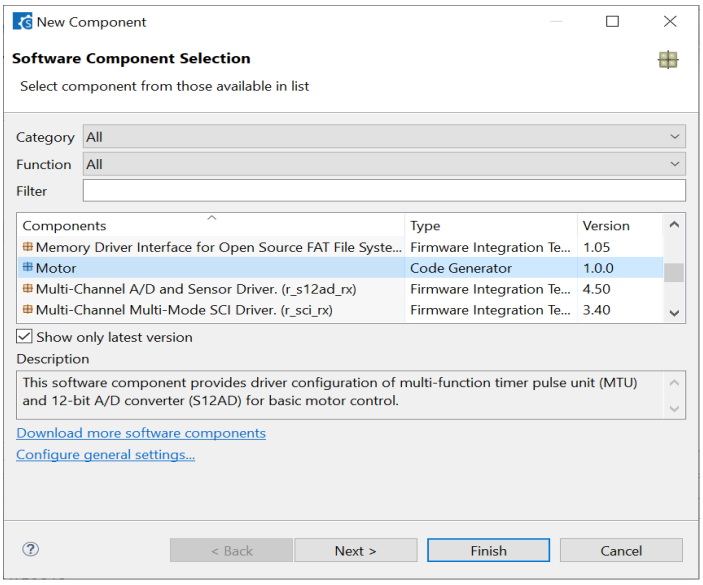


Figure 2-5: Adding Motor driver component from the “New Component” dialog

3. Changes

This chapter describes changes to the Smart Configurator for RX V2.7.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations (RX100, RX200 Family) ○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Fixed the GUI blank issue for MTU channel 1 and MTU channel 2 in PWM Mode component	/	/	/	/	○	/	/	/	/	○	
2	Fixed the generated codes issue for MTU7 interrupt enabling and priority level setting in Complementary PWM Mode component	/	/	/	/	/	/	/	/	/	○	
3	Fixed the main clock oscillator frequency issue when oscillating USB-Dedicated PLL at 48 MHz and the PLL at 54 MHz	/	/	/	/	/	○	/	/	○	/	
4	Fixed the pin assignments issue when multiple FIT components are added simultaneously	○	○	○	○	○	○	○	○	○	○	
5	Fixed the checking condition issue for 'MD_ERROR3' return error in master receive API of I2C master component and supported the 10 bits format slave address in master receive mode	○	○	○	○	○	○	○	○	○	○	
6	Fixed the PLL clock source issue when USB clock is used on the clock page	/	/	/	/	/	/	/	/	/	/	
7	Fixed the issue that external bus clock (BCLK) can be configurable on the clock page	/	/	/	/	/	○	/	/	/	/	
8	Fixed the error icon display issue on the USB-PLL circuit of clock page	/	/	/	/	/	○	/	/	/	/	
9	Fixed the issue that HOCO oscillation enable setting is not configurable on the clock page	○	○	○	○	○	○	○	○	○	○	
10	Fixed the CLKOUT25M pin error message issue on the pin page	/	/	/	/	/	/	/	/	/	/	
11	Fixed an issue that "DCLIN_A" and "DCLIN_D" pins cannot be assigned from the MCU package view when selected from the context menu	/	/	/	/	/	/	/	/	○	/	
12	Fixed the inaccurate waiting time issue for HOCO clock power supply stabilization	/	/	/	/	/	/	/	/	/	/	
13	Fixed the pin assignment issue for PGAVSS0 and PGAVSS1 pin functions in the S12AD Single Scan Mode and Continuous Scan Mode components	/	/	/	/	/	/	/	/	/	○	RX24U only
14	Fixed an unexpected pin error issue when configuring the pin assignment for RXD and TXD for “r_sci_rx” FIT component	/	/	/	/	/	/	/	/	/	/	
15	Fixed the issue that "Clear pin assignments" command in the Pins page doesn't work after device change	○	○	○	○	○	○	○	○	○	○	
16	Fixed the source code files update issue on the file tree of CS+ project	○	○	○	○	○	○	○	○	○	○	

Table 3-2 List of Correction of issues/limitations (RX600, RX700 Family) ○: Applicable, /: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
1	Fixed the GUI blank issue for MTU channel 1 and MTU channel 2 in PWM Mode component	/	/	/	/	/	/	/	/	
2	Fixed the generated codes issue for MTU7 interrupt enabling and priority level setting in Complementary PWM Mode component	/	/	/	/	/	/	/	/	
3	Fixed the main clock oscillator frequency issue when oscillating USB-Dedicated PLL at 48 MHz and the PLL at 54 MHz	/	/	/	/	/	/	/	/	
4	Fixed the pin assignments issue when multiple FIT components are added simultaneously	○	○	○	○	○	○	○	○	
5	Fixed the checking condition issue for 'MD_ERROR3' return error in master receive API of I2C master component and supported the 10 bits format slave address in master receive mode	○	○	○	○	○	○	○	○	
6	Fixed the PLL clock source issue when USB clock is used on the clock page	○	○	○	○	○	○	○	○	
7	Fixed the issue that external bus clock (BCLK) can be configurable on the clock page	/	/	/	/	/	/	/	/	
8	Fixed the error icon display issue on the USB-PLL circuit of clock page	/	/	/	/	/	/	/	/	
9	Fixed the issue that HOCO oscillation enable setting is not configurable on the clock page	○	○	○	○	○	○	○	○	
10	Fixed the CLKOUT25M pin error message issue on the pin page	/	/	○	/	/	○	○	/	
11	Fixed an issue that "DCLIN_A" and "DCLIN_D" pins cannot be assigned from the MCU package view when selected from the context menu	/	/	/	/	/	/	/	/	
12	Fixed the inaccurate waiting time issue for HOCO clock power supply stabilization	○	○	/	/	○	/	/	/	
13	Fixed the pin assignment issue for PGAVSS0 and PGAVSS1 pin functions in the S12AD Single Scan Mode and Continuous Scan Mode components	/	/	/	/	/	/	/	/	
14	Fixed an unexpected pin error issue when configuring the pin assignment for RXD and TXD for “r_sci_rx” FIT component	/	○	○	/	/	○	○	/	
15	Fixed the issue that "Clear pin assignments" command in the Pins page doesn't work after device change	○	○	○	○	○	○	○	○	
16	Fixed the source code files update issue on the file tree of CS+ project	○	○	○	○	○	○	○	○	

3.1.1 Fixed the GUI blank issue for MTU channel 1 and MTU channel 2 in PWM Mode component

The When using MTU channel 1 and channel 2 with PWM Mode component, the GUI cannot be displayed (blank) in the configuration panel, this issue has been fixed from SC for RX V2.7.0

3.1.2 Fixed the generated codes issue for MTU7 interrupt enabling and priority level setting in Complementary PWM Mode component

When using MTU6 and MTU7 with Complementary PWM Mode component, the generated codes for interrupt enabling and priority level setting for MTU7 are wrong, MTU4 interrupt information are mistakenly used as parameters in the IEN and IPR macro functions, this issue has been fixed from SC for RX V2.7.0

3.1.3 Fixed the main clock oscillator frequency issue when oscillating USB-Dedicated PLL at 48 MHz and the PLL at 54 MHz

When configuring the main clock frequency on clock page, main clock oscillator frequency is not set to 4, 6, 8 or 12 MHz when oscillating USB-Dedicated PLL at 48 MHz and the PLL at 54 MHz according to UM note, this issue has been fixed from SC for RX 2.7.0

3.1.4 Fixed the pin assignments issue when multiple FIT components are added simultaneously

When a board is selected and ‘r_sci_rx’ FIT component is first added with other FIT components simultaneously, some unnecessary pin assignments will be carried out on the pin page with pin warning messages, when click ‘r_sci_rx’ configuration node on the configuration tree, these pin assignments and corresponding warning messages will disappear, this issue has been fixed from SC for RX V2.7.0

3.1.5 Fixed the checking condition issue for 'MD_ERROR3' return error in master receive API of I2C master component and supported the 10 bits format slave address in master receive mode

When using master receive mode with I2C master component, the checking condition for ‘MD_ERROR3’ is incorrect in the master receive API, it should check against ‘0x7FU’ instead of ‘0xFFU’, and 10 bits format slave address is not supported as well, this issue has been fixed and 10 bits format slave address in master receive mode has been supported from SC for RX V2.7.0

3.1.6 Fixed the PLL clock source issue when USB clock is used on the clock page

When using USB clock on the clock page, HOCO can be set as PLL clock source but it is not allowed according to the Hardware User Manual, this issue has been fixed from SC for RX V2.7.0

3.1.7 Fixed the issue that external bus clock (BCLK) can be configurable on the clock page

When creating project with 64 or 48 pins packages on RX231/0, the external bus clock GUI setting (BCLK) is still available for configuration on the clock page although external bus component (Buses) is not supported on these devices. This issue has been fixed from SC for RX V2.7.0 0

3.1.8 Fixed the error icon display issue on the USB-PLL circuit of clock page

When USB-PLL circuit is not used for USB clock (UCLK) output on the clock page, some main clock input (e.g. 14 MHz) will cause an error displayed beside the ‘Frequency Multiplication’ combo box and this error cannot be cleared, this issue has been fixed from SC for RX V2.7.0

3.1.9 Fixed the issue that HOCO oscillation enable setting is not configurable on the clock page

When configuring clock settings on clock page, the HOCO oscillation enable setting is not supported although there is a corresponding register bit (OFS1.HOCOEN) for controlling it according to Hardware User Manual, this issue has been fixed from SC for RX V2.7.0

3.1.10 Fixed the CLKOUT25M pin error message issue on the pin page

When creating a new project, CLKOUT25M pin is set to be used by default and an error message with text “component require a pin” will be shown on the pin page when uncheck this CLKOUT25M pin manually. This issue has been fixed from SC for RX V2.7.0, the CLKOUT25M pin is not used by default and clock page won't control this pin enable status anymore, this pin enable/disable will be fully controlled in r_ether_rx FIT component GUI configuration

3.1.11 Fixed an issue that "DCLIN_A" and "DCLIN_D" pins cannot be assigned from the MCU package view when selected from the context menu

When using context menu on the MCU package view to assign pins, it won't succeed for 'DCLIN_A' and 'DCLIN_D' pin functions, this issue has been fixed from SC for RX V2.7.0

3.1.12 Fixed the inaccurate waiting time issue for HOCO clock power supply stabilization

When using the HOCO clock on the clock page, the generated codes for HOCO waiting time macro (_XXXX_CGC_HOCOP_WAIT) value is inaccurate, which causes the waiting time is a bit shorter than expected, this issue has been fixed from SC for RX V2.7.0

3.1.13 Fixed the pin assignment issue for PGAVSS0 and PGAVSS1 pin functions in the S12AD Single Scan Mode and Continuous Scan Mode components

When using S12AD Single Scan Mode and Continuous Scan Mode components, pins are assigned for PGAVSS0 and PGAVSS1 pin functions immediately after creating new configurations with these two components, they should be assigned when corresponding GUI setting "Enable PXXX amplifier pass-through" checkbox is checked, this issue has been fixed from SC for RX V2.7.0

3.1.14 Fixed an unexpected pin error issue when configuring the pin assignment for RXD and TXD for “r_sci_rx” FIT component

When configuring the pin assignment for RXD and TXD for "r_sci_rx" FIT component, an unexpected pin error will be displayed for these multi-purpose pin functions as below:

- RXD and TXD: No component using this pin
- SMISO, SMOSI, SSCL and SSDA: Component requires a pin

This issue occurs on the following RX devices and channels and it has been fixed from SC for RX V2.7.0

- RX651/N: SCI channel 10 and 11
- RX66N/RX72N, RX72M: SCI channel 8, 9, 10 and 11

3.1.15 Fixed the issue that "Clear pin assignments" command in the Pins page doesn't work after device change

When using the "Clear pin assignments" context menu command in the pin number tab of Pins page, it doesn't work anymore after device change operation, this issue has been fixed from SC for RX V2.7.0

3.1.16 Fixed the source code files update issue on the file tree of CS+ project time

When using Smart Configurator standalone RCP version with CS+, user needs to click "Generate code" button two times to update the source files content on the project file tree, this issue has been fixed from SC for RX V2.7.0

3.2 Specification changes

Table 3-3 List of Specification changes (RX100, RX200 family) ○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Improved the operation selection items' descriptions for better understanding in the complementary PWM Mode timer component	○	○	○	○	○	○	○	○	○	○	
2	Changed the if-else statement to switch statement in the R_{Configuation_Name} _Get_ValueResult () API generated in the S12AD components	○	○	○	○	○	○	○	○	○	○	
3	The FIT component "r_lpc_rx", "r_sci_rx" and "r_sci_iic_rx" are removed from the block list	○	○	○	○	○	○	○	○	○	○	
4	Executable (.exe) files will no longer be duplicated into the "/trash" folder when "Generate Code" button is pressed	○	○	○	○	○	○	○	○	○	○	
5	The "Enable data reception completion interrupt" checkbox is set to unchecked as default	/	/	/	○	/	/	/	/	/	/	

Table 3-4 List of Specification changes (RX600, RX700 family) ○: Applicable, /: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
1	Improved the operation selection items' descriptions for better understanding in the complementary PWM Mode timer component	○	○	○	○	○	○	○	○	
2	Changed the if-else statement to switch statement in the R_{Configuation_Name} _Get_ValueResult () API generated in the S12AD components	○	○	○	○	○	○	○	○	
3	The FIT component "r_lpc_rx", "r_sci_rx" and "r_sci_iic_rx" are removed from the block list	○	○	○	○	○	○	○	○	
4	Executable (.exe) files will no longer be duplicated into the "/trash" folder when "Generate Code" button is pressed	○	○	○	○	○	○	○	○	
5	The "Enable data reception completion interrupt" checkbox is set to unchecked as default	/	/	/	/	/	/	/	/	

3.2.1 Improved the operation selection items' descriptions for better understanding in the Complementary PWM Mode Timer component

The operation selection items' descriptions for the Complementary PWM Mode Timer component have been improved for better understanding.

- 'Complementary PWM mode 1' is changed to 'Complementary PWM mode 1 (Transfer at crest)'
- 'Complementary PWM mode 2' is changed to 'Complementary PWM mode 1 (Transfer at trough)'
- 'Complementary PWM mode 3' is changed to 'Complementary PWM mode 1 (Transfer at crest and trough)'

3.2.2 Changed the if-else statement to switch statement in the R_{Configuation_Name}_Get_ValueResult () API generated in the S12AD components

In the S12AD component (Single Scan Mode DSAD and Continuous Scan Mode DSAD), the if-else statement has been changed to switch statement in the generated R_{Configuation_Name}_Get_ValueResult () API to improve execution efficiency.

3.2.3 The FIT component "r_lpc_rx", "r_sci_rx" and "r_sci_iic_rx" are removed from the block list.

The FIT modules "r_lpc_rx", "r_sci_rx" and "r_sci_iic_rx" are removed from the FIT component block list, now they are always displayed in component list regardless the block list active status in the preference page.

3.2.4 The executable (.exe) files will no longer be duplicated into the "/trash" folder when "Generate Code" button is pressed

The executable (.exe) files under Smart Configurator generated codes folder will no longer be duplicated into "/trash" folder when "Generate Code" button is pressed.

3.2.5 The "Enable data reception completion interrupt" checkbox is set to unchecked as default

The "Enable data reception completion interrupt" checkbox is set to unchecked after adding new Remote-Control Signal Receiver component or click "Reset to default" from configuration context menu.

4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Sep. 1, 2017	R20TS0198	1. When using the I2C bus interface in slave mode https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0198	RX130, RX64M, RX651, RX65N	V1.3.0
Apr. 1, 2018	R20TS0294	1. When using the bus for peripheral functions https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0294	RX230, RX231	V1.4.0
Oct. 01, 2018	R20TS0351	1. Setting TPU0 channel of PWM Mode Timer https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0351	RX65N, RX651, RX64M	V1.5.0
Feb.01, 2019	R20TS0401	1. Point for caution when using the GTIOCnm pin (n = 0 to 9, m = A, B) of the general PWM timer (GPTW) as a hardware source https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0401	RX66T	V2.1.0
Apr.16, 2019	R20TS0425	1. When using the I2C bus interface in master mode https://www.renesas.com/search/keyword-search.html#q=R20TS0425	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX71M	V2.2.0
Jun.01, 2019	R20TS0434	1. When using self-diagnosis function of 12-bit A/D converter in Single Scan Mode 2. When using Serial Peripheral Interface clock synchronous mode in slave transmit 3. When using I2C Bus Interface with Fast-mode Plus enabled https://www.renesas.com/search/keyword-search.html#q=R20TS0434	RX230, RX231, RX66T, RX72T, RX64M, RX651, RX65N, RX71M	V2.2.0
Jun.16, 2019	R20TS0436	1. When using general PWM timer https://www.renesas.com/search/keyword-search.html#q=R20TS0436	RX66T, RX72T	V2.2.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Aug.01, 2019	R20TS0466	1. When using the NACK reception transfer suspension function on the I²C bus interface https://www.renesas.com/search/keyword-search.html#q=R20TS0466	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX66T, RX71M, RX72M, RX72T	V2.3.0
Sep.17, 2019	R20TS0477	1. When Using the Automatic Adjustment Function for Time Error Adjustment on the Realtime Clock https://www.renesas.com/search/keyword-search.html#q=R20TS0477	RX110, RX111, RX113, RX130, RX230, RX231, RX64M, RX651, RX65N	V2.4.0
Dec.16, 2019	R20TS0522	1. When using temperature sensor output or internal reference voltage for comparison function on S12AD components (Single Scan Mode, Group Scan Mode and Continuous Scan Mode) 2. When using calendar mode API to set counter value on RTC component 3. When using window B for comparison function on S12AD Continuous Scan Mode component 4. When using double trigger mode on S12AD Single Scan Mode component https://www.renesas.com/search/keyword-search.html#q=R20TS0522	RX64M, RX651, RX65N, RX66T, RX71M, RX72M, RX72T	V2.4.0
Feb. 01, 2020	R20TS0546	1. When using the PLL frequency synthesizer of the clock https://www.renesas.com/search/keyword-search.html#q=R20TS0546	RX64M, RX651, RX65N, RX66T, RX71M, RX72T	V2.5.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Mar. 16, 2020	R20TS0555	1. When using the TGIC7 and TGID7 interrupts in Normal Mode Timer or PWM Mode Timer 2. When creating a project with RX24T 64-pin FK packages 3. When using compare level of AN109 in Single Scan Mode S12AD https://www.renesas.com/search/keyword-search.html#q= R20TS0555	RX24T, RX24U, RX71M	V2.5.0
Apr.03, 2020	TN−RX*-A0222	Errata to RX72N Group User's Manual: Hardware Rev.1.00 https://www.renesas.com/search/keyword-search.html#genre=document&q=TN-RX*-A0222	RX72N	V2.5.0
May.16, 2020	R20TS0579	1. When using Stop API in Continuous Scan Mode DSAD and Single Scan Mode DSAD components https://www.renesas.com/search/keyword-search.html#q= R20TS0579	RX23E-A	V2.6.0
Jun.16, 2020	R20TS0591	1. When using Data Transfer Controller (DTC) component and making configuration for its vector base address 2. When using SCI/SCIF Asynchronous Mode component and making configuration for its bit-rate 3. When using AN007 or AN107 as analog input pins in S12AD components https://www.renesas.com/search/keyword-search.html#q= R20TS0591	RX230, RX231, RX651, RX65N, RX66T, RX72T	V2.6.0
Sep. 01, 2020	R20TS0611	When using PWM Mode component and making configuration with MTU channel 1 and 2 https://www.renesas.com/sg/en/search/keyword-search.html#q=R20TS0611	RX13T, RX23T, RX24T, RX24U	V2.7.0
Sep. 24, 2020	TN-RX*-A0235B/E	Notes on the Transmit Data Empty Interrupt When the FIFO is in Use with the Serial Communications Interface (SCI) https://www.renesas.com/sg/en/search/keyword-search.html#q=TN-RX*-A0235	RX651, RX65N, RX66N, RX66T, RX72M, RX72N, RX72T	V2.7.0
Oct. 01, 2020	R20TS0623	1. When using "r_sci_rx" component and making pin configurations for RXD and TXD 2. When using "r_sci_rx" component, duplicate SCI11 channels are displayed in the Components configuration panel https://www.renesas.com/sg/en/search/keyword-search.html#q=R20TS0623	RX651, RX65N, RX66N, RX72M, RX72N	V2.7.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RX V2.7.0. Please refer to a document of each module about a caution of a FIT module.

5.1 List of Limitation

Table 5-1 List of Limitation (RX100, RX200 family) **○: Applicable, /: Not Applicable**

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Note on folder expansion status of the configuration tree	○	○	○	○	○	○	○	○	○	○	
2	Note on general I/O port direction issue on MCU package view when using Port Component	○	○	○	○	○	○	○	○	○	○	
3	Note on external bus pin codes generation issue in the Pin.c file	/	/	/	/	/	○	/	/	/	/	
4	Note on CLKOUT pin settings on the clock page	○	○	○	○	/	○	/	/	/	/	
5	Note on Analog pins' connection tab issue of AFE configuration after performing device change operation on RX23E-A	/	/	/	/	/	/	○	/	/	/	
6	Note on ELC settings issue when performing device change operation	○	○	○	○	/	○	○	/	○	/	
7	Note on A/D conversion interrupt setting issue when using Motor component	/	/	/	○	/	/	/	○	/	○	
8	Note on peripheral resource conflict checking issue when using FIT component	○	○	○	○	○	○	○	○	○	○	
9	Note on the technical update for RX113 Hardware User Manual 1.10	/	/	○	/	/	/	/	/	/	/	
10	Note on configuration for generated files' folder location	○	○	○	○	○	○	○	○	○	○	
11	Note on the external bus pin code generation issue when using Buses component	/	/	/	/	/	○	/	/	/	/	
12	Note on counter source division macro definition for Timer components	○	○	○	○	○	○	○	○	○	○	
13	Note on the external pin codes location issue when using Interrupt Controller component	○	○	○	○	○	○	○	○	○	○	
14	Note on the generated report content issue when using Motor component	/	/	/	○	/	/	/	○	/	○	
15	Note on the Timer pulse output selection setting issue when performing resource change	/	/	/	○	/	/	/	○	/	○	
16	Note on the build issue when using Data Transfer Controller component	/	/	/	/	/	/	/	○	/	/	
17	Note on the C++ project	○	○	○	○	○	○	○	○	○	○	
18	Note on address pin when using external bus	/	/	/	/	/	○	/	/	○	/	
19	Note on generated codes issue when using Motor component	/	/	/	/	/	/	/	/	/	/	
20	Note on write protection issue for pin function control registers when using Motor component	/	/	/	○	/	/	/	○	/	○	
21	Note on pin conflict error issue when using r_sci_rx FIT component	○	○	○	○	○	○	○	○	○	○	

Table 5-2 List of Limitation (RX600, RX700 family) **○: Applicable, /: Not Applicable**

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
1	Note on folder expansion status of the configuration tree	○	○	○	○	○	○	○	○	
2	Note on the general I/O port direction issue on MCU package view when using Port Component	○	○	○	○	○	○	○	○	
3	Note on external bus pin codes generation issue in the Pin.c file	○	○	○	○	○	○	○	○	
4	Note on CLKOUT pin settings issue on the clock page	/	/	/	/	/	/	/	/	
5	Note on Analog pins' connection tab issue of AFE configuration after performing device change operation on RX23E-A	/	/	/	/	/	/	/	/	
6	Note on ELC settings issue when performing device change operation	○	○	○	○	○	○	○	○	
7	Note on A/D conversion interrupt setting issue when using Motor component	/	/	/	○	/	○	/	○	
8	Note on peripheral resource conflict checking issue when using FIT component	○	○	○	○	○	○	○	○	
9	Note on the technical update for RX113 Hardware User Manual 1.10	/	/	/	/	/	/	/	/	
10	Note on configuration for generated files' folder location	○	○	○	○	○	○	○	○	
11	Note on the external bus pin code generation issue when using Buses component	○	○	/	/	○	/	/	/	
12	Note on counter source division macro definition for Timer components	○	○	○	○	○	○	○	○	
13	Note on the external pin codes location issue when using Interrupt Controller component	○	○	○	○	○	○	○	○	
14	Note on the generated report content issue when using Motor component	/	/	/	○	/	○	/	○	
15	Note on the Timer pulse output selection setting issue when performing resource change	/	/	/	○	/	○	/	○	
16	Note on the build issue when using Data Transfer Controller component	/	/	○	/	/	○	○	/	
17	Note on the C++ project	○	○	○	○	○	○	○	○	
18	Note on address pin when using external bus	○	○	○	○	○	○	○	○	
19	Note on generated codes issue when using Motor component	/	/	/	○	/	/	/	○	
20	Note on write protection issue for pin function control registers when using Motor component	/	/	/	○	/	○	/	○	
21	Note on pin conflict error issue when using r_sci_rx FIT component	○	○	○	○	○	○	○	○	

5.2 Details of Limitation

5.2.1 Note on folder expansion status of the configuration tree

When there are FIT component configurations on the configuration tree of Components page, if their previous folders are expanded, then if open the "Preferences" dialog and click "Apply and Close" button, these expanded folders will collapse automatically

5.2.2 Note on the general I/O port direction issue on MCU package view when using Port Component

When adding two configurations for Port component, and set different direction for the same port pin in these two configurations, e.g. set P14 as output in 1st configuration while P14 as input in the 2nd configuration, after that remove the 2nd configuration, but now the P14 direction is marked as 'I' on the MCU package view for 1st configuration

5.2.3 Note on external bus pin codes generation issue in the Pin.c file

When using Buses component, the external bus pin codes are not generated in R_Pins_Create () API function of Pin.c file after code generation

5.2.4 Note on CLKOUT pin settings issue on the clock page

The CLKOUT pin settings are not supported on the clock page although they are configurable according to Hardware User Manual

5.2.5 Note on Analog pins' connection tab issue of AFE configuration when performing device change operation on RX23E-A

After performing device change operation within RX23E-A package devices, the valid connection between AMUX and DSAD in Analog pins' connection tab of AFE configuration will be grayed off, to avoid such issue, user needs to click the corresponding DSAD configuration node first in configuration tree after device change

5.2.6 Note on ELC settings issue when performing device change operation

When using Event Link Controller component, if the ELC linkage destination is port configuration, these port configuration destination settings will be lost after device change, user needs to click the port configuration node first in configuration tree to avoid the loss of these settings after device change

5.2.7 Note on A/D conversion interrupt setting issue when using Motor component

When using Motor component, the A/D conversion interrupt setting status doesn't reflect correctly to the Interrupt page in some cases, but generated code for A/D conversion interrupt doesn't have problem, thus please ignore the status of A/D Conversion interrupt (S12ADI, S12ADI1 or S12ADI2) in the Interrupt page

5.2.8 Note on peripheral resource conflict checking issue when using FIT component

When using FIT component, the peripheral resource conflict applies to all the channels listed in the resource information of the MDF file, in fact, the conflict should only apply to the channels that are enabled via GUI configuration

5.2.9 Note on the technical update for RX113 Hardware User Manual 1.10

Technical update (TN-RX*-A0234A/E) for RX113 Hardware User Manual 1.10 is not supported and it will be supported from next release

5.2.10 Note on configuration for generated files' folder location

Currently Smart Configurator doesn't support user to specify his own folder for the generated files and the folder is fixed to 'smc_gen', this situation will be improved from the next release

5.2.11 Note on the external bus pin code generation issue when using Buses component

When using Buses component, pin codes (PMR register setting) for external bus pins are not generated out in the configuration's initialization file because default PMR register values after hardware reset are zero already, but it is suggested to generate these pin codes, and this situation will be improved from next release

5.2.12 Note on counter source division macro definition for Timer components

For all Timer components that have counter source division settings, current spec is there are no corresponding macro definitions generated in their header files (e.g. #define MTU0_PCLK_COUNTER_DIVISION 1024 in the r_cg_mtu3.h file), this situation will be improved from next release

5.2.13 Note on the external pin codes location issue when using Interrupt Controller component

When using the Interrupt Controller component, the external pin codes location generated out in the R_Config_ICU_Create () API doesn't follow the Hardware User Manual Note sequence, these codes should be moved right before the interrupt detection type setting codes, this issue will be fixed from next release

5.2.14 Note on the generated report content issue when using Motor component

When using Motor component, the generated report content of Motor configuration is incorrect. Please do not refer to the Motor configuration report content and this issue will be fixed from next release

5.2.15 Note on the Timer pulse output selection setting issue when performing resource change

When using Motor component, the settings of Timer pulse output selection will be invalid after changing the resource from MTU6-7 to MTU3-4 for brushless DC motor and stepping motor (fast decay). Please reconfigure all output phases settings manually after changing the resource and this issue will be fixed from next release

5.2.16 Note on the build issue when using Data Transfer Controller component

When using Data Transfer Controller component in e^2 studio GCC project, a build error message saying ". dtc_vector** is not within region 'RAM'" will generate in the console when building the project for devices that have 'RAM2' area. To avoid this build issue, user needs to open the linker_script.ld file and then modify the "Virtual Memory Region" value of ". dtc_vector**" section from 'RAM' to "RAM2" (**Figure 5-1**). This issue will be fixed from next release

****: The DTC activation source vector number**

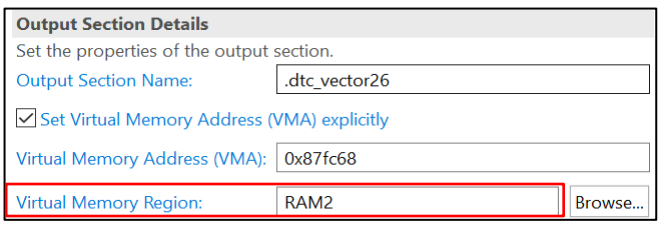


Figure 5-1 "Virtual Memory Region" value should be 'RAM2'

5.2.17 Note on the C++ project

Smart Configurator cannot be used in C++ project.
If you use Smart Configurator, please select C in language for Toolchain Settings.

5.2.18 Note on address bus when using external bus

When using Address/Data multiplexed bus in external bus, disable all unnecessary address output pin settings.

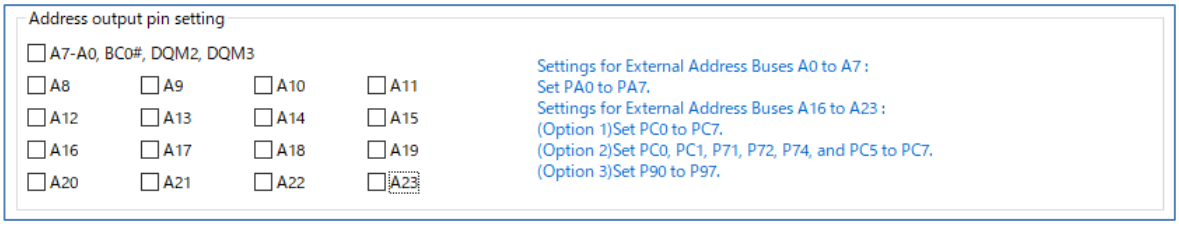


Figure 5-2 “Address output pin setting” value should be disable

5.2.19 Note on generated codes issue when using Motor component

When using Motor component in standalone RCP version or standalone RCP version with CS+, the generated codes for S12AD1.ADPGACR.BIT.PXXXDEN and S12AD1.ADPGADCR0. BIT.PXXXCR are incorrect if use ANXXX as input for AD converter (XXX = 100, 101 or 102). As a workaround, please add the following codes into the R_{Configuration Name}_Create_UserInit (void) API, e.g. AN100

```
void R_{Configuration Name}_Create_UserInit (void)
{
    /* Start user code for user init. Do not edit comment generated here */
    S12AD1.ADPGADCR0.BIT.P100DEN = 0U;
    S12AD1.ADPGACR.BIT.P100CR = 1U;
    /* End user code. Do not edit comment generated here */
}
```

5.2.20 Note on write protection issue for pin function control registers when using Motor component

When using Motor component in standalone RCP version or standalone RCP version with CS+, The write protection for pin function control registers (PmnPFS) is mistakenly enabled after initializing configuration of Motor component, therefore other component configurations’ codes for PmnPFS registers which are initialized after Motor configuration do not work. As a workaround, please add the following codes into the R_{Configuration Name}_Create_UserInit (void) API

```
void R_{Configuration Name}_Create_UserInit (void)
{
    /* Start user code for user init. Do not edit comment generated here */
    MPC.PWPR.BIT.B0WI = 0U;
    MPC.PWPR.BIT.PFSWE = 1U;
    /* End user code. Do not edit comment generated here */
}
```

5.2.21 Note on pin conflict error issue when using r_sci_rx FIT component

When using r_sci_rx FIT component, pin conflict error may be displayed after device change operation because unnecessary pin assignments are added to the SCI channels, following is one example:

1. Add r_sci_rx to an SC RX72M project
2. Select RXD10/SMISO10/SSCL10 pin and TXD10/SMOSI10/SSDA10 pin in the Components page
3. Make pin assignments for SMISO10 and SMOSI10 in the Pins page
4. In the Boards page, change device to another RX72M part number

After the device change operation, pin conflict errors are displayed because unnecessary pin assignments (RXD10 and TXD10) are added to the SCI channel, to resolve this issue, please deselect the unnecessary pin assignments from Pin page. Regarding to the above case, just deselect RXD10 and TXD10 from Pin page, then the pin conflict error will disappear automatically

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RX V2.7.0. Please refer to a document of each module about a caution of a FIT module.

6.1 List of Caution

Table 6-1 List of Caution (RX100, RX200 Family)

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Note on configuring GPT interrupt	/	/	/	/	/	/	/	/	/	○	
2	Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode	○	○	○	○	○	○	○	○	○	○	
3	Note on using only reception in SCI Clock Synchronous Mode	○	○	○	○	○	○	○	○	○	○	
4	Notes on using high transfer speed in SCIF Synchronous Mode	/	/	/	/	/	/	/	/	/	/	
5	Note on device change functionality	○	○	○	○	○	○	○	○	○	○	
6	Note on using Smart Configurator for RTOS project	/	/	/	○	/	○	/	/	/	/	Refer to FreeRTOS packages
7	Note on using Smart Configurator for GCC project in e^2 studio 7.4.0	○	○	○	○	○	○	○	○	/	○	
8	Note on using Data Transfer Controller	/	/	/	/	○	/	○	/	/	/	
9	Note on Ports setting when using S12AD components	○	/	○	○	/	/	/	/	○	/	
10	Note on section build warning when using FIT components	○	○	○	○	○	○	○	○	○	○	
11	Note on clock frequency usage	○	○	○	○	○	○	○	○	○	○	
12	Note on the BSP version update	○	○	○	○	○	○	○	○	○	○	

Table 6-2 List of Caution (RX600, RX700 Family)

○: Applicable, /: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX71M	RX72M	RX72N	RX72T	Remarks
1	Note on configuring GPT interrupt	○	/	○	○	○	○	○	○	
2	Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode	○	○	○	○	○	○	○	○	
3	Note on using only reception in SCI Clock Synchronous Mode	○	○	○	○	○	○	○	○	
4	Notes on using high transfer speed in SCIF Synchronous Mode	○	/	/	/	○	/	/	/	
5	Note on device change functionality	○	○	○	○	○	○	○	○	
6	Note on using Smart Configurator for RTOS project	○	○	○	○	○	○	○	○	Refer to FreeRTOS packages
7	Note on using Smart Configurator for GCC project in e^2 studio 7.4.0	○	○	○	○	○	/	○	○	
8	Note on using Data Transfer Controller	/	○	○	/	/	○	○	/	
9	Note on Ports setting when using S12AD components	○	○	○	/	○	○	○	/	
10	Note on section build warning when using FIT components	○	○	○	○	○	○	○	○	
11	Note on clock frequency usage	○	○	○	○	○	○	○	○	
12	Note on the BSP version update	○	○	○	○	○	○	○	○	

6.2 Details of Caution

6.2.1 Note on configuring GPT interrupts

The GPT interrupts are not specified as the Software Configurable Interrupt in the initial state even after the GPT interrupts are configured by GPT component. To specify GPT interrupts as Software Configurable Interrupt source, release unused Software Configurable interrupt source on the Interrupt sheet and allocate GPT interrupts instead.

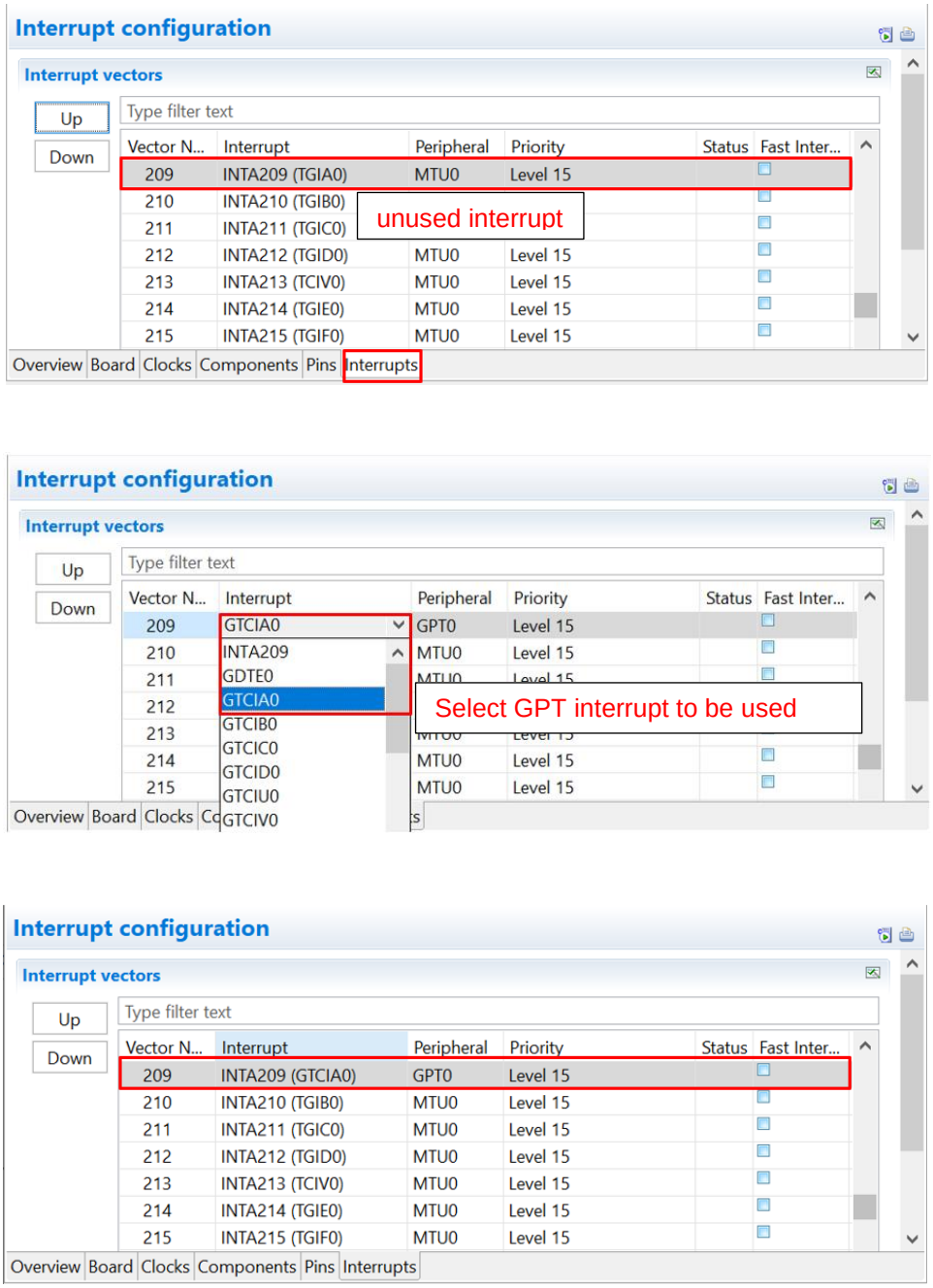


Figure 6-1 How to allocate GPT interrupt vector number

6.2.2 Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode

Sequence of setting SCR.TE bit does not follow the usage note in User's Manual: Hardware.
Instead, SCR.TE bit is set to 1 after changing the pin function to TXDn. Output of TXDn pin becomes high impedance.
Please connect a pull-up resistor to the TXDn line, prevent the TXDn line from becoming high impedance.

6.2.3 Note on using only reception in SCI Clock Synchronous Mode

In SCI Clock Synchronous Mode using internal clock, if only reception is enabled in high communication speed, extra clocks are generated even though reception has been completed.
This is due to the delay in disabling RE to stop the clock after the desired number of data is received.
To prevent this issue, select Transmission/Reception work mode when using Smart Configurator. Use "R_<Configuration Name>_Serial_Send_Receive" function instead of "R_<Configuration Name>_Serial_Receive". The same number of data for tx_num and rx_num should be specified.
Disable TXDn pin in Smart Configurator Pins page and send dummy data if transmission is not required.
There will be warnings when TXDn pin is disabled. These warnings can be ignored as TXDn pin is not intended to be used originally.

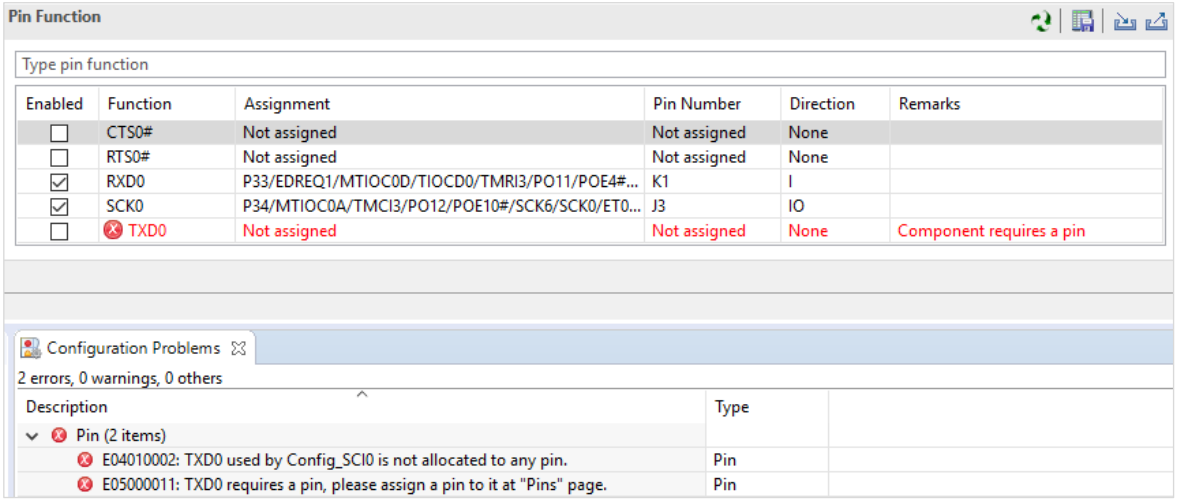


Figure 6-2 Ignore warnings when TXDn pin is disabled (Example with TXD0)

6.2.4 Note on using high transfer speed in SCIF Synchronous Mode

If the number of reception data specified for the API (R_<Configuration Name>_Serial_Receive or R_<Configuration Name>_Serial_Send_Receive) and reception FIFO threshold specified on GUI do not satisfy the formula below:

(Reception Data Size) = n * (Reception FIFO threshold) (n=1,2,3,,,,)

extra clock generation may occur after the desired number of data is received in high communication speed when using internal clock.
To prevent this issue, specify the reception data size and reception FIFO threshold that satisfy the formula.

6.2.5 Note on device change functionality

Save project settings before performing change device operation. After change device, perform these operations:

1. Visual check on Components window and Configuration Problems window. Resolve error and conflicts if there is any.
2. Check each component and converted settings.
3. Re-generate codes.

6.2.6 Note on using Smart Configurator for RTOS project

When using Smart Configurator for RTOS project, only FIT modules are supported. From Smart Configurator for RX V2.2.0, all FIT modules are displayed in "Add component" dialog by default.

6.2.7 Note on using Smart Configurator for GCC project in e^2 studio 7.4.0

When using default options to create new "GCC for Renesas RX Executable Project" with Smart Configurator in e^2 studio 7.4.0, build error occurs.

```
C:\example\src\smc_gen\r_bsp/mcu/all/r_bsp_common.h:55:24:
fatal error: stdbool.h: No such file or directory
```

As workaround, use e^2 studio 7.5.0 to create new "GCC for Renesas RX Executable Project" with Smart Configurator.

6.2.8 Note on using Data Transfer Controller

Smart Configurator does not support sequence transfer, write-back skip, write-skip disable and displacement addition features.

6.2.9 Note on Ports setting when using S12AD components

Some pins cannot be configured as output pin when S12AD components (Single Scan Mode, Continuous Scan Mode and Group Scan Mode) are used. For more information, refer to User's Manual: Hardware of the affected groups, "12-Bit A/D Converter" chapter, "Pin Setting When Using the 12-bit A/D Converter" usage note. From SC for RX 2.4.0, this note has been highlighted on the top GUI of S12AD components.

Device groups	Port pins
RX110, RX113	P40 to P44, P46
RX113	P40 to P44, P46 P90 to P92
RX130, RX23W	P40 to P47
RX64M, RX651, RX65N, RX66N, RX71M, RX72M, RX72N	P00 to P02, P03, P05, P07 P40 to P47 P90 to P93 PD0 to PD7 PE0 to PE7

6.2.10 Note on section build warning when using FIT components

When using FIT components (e.g. r_ether_rx) with section settings, these section settings will be added automatically into IDE C/C++ builder setting, but these section settings will not automatically removed from the C/C++ builder setting when these FIT components are deleted from SC, thus there are build warnings for not finding section declaration when execute build operation after these FIT components are removed, please ignore these build warnings.

6.2.11 Note on clock frequency usage

In the generated code for Smart Configurator, it is not suggested to change the clock settings codes after initialization. If clock settings/frequencies are needed to change, please change them through clock page GUI and re-generate codes after that, should not modify the generated codes related to CGC directly.

6.2.12 Note on BSP version update

When using Smart Configurator standalone RCP version with CS+ and create a project or load an existing project, BSP component will be automatically added, but if there is an information icon on the BSP configuration node of the configuration tree as below, that means there is a newer version of BSP which is available for update, please use “Change version” context menu to update it to latest version.

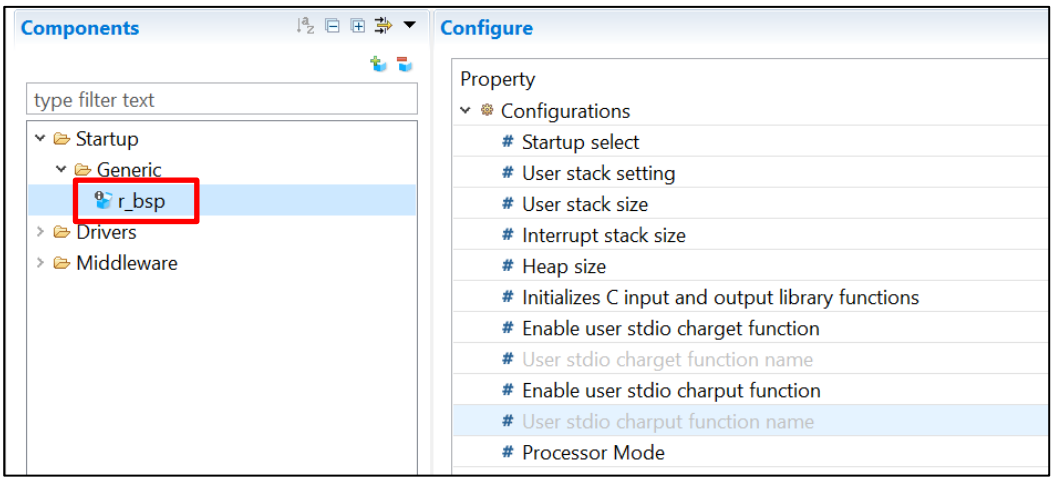


Figure 6-3 Information icon on the BSP configuration node to remind an update

Revision History

Rev.	Date	Description	
		Page	Summary
2.20	Jul.22.19	33	Create new
2.21	Oct.08.19	44	Update to Rev.2.2.1
2.30	Nov.05.19	27	Update to Rev.2.3.0
2.40	Jan.20.20	35	Update to Rev.2.4.0
2.50	Apr.20.20	42	Update to Rev.2.5.0
2.60	Jul.20.20	48	Update to Rev.2.6.0
2.70	Oct.20.20	39	Update to Rev.2.7.0
2.71	Oct.30.20	32 - 33	Add 3 limitations. ● Note on generated codes issue when using Motor component ● Note on write protection issue for pin function control registers when using Motor component ● Note on pin conflict error issue when using r_sci_rx FIT component

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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