

Thank you for using the CS+ integrated development environment.

This document describes restrictions on and points for caution regarding the simulator. Read this document before using the product.

## Contents

Chapter 1. Target Devices .....	2
Chapter 2. User's Manuals .....	3
Chapter 3. Uninstallation .....	4
Chapter 4. Changes .....	5
4.1 Improvement to differences between the target device and RH850G3KH core simulation.....	5
4.2 Removal of Restriction .....	5
Chapter 5. Points for Caution .....	6
5.1 CPU Operating Clock .....	6
5.2 Access Latency .....	6
5.3 Peripheral Functions .....	6
Chapter 6. Restriction.....	7
6.1 Simulation of the HALT Instruction.....	7

## Chapter 1. Target Devices

The simulator allows the simulation of instructions for the following RH850 CPU cores: RH850G4MH, RH850G3M, RH850G3MH, RH850G3K, and RH850G3KH.

The target devices the CS+ IDE supports are listed on the Web site.

Please see the URL below.

CS+ Product Page

<http://www.renesas.com/cs+>

## Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CS+ V8.03.00 Integrated Development Environment User's Manual: RH850 Debug Tool	R20UT4589EJ0100
CS+ V8.03.00 Integrated Development Environment User's Manual: Message	R20UT4585EJ0100

## Chapter 3. Uninstallation

There are two ways to uninstall this product.

- Use the integrated uninstaller from Renesas (uninstalls all CS+ components)
- Use the Windows uninstaller (only uninstalls this product)

To use the Windows uninstaller, select [CS+ for CC] from [Apps & features] from [Settings] of Windows or [Programs and Features] of the control panel.

## Chapter 4. Changes

This chapter describes changes from V5.00.00 to V5.01.00

### 4.1 Improvement to differences between the target device and RH850G3KH core simulation

The default value of MCTL system register in RH850G3KH core is 0x80000002, but it was 0x80000000 in the instruction simulator. It has been improved to be the same value because there was the difference with the target device.

Bit MA, which had a different value after reset, is a bit that controls misaligned access. It is 1 for the target device (Access proceeds and a misaligned access exception MAE is not generated.), and 0 (A misaligned access exception MAE is generated in response to misaligned access.) in the instruction simulator V5.00.00 or earlier. However, in the instruction simulator V5.01.00, the value after reset is same as the target device.

### 4.2 Removal of Restriction

The following restriction has been removed, and blanks are displayed when the trace data at the interrupt location cannot correctly indicate the instruction (disassembly result).

✓ Trace Data Acquired from Current Addresses when Interrupts Occurred

[Affected device] RH850G4MH

[Details] Acquired trace data may not correctly indicate the instruction (disassembled code) at an address that was current PC when an interrupt occurred. Specifically, the values of the following items may not be correct.

- The instruction (disassembled code) displayed in the [Source / Disassemble] area of the Trace panel
  - The member variable Mnemonic of class TraceInfo, an object of which is acquired by executing the debugger.Trace.Get or debugger.XTrace.Dump function in the Python console
- Note, however, that this phenomenon does not affect the normal execution of programs.

## Chapter 5. Points for Caution

This chapter describes points you will need to note when you are using the instruction simulator for RH850.

For details, refer to section 2.3.3, [Simulator], in the CS+ V8.03.00 Integrated Development Environment User's Manual: RH850 Debug Tool.

### 5.1 CPU Operating Clock

The CPU clock operates at the frequency set up with the property "Main clock frequency [MHz]" of the RH850 simulator.

### 5.2 Access Latency

Since the latency of access to the various types of memory and peripheral modules is not considered, the execution times (numbers of cycles) will be different from those for the actual device.

Thus, the results of measuring the following items differ according to whether the instruction simulator or an actual device is in use.

- The results of measurement by the Run-Break timer
- The results of measurement of Timer Result events
- The [Pipeline] area of the Trace panel
- The [Time] area of the Trace panel
- Result of tracing when the trace target is selected as [All core] (timing between processor elements)
- Timestamps of the software trace data

### 5.3 Peripheral Functions

The instruction simulator for RH850 does not support simulation of the peripheral functions.

## Chapter 6. Restriction

This chapter describes restriction on the use of the instruction simulator for RH850.

### 6.1 Simulation of the HALT Instruction

[Affected device] RH850G4MH

[Details] Execution of the HALT instruction is not reflected in the results of tracing. However, the results of tracing in the processor elements for which the HALT instruction was not executed are not affected.

[Workaround] There is no workaround.

[Schedule for fixing the problem] We will fix this problem in the next and subsequent versions.

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(Rev.4.0-1 November 2017)

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