ISL71610x

Total Dose Test Report

Introduction

This report documents the results of Low Dose Rate (LDR) total dose testing and subsequent high temperature biased annealing of the ISL71610SLHM and ISL71610M passive-input digital signal isolator with a CMOS output. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias or anneal sensitivity. Parts were irradiated biased and unbiased at LDR (0.01rad(Si)/s). The ISL71610SLHM is rated to 75krad(Si) at LDR and the ISL71610M is rated at 30krad(Si) at LDR.

Related Literature

For a full list of related documents, visit our website:

- ISL71610M device page
- ISL71610SLHM device page

Product Description

The ISL71610x is a passive-input digital signal isolator with a CMOS output. It has a similar interface as traditional optocouplers but has better performance and higher package density.

The ISL71610x is manufactured with Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. A ceramic/polymer composite barrier provides excellent isolation and an unlimited barrier life. A series external resistor sets the input coil current and a capacitor in parallel with the current-limiting resistor provides improved dynamic performance. This versatile component can be used to replace a variety of optocouplers, function over a wide range of data rates, edge speeds, and power supply levels. The device output is compatible with 3.3V and 5V supplies, allowing an interface to the controller without additional level shifting. With the coil energized with a minimum of ±8mA (bidirectional current), the ISL71610x is suitable for single-ended and differential drive applications.

The ISL71610x is offered in an 8 Ld 5mmx4mm NSOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C.

The pinout for the ISL71610x is shown in Figure 1 with the pin descriptions shown in Table 1.

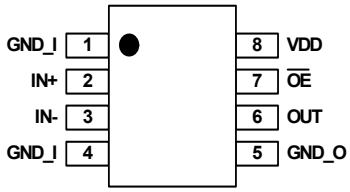

Figure 1. ISL71610x Package and Pin Configuration

Table 1. ISL71610x Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 4	GND_I	N/A	No internal connection. Use for input shielding, connect to input side ground
2	IN+	N/A	Coil connection. The voltage applied to IN+ is more negative than IN- to cause the voltage of OUT to switch to V_{OL} (logic low).
3	IN-	N/A	Coil connection. The voltage applied to IN- is more positive than IN+ to cause the voltage of OUT to switch to V_{OL} (logic low).
5	GND_O	N/A	Ground return for VDD
6	OUT	2	Data output. The OUT pin logic high is the zero input current state.

Table 1. ISL71610x Pin Descriptions (Continued)

Pin Number	Pin Name	ESD Circuit	Description
7	$\overline{OE}$	1	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD	N/A	Receiver supply voltage

1. Test Description

1.1 Irradiation Facilities

The irradiation was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic commercial irradiator. This irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation, at 100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configurations used for biased irradiation.

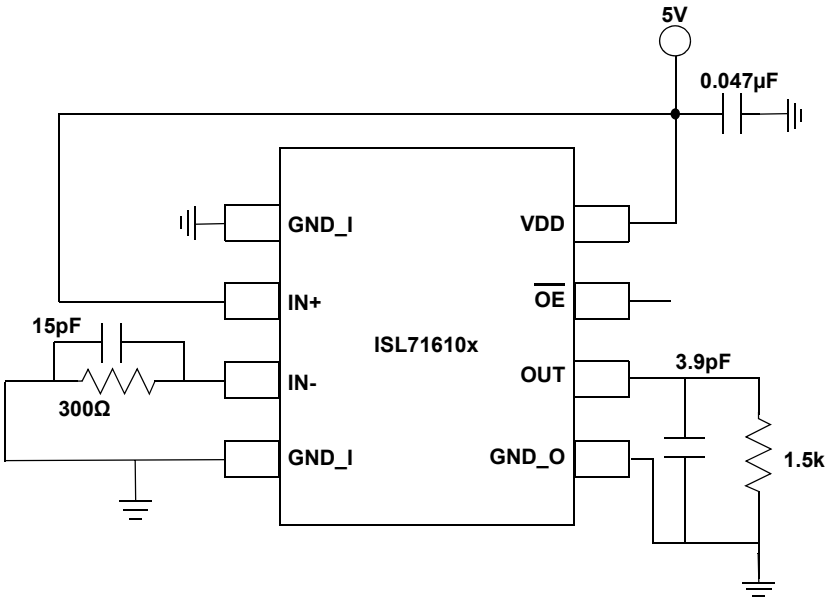

Figure 2. ISL71610x TID Bias Schematic (V_{DD} = 5.5V)

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with data logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed following the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 24 samples irradiated under bias and 24 samples irradiated with all pins grounded, bias. At anneal all samples were biased.

The ISL71610x samples were drawn from wafer lot 194606. All samples were packaged in the standard 8 Ld SOIC. Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the tests were 0, 10, 30, 50, 75, and 100krad(Si), followed by a 168 hour high temperature anneal at 100°C under bias, as described in Experimental Matrix.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL71610x is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

Table 2. ISL71610x Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass (Note 1)	Fail
0.01	Biased (Figure 2)	24	Pre-irradiation	24	
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	24	0
0.01	GND	24	Pre-irradiation	24	
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	24	0

Note:
1. A pass indicates a sample that passes all post-irradiation datasheet limits.

2.2 Key Parameter Variables Data

The plots in Figure 3 through Figure 19 show the TID response of selected parameters as shown in Table 3 in the Appendix. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and grounded, and Post Anneal (PA). The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples. However, in some plots, the error bars are not visible because of their values compared to the scale of the graph.

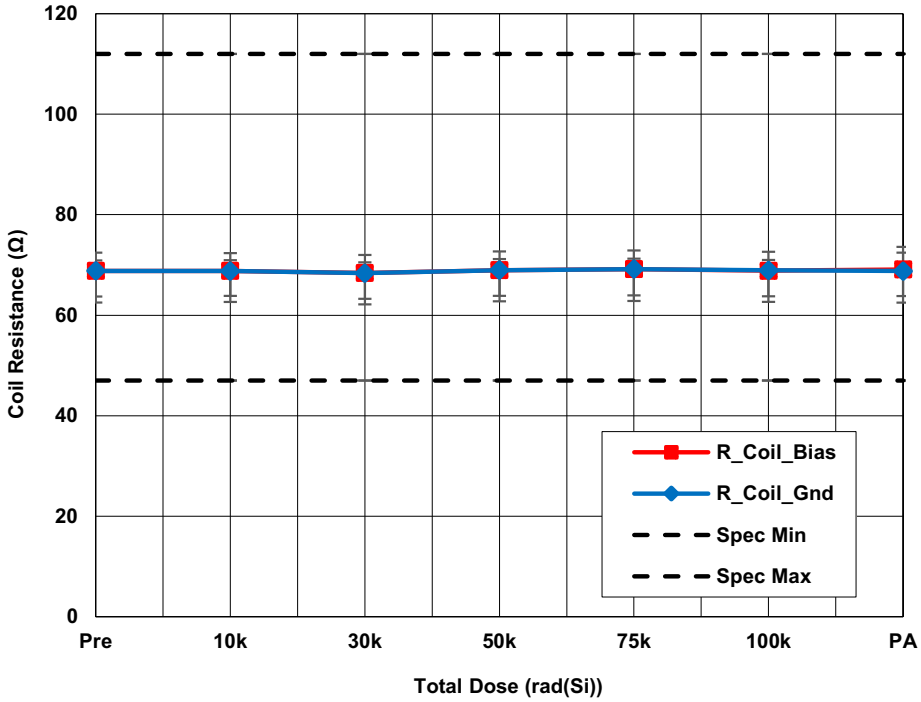

Figure 3. ISL71610x average coil resistance (R_{COIL}) as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 47Ω minimum and 112Ω maximum.

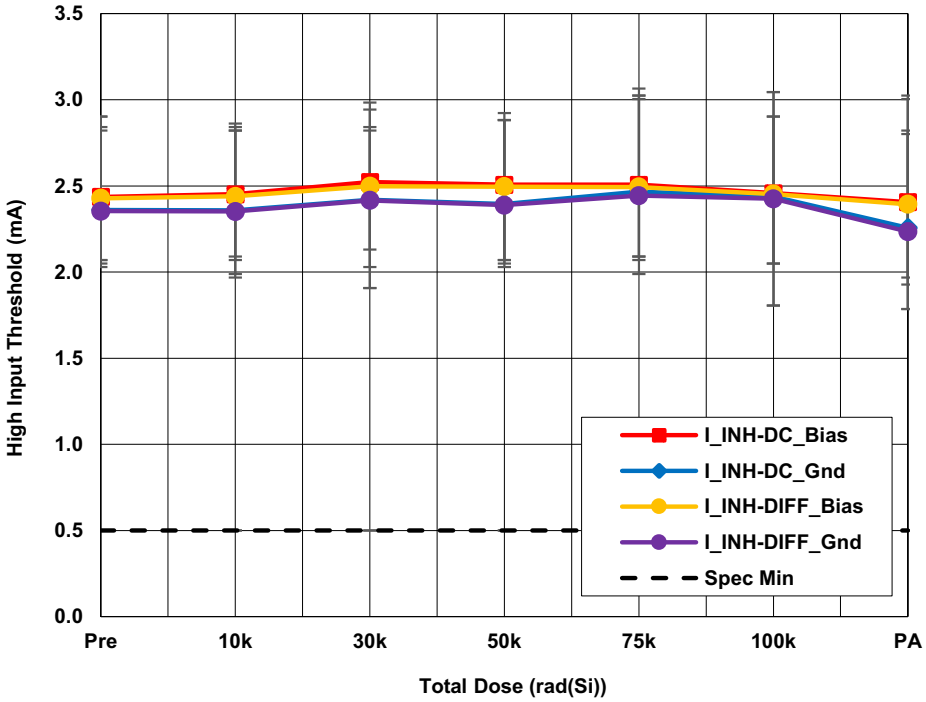

Figure 4. ISL71610x average high input threshold, DC single-ended (I_{INH-DC}) and differential ($I_{INH-DIFF}$) as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 0.5mA minimum.

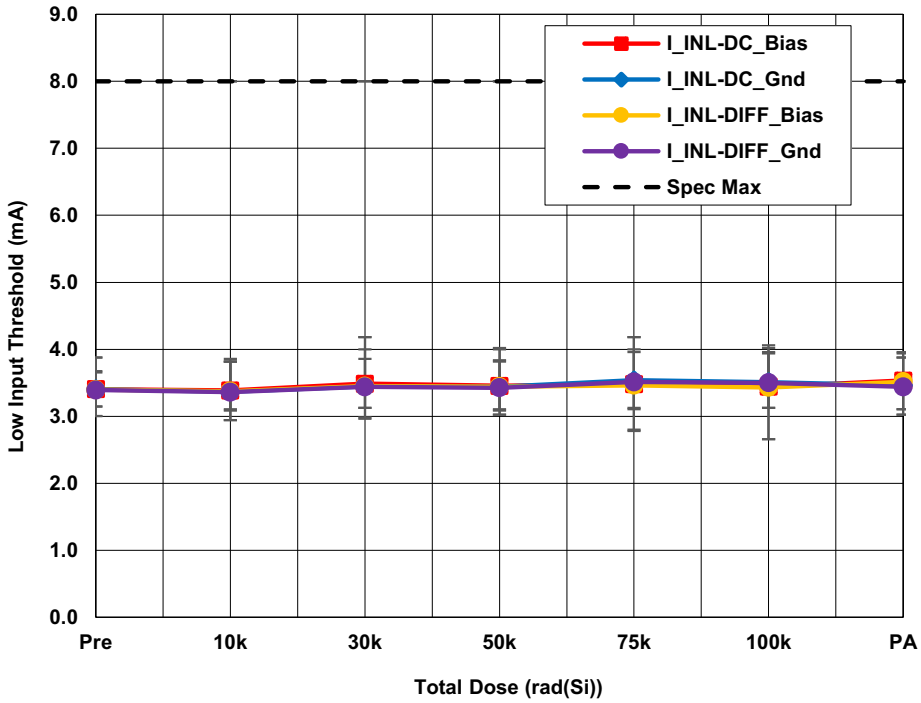

Figure 5. ISL71610x average low input threshold, DC single-ended (I_{INL-DC}) and differential ($I_{INL-DIFF}$) as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 8mA maximum.

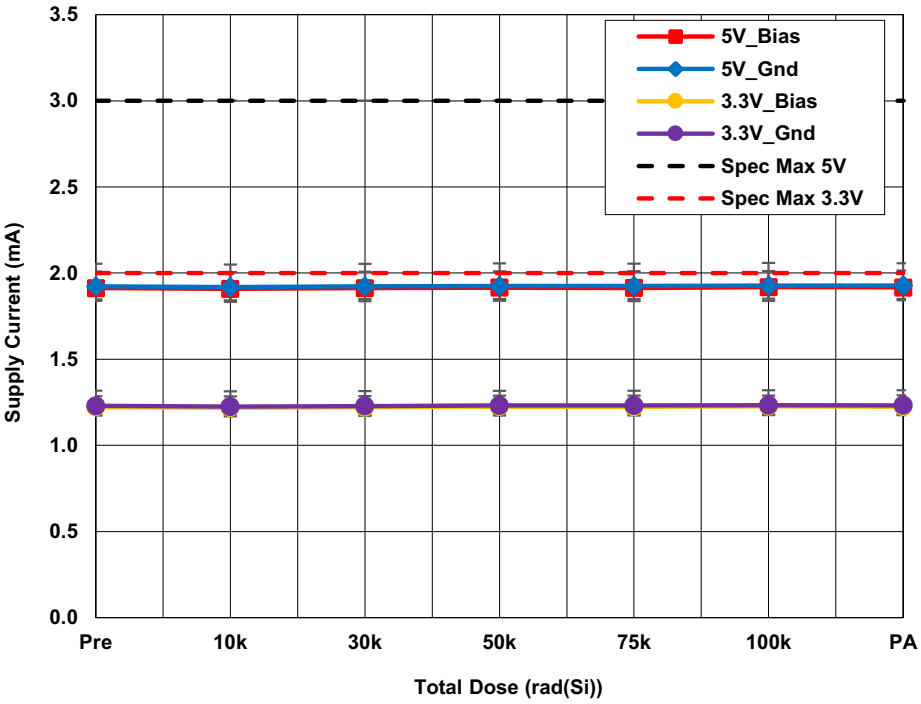

Figure 6. ISL71610x average quiescent current (I_{DDQ}) with V_{DD} = 5.0V and 3.3V and IN+ = IN- = OPEN as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 2mA maximum for 3.3V and 3mA maximum for 5V.

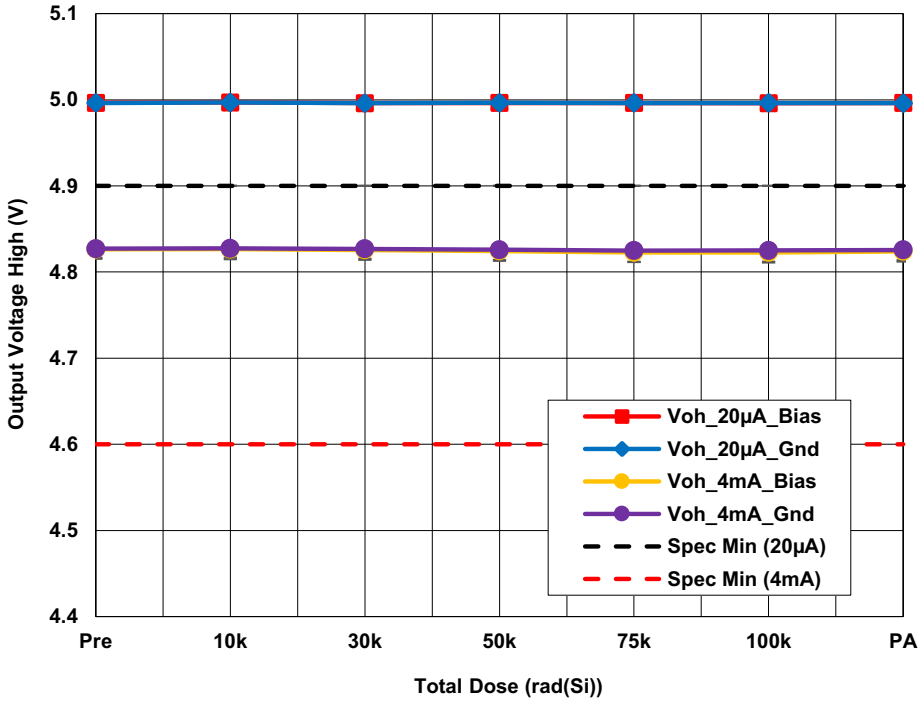

Figure 7. ISL71610x average output voltage high (V_{OH}) with V_{DD} = 5V and I_{OUT} = 20µA and 4mA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 4.9V minimum for 20µA and 4.6V minimum for 4mA.

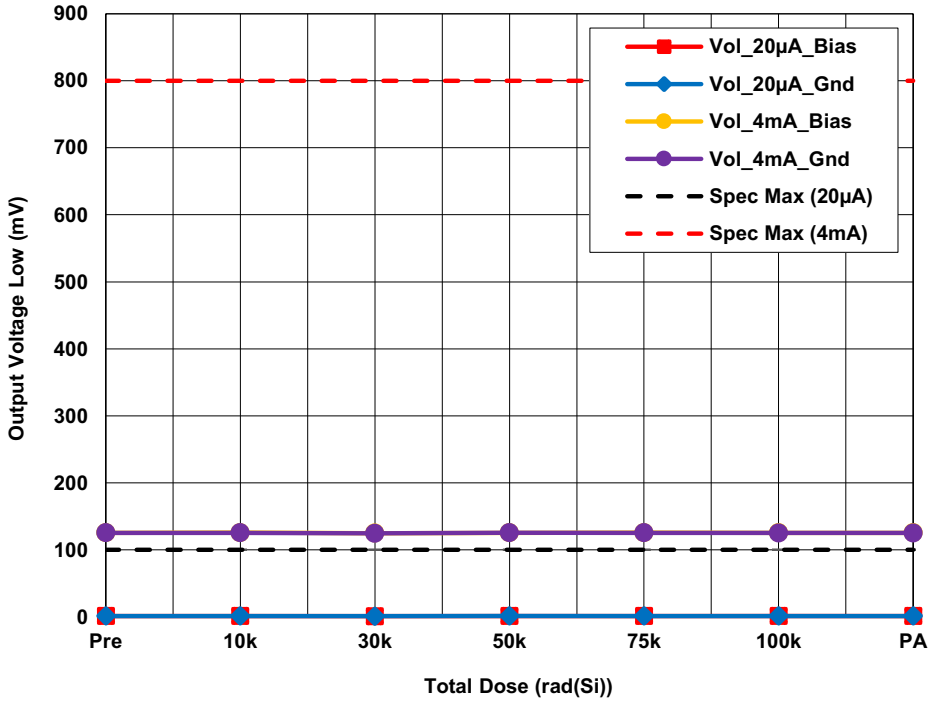

Figure 8. ISL71610x average output voltage low (V_{OL}) with V_{DD} = 5V and I_{OUT} = -20µA and -4mA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 100mV maximum for -20µA and 800mV maximum for -4mA.

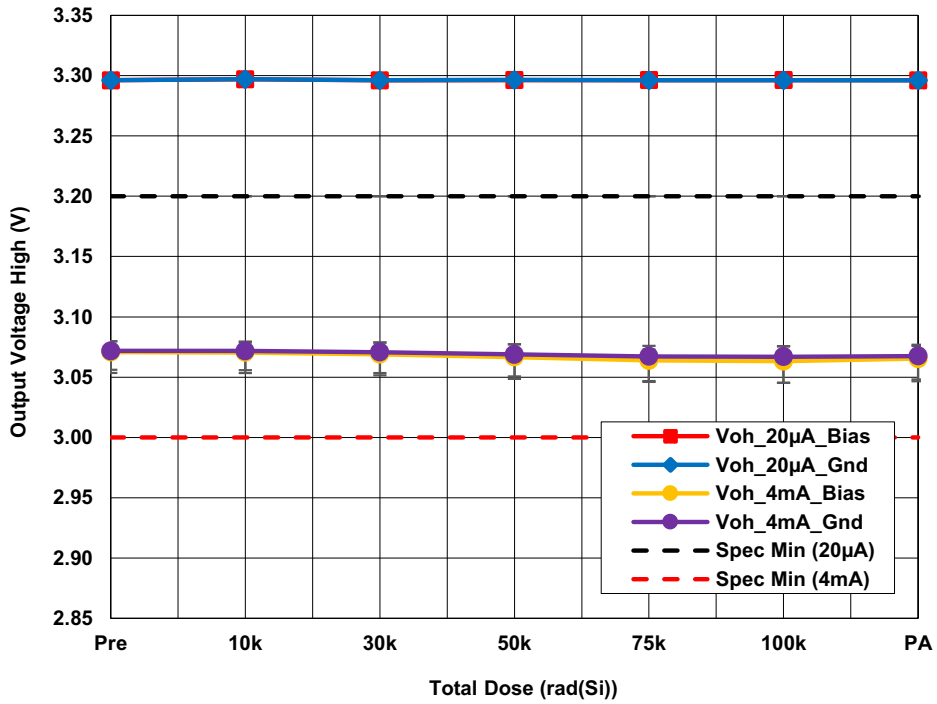

Figure 9. ISL71610x average output voltage high (V_{OH}) with V_{DD} = 3.3V and I_{OUT} = 20µA and 4mA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 3.2V minimum for 20µA and 3.0V minimum for 4mA.

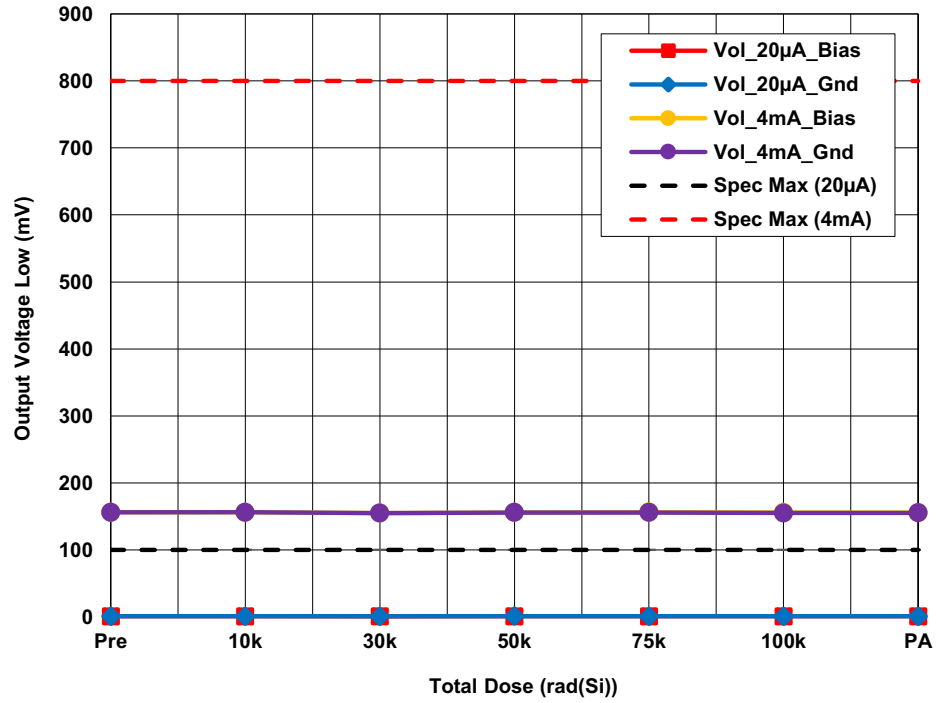

Figure 10. ISL71610x average output voltage low (V_{OL}) with V_{DD} = 3.3V and I_{OUT} = -20µA and -4mA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 100mV maximum for -20µA and 800mV maximum for -4mA.

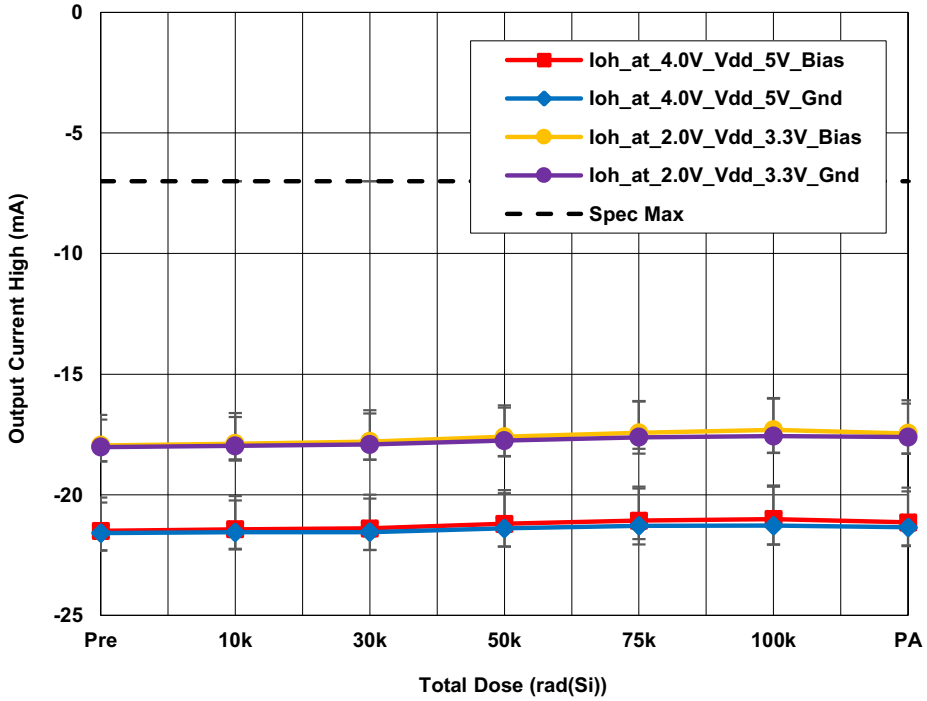

Figure 11. ISL71610x average logic high output drive current (I_{OH}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is -7.0mA maximum.

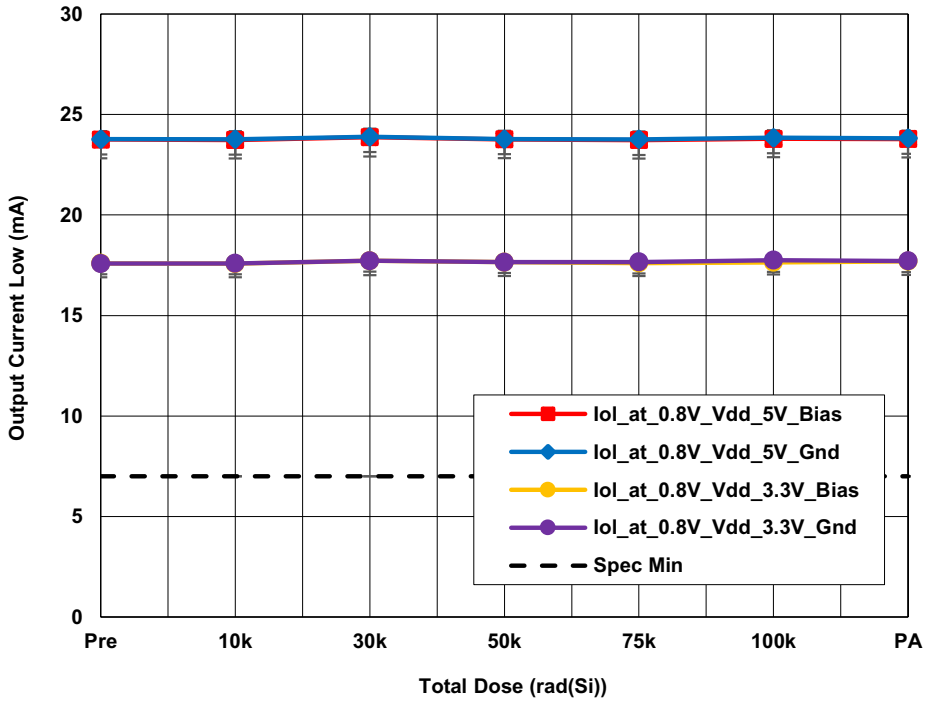

Figure 12. ISL71610x average logic low output drive current (I_{OL}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 7.0mA minimum.

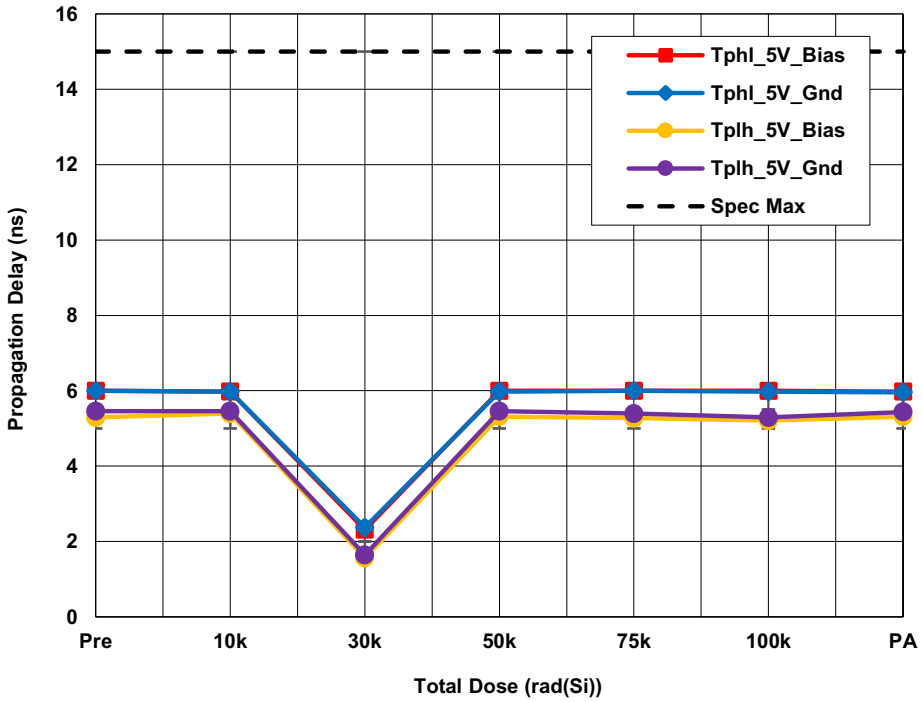

Figure 13. ISL71610x average propagation delay (t_{PHL}, t_{PLH}) with V_{DD} = 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 15ns maximum.

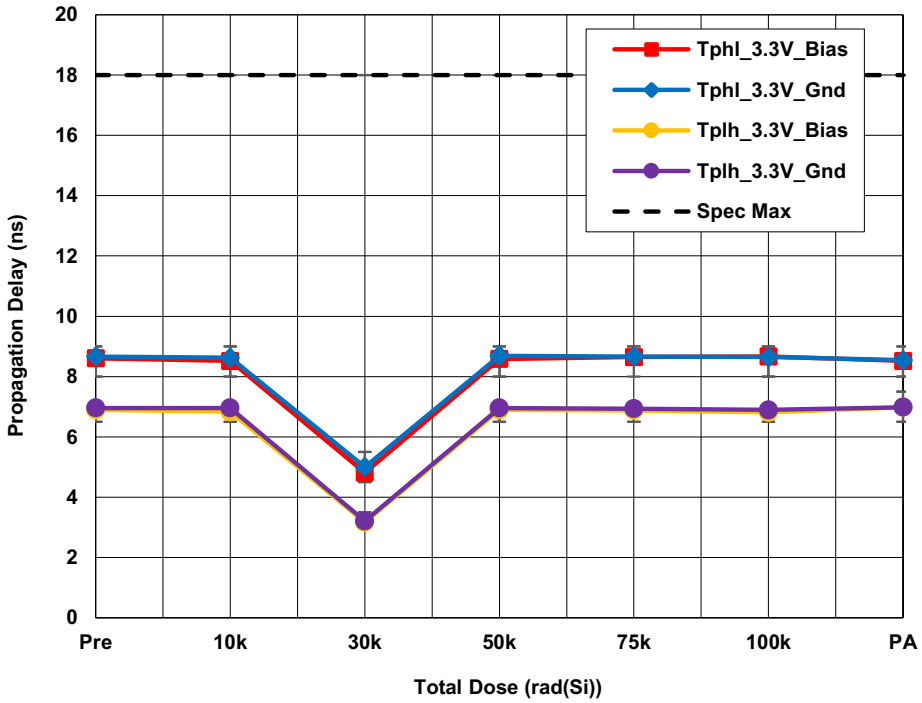

Figure 14. ISL71610x average propagation delay (t_{PHL}, t_{PLH}) with V_{DD} = 3.3V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 18ns maximum.

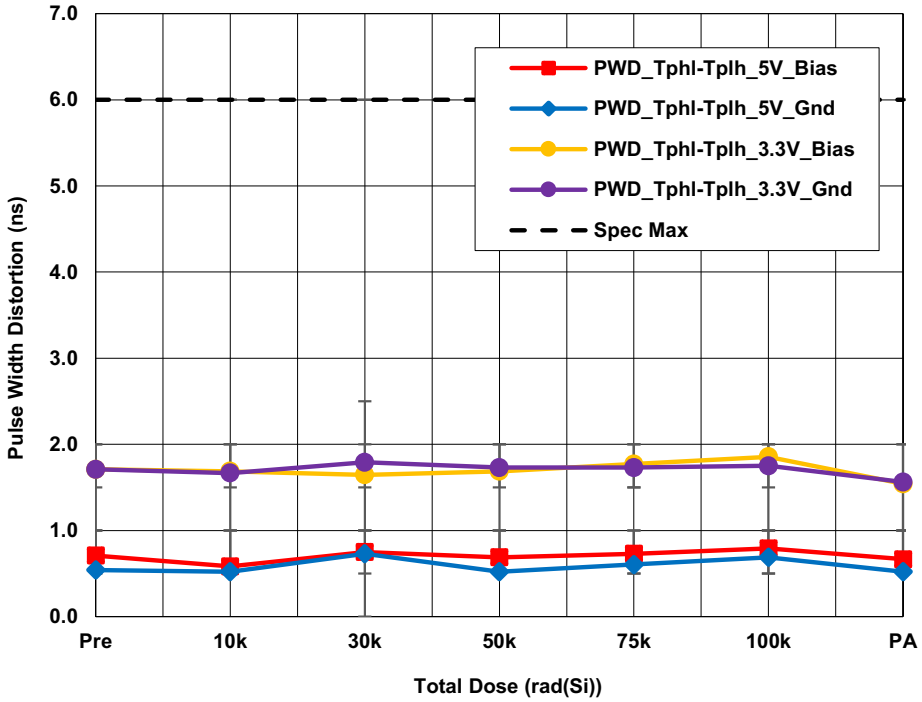

Figure 15. ISL71610x average Pulse Width Distortion (PWD) as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 6ns maximum.

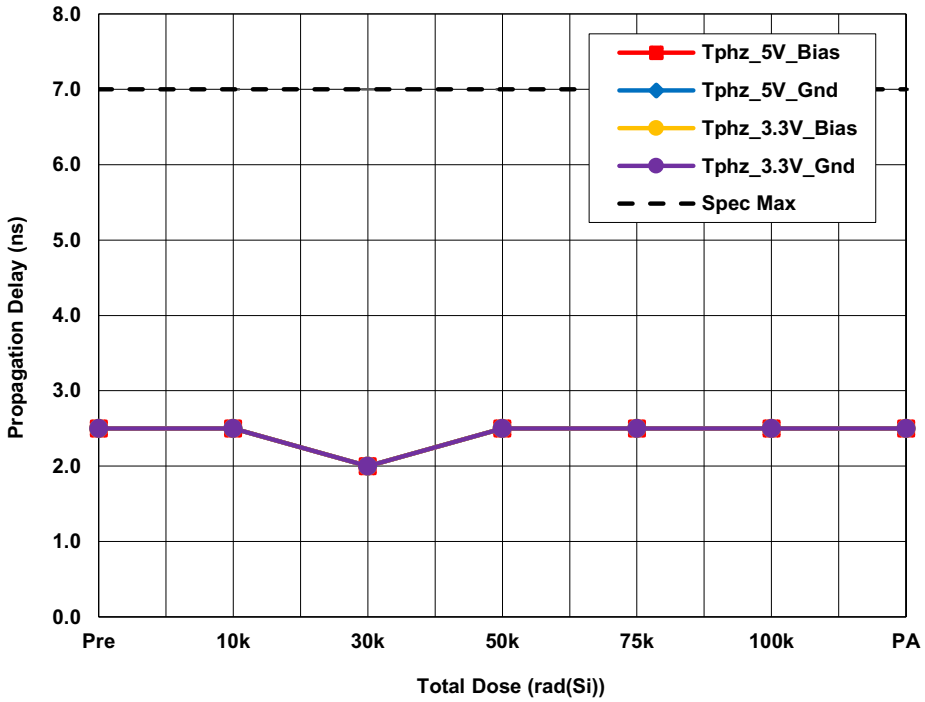

Figure 16. ISL71610x average enable to output propagation delay, high-to-high impedance (t_{PHZ}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

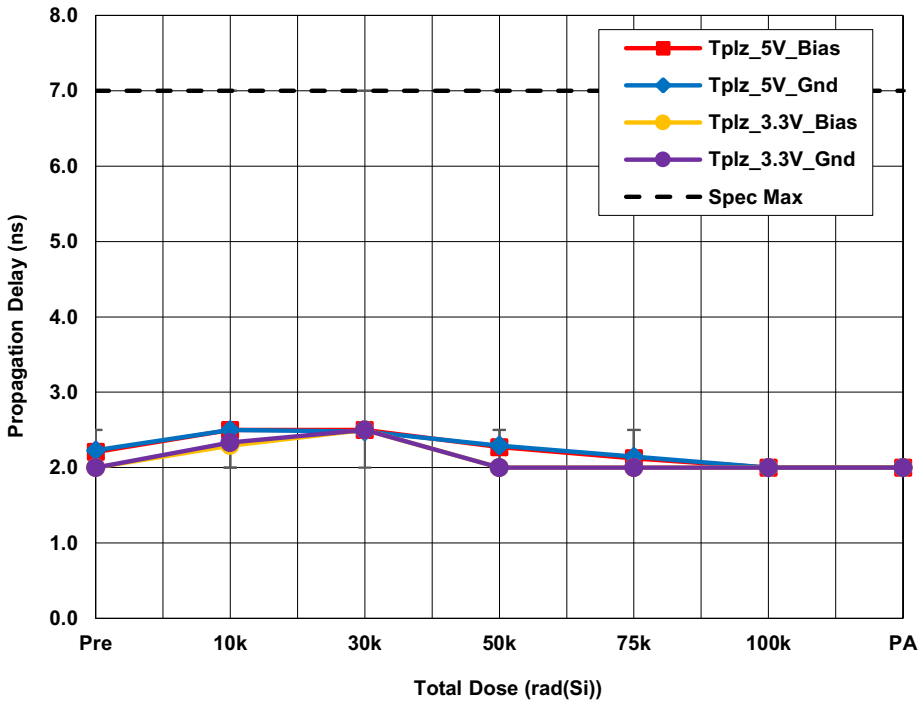

Figure 17. ISL71610x average enable to output propagation delay, low-to-high impedance (t_{PLZ}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

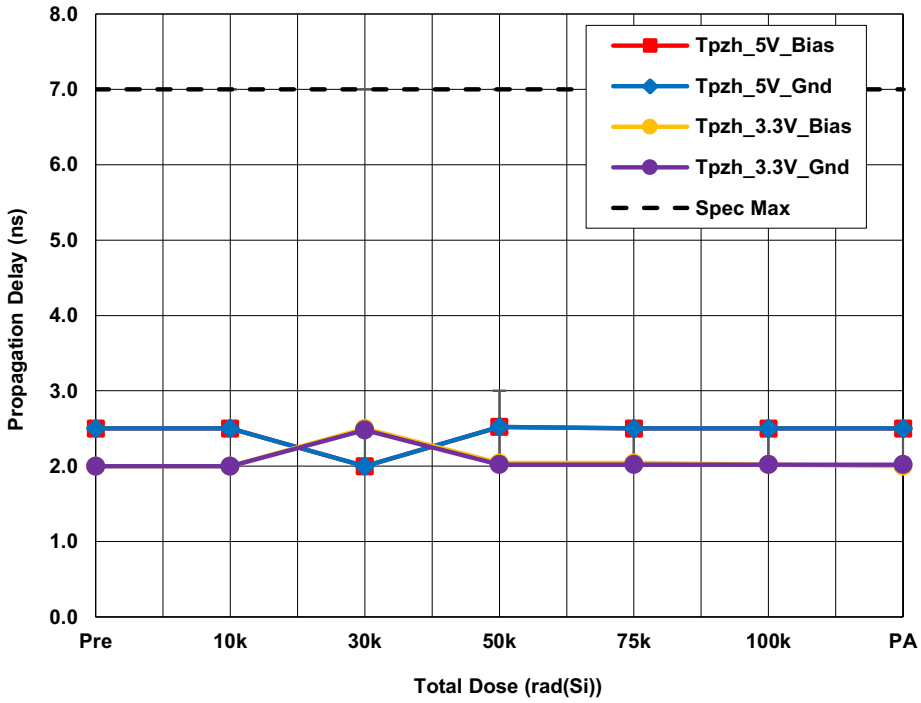

Figure 18. ISL71610x average enable to output propagation delay, high impedance-to-high (t_{PZH}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

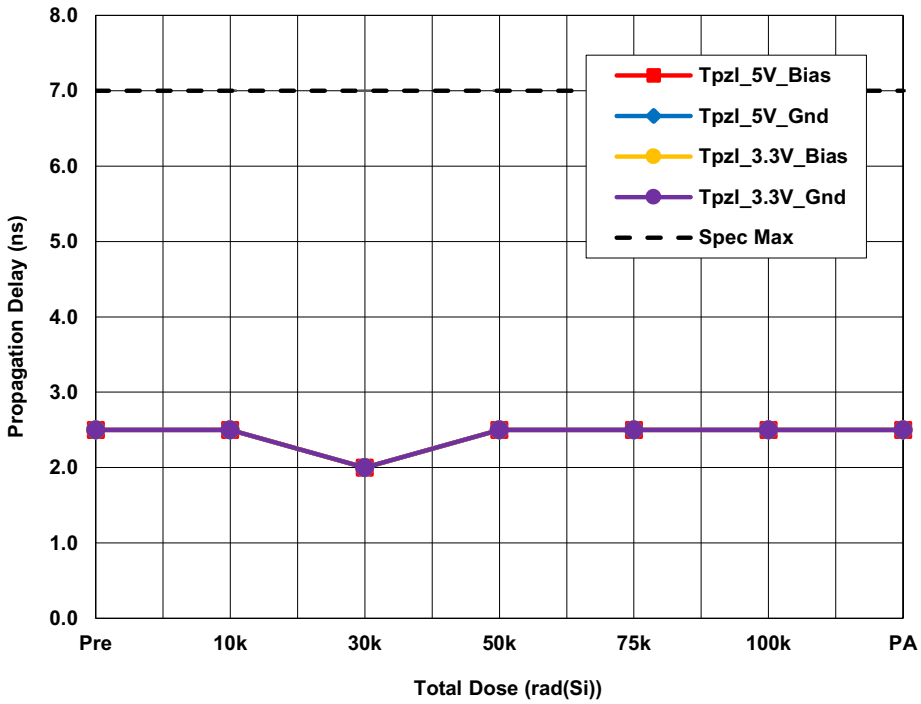

Figure 19. ISL71610x average enable to output propagation delay, high impedance-to-low (t_{PZL}) with V_{DD} = 3.3V and 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

3. Discussion and Conclusion

We report the results of a LDR total dose test of the ISL71610x radiation tolerant passive-input digital isolator. The irradiation of biased and grounded samples to 100krad(Si) was followed by a 168 hour anneal at 100°C under bias. All datasheet parameters passed at all downpoints, but as can be seen in Figure 13, Figure 14, Figure 17, Figure 18 and Figure 19, the ATE AC measurements (propagation delays) were not quite the same at the 30krad(Si) downpoint as the other downpoints, probably because of a slight setup variation. No evidence of bias dependence was observed.

4. Appendices

4.1 Reported Parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 19. All limits are taken from the ISL71610SLHM and ISL71610M datasheets.

Table 3. ISL71610x Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
3	Coil Input Resistance	R_{COIL}	V_{DD} = 3.0 - 5.5V	47	112	Ω
4	DC High Input Threshold	I_{INH-DC}	Single Ended Circuit, V_{DD} = 4.5 - 5.5V	0.5	-	mA
		$I_{INH-DIFF}$	Differential Circuit, V_{DD} = 3.0 - 5.5V, C_{BOOST} = 0pF			
5	DC Low Input Threshold	I_{INL-DC}	Single Ended Circuit, V_{DD} = 4.5 - 5.5V	-	8	mA
		$I_{INL-DIFF}$	Differential Circuit, V_{DD} = 3.0 - 5.5V, C_{BOOST} = 0pF			

Table 3. ISL71610x Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
6	Quiescent Current	I_{DDQ}	V_{DD} = 5.0V, IN+ = IN- = OPEN	-	3	mA
			V_{DD} = 3.3V, IN+ = IN- = OPEN	-	2	mA
7	Logic High Output Voltage	V_{OH}	V_{DD} = 5V, I_{OUT} = 20µA	4.9	-	V
			V_{DD} = 5V, I_{OUT} = 4mA	4.6	-	V
8	Logic Low Output Voltage	V_{OL}	V_{DD} = 5V, I_{OUT} = -20µA	-	0.1	V
			V_{DD} = 5V, I_{OUT} = -4mA	-	0.8	V
9	Logic High Output Voltage	V_{OH}	V_{DD} = 3.3V, I_{OUT} = 20µA	3.2	-	V
			V_{DD} = 3.3V, I_{OUT} = 4mA	3.0	-	V
10	Logic Low Output Voltage	V_{OL}	V_{DD} = 3.3V, I_{OUT} = -20µA	-	0.1	V
			V_{DD} = 3.3V, I_{OUT} = -4mA	-	0.8	V
11	Logic High Output Drive Current	I_{OH}	V_{DD} = 3.3V, 5V	-	-7	mA
12	Logic Low Output Drive Current	I_{OL}	V_{DD} = 3.3V, 5V	7	-	mA
13	Propagation Delay	t_{PHL} / t_{PLH}	V_{DD} = 5V, single-ended circuit, T_{IR} = T_{IF} = 3ns, C_{BOOST} = C_{OUT} = 16pF, R_{OUT} = 1kΩ	-	15	ns
14	Propagation Delay	t_{PHL} / t_{PLH}	V_{DD} = 3.3V, single-ended circuit, T_{IR} = T_{IF} = 3ns, C_{BOOST} = C_{OUT} = 16pF, R_{OUT} = 1kΩ	-	18	ns
15	Pulse Width Distortion	PWD	V_{DD} = 3.3V, 5V, single-ended circuit, T_{IR} = T_{IF} = 3ns, C_{BOOST} = C_{OUT} = 16pF, R_{OUT} = 1kΩ	-	6	ns
16	Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	V_{DD} = 3.3V, 5V, C_L = 15pF	-	7	ns
17	Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	V_{DD} = 3.3V, 5V, C_L = 15pF	-	7	ns
18	Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	V_{DD} = 3.3V, 5V, C_L = 15pF	-	7	ns
19	Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	V_{DD} = 3.3V, 5V, C_L = 15pF	-	7	ns

5. Revision History

Rev.	Date	Description
1.00	Sep.29.20	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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