ISL70003SEH

Total Dose Testing

AN1924
Rev 1.00
October 13, 2016

Introduction

This report provides results of a low and high dose rate total dose test of the ISL70003SEH point-of-load converter. The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if the part is low dose rate sensitive. The test also performs biased high temperature anneals after the completion of irradiation in order to evaluate the accelerated aging characteristics of the part.

Related Literature

- For a full list of related documents please visit our web pages
  - ISL70003SEH product page

Part Description

The ISL70003SEH is a radiation and single-event effects tolerant synchronous buck regulator capable of operating over an input voltage range of 3.0V to 13.2V. Featuring integrated MOSFETs, this efficient single chip power solution provides a regulated output voltage that is externally adjustable from 0.6V to ~90% of the input voltage. Continuous output load current capability is 6A for $T_J \leq +125°C$ and 3A for $T_J \leq +150°C$. The ISL70003SEH uses voltage mode control architecture with feed-forward and switches at pin-selected frequencies of 500kHz or 300kHz. Loop compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance. The internal synchronous power switches are optimized for high efficiency and excellent thermal performance. The chip features two logic-level disable inputs that can be used to inhibit pulses on the phase (LXx) pins in order to maximize efficiency based on the load current.

The ISL70003SEH also supports DDR applications and contains a buffer amplifier for generating the VREF voltage. Typical ISL70003SEH applications include FPGA, CPLD and DSP power management, CPU core and I/O supply, and DDR memory power management in high-density distributed power systems for space applications. The part is available in a 64 Ld lead CQFP with a built-in heat sink (R64.C) or without a heat sink (R64.A).

The ISL70003SEH is radiation tolerant to a total dose (TID) rating of 100krad(Si) at both high (50 to 300rad(Si)/s) and low (<0.01rad(Si)/s) dose rates as specified in MIL-STD-883 test method 1019.7. The present document reports data for 150krad(Si) at low dose rate and 150krad(Si) at high dose rate, with the irradiations followed by a biased anneal at +100°C for 168 hours. No failures were encountered at any downpoint. The part is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate, and to 100krad(Si) at high dose rate, as indicated by the EH suffix in the part number.

The ISL70003SEH is also Single-Event Effects (SEE) tolerant to a Linear Energy Transfer (LET) value of $86.4 MeV \cdot cm^2/mg$. Single-Event Transients (SET) are a major issue in power management parts driving voltage-sensitive loads, and the ISL70003SEH provides superior performance [1] in this environment.

The ISL70003SEH is implemented in a submicron BiCMOS process optimized for power management applications. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial power management devices.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

Test Description

Irradiation Facilities

High dose rate testing was performed using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing used a Hopewell Designs (Alpharetta, GA) N40 vault-type low dose rate irradiator located in the same facility. The high dose rate irradiations were performed at 64.9rad(Si)/s and the low dose rate work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Test Method 1019.7. In the low dose rate facility, PbAl spectrum hardening boxes are used to shield the test fixture and devices under test against low energy secondary gamma radiation. The post-irradiation biased anneals were performed at 100°C using a small temperature chamber.

Test Fixturing

Figure 1 on page 2 shows the irradiation biased configuration per Standard Microcircuit Drawing (SMD) 5962-14203. This configuration was used for low and high dose rate testing.

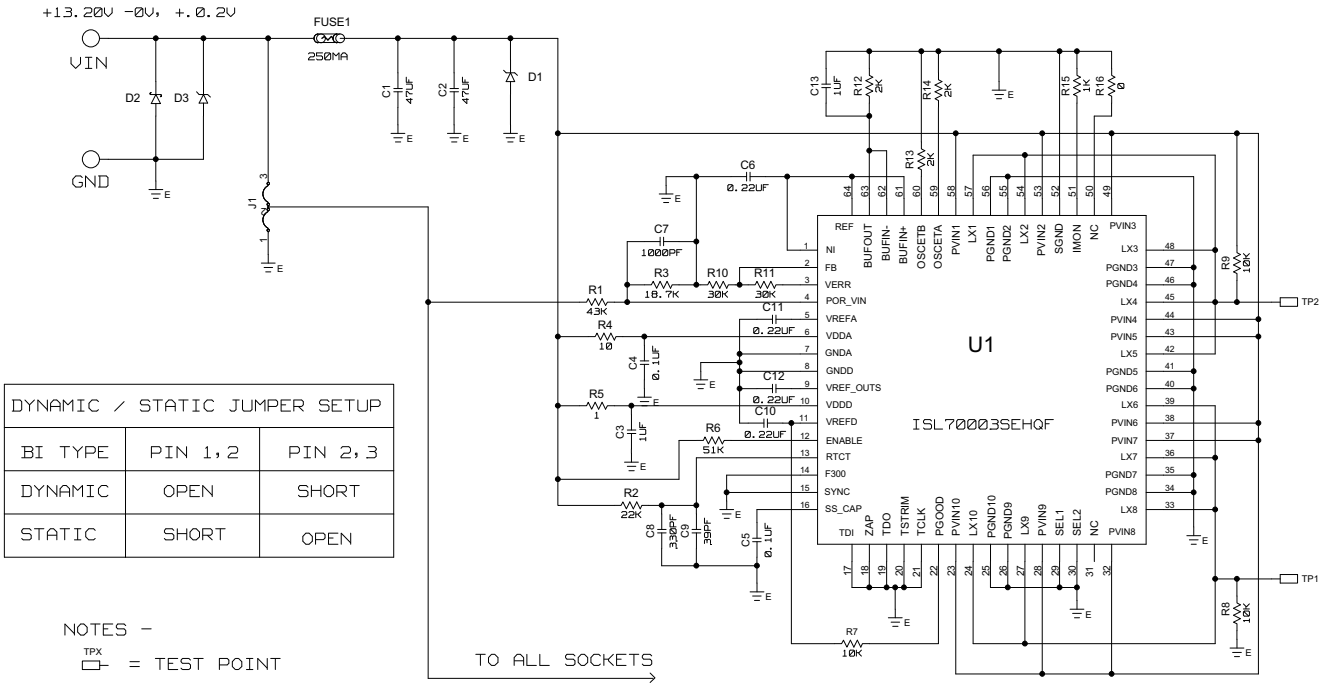

FIGURE 1. IRRADIATION BIAS CONFIGURATION FOR THE ISL70003SEH PER STANDARD MICROCIRCUIT DRAWING (SMD) 5962-14203.

Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

Experimental Matrix

Testing proceeded in accordance with the low dose rate sensitivity diagnostic protocol outlined in MIL-STD-883 Test Method 1019.7. The experimental matrix consisted of six samples irradiated at high dose rate with all pins grounded, six samples irradiated at high dose rate under bias, six samples irradiated at low dose rate with all pins grounded, and six samples irradiated at low dose rate under bias. Three control units were used.

A biased anneal at 100°C for 168 hours was performed following the irradiations to evaluate the accelerated aging characteristics of the part.

Samples of the ISL70003SEH were drawn from Lot 3X4FB, date code 1340 (lot sealed 30 September 2013). Samples were packaged in the standard hermetic 64 Ld ceramic quad flatpack (CQFP) production package, code RKV. Samples were processed through the standard QML-V burnin screens of 180 hours dynamic burnin and 72 hours static burnin cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-14203 SMD limits at room, low, and high temperatures before the start of total dose testing.

Downpoints

The high dose rate downpoints were 0, 30, 50, 100, and 150krad(Si). The low dose rate downpoints were 0, 10, 30, 50, 100, and 150krad(Si). The biased anneals were performed at 100°C for 168 hours.

Results

Total dose testing of the ISL70003SEH showed no reject devices after biased or grounded irradiation at either dose rate. All samples were classified as Bin 1 at all downpoints including anneal, indicating full compliance with all datasheet and SMD parametric limits.

Attributes Data

Table 1 shows the attributes data.

TABLE 1. ISL70003SEH ATTRIBUTES DATA

PART	DOSE RATE, (rad(Si)/s)	BIAS	SAMPLE SIZE	DOWNPOINT	PASS (Note 1)	FAIL
ISL70003SEH	0.01	Biased	6	Pre-irradiation	6	0
				10krad(Si)	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0
ISL70003SEH	0.01	Grounded	6	Pre-irradiation	6	0
				10krad(Si)	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0
ISL70003SEH	64.9	Biased	6	Pre-irradiation	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0
ISL70003SEH	64.9	Grounded	6	Pre-irradiation	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0

NOTE:

1. ‘Pass’ indicates a sample that passes all SMD limits.

Variables Data

The ISL70003SEH is a complex part and plotting all of the approximately 300 tested parameters would be a lengthy undertaking. The plots in Figures 2 through 30 show data for representative parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the median because of the relatively small sample sizes involved. Figure 7 reports the total dose response of the reference tolerance parameter (V_{REF} + error amplifier input offset voltage), and we have plotted the average, minimum, and maximum at each downpoint for this parameter of particular interest.

All parts showed excellent stability over irradiation and anneal, with no observed dose rate or bias sensitivity. It should be noted that the SMD data tables contain no post-total dose limits; the pre- and post-irradiation limits are identical. This implies that the part has no dose rate sensitivity by definition, and this conclusion is confirmed by the data.

Variables Data Plots

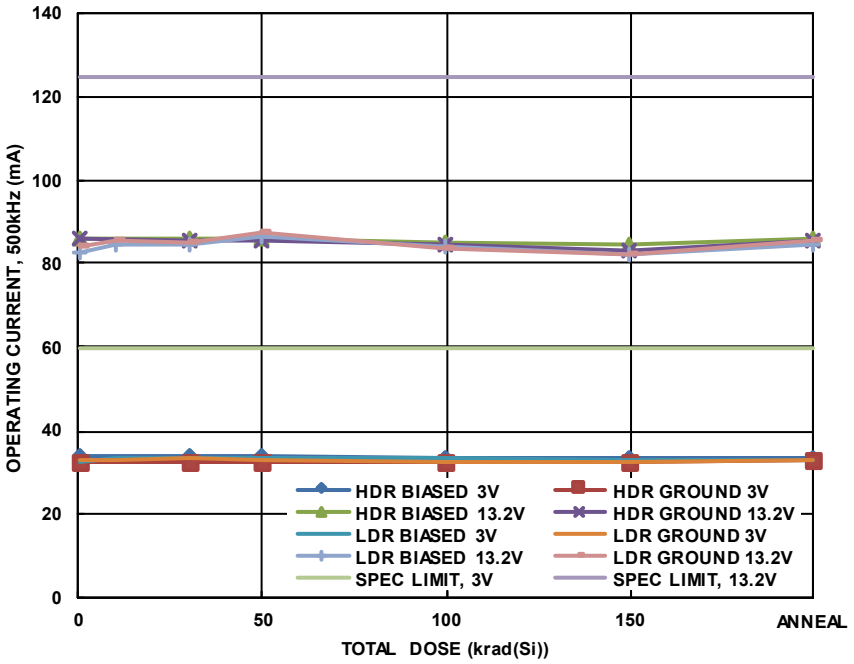

FIGURE 2. ISL70003SEH operating current at 500kHz, 3V, and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 60mA maximum (3V case) and 125mA maximum (13.2V case).

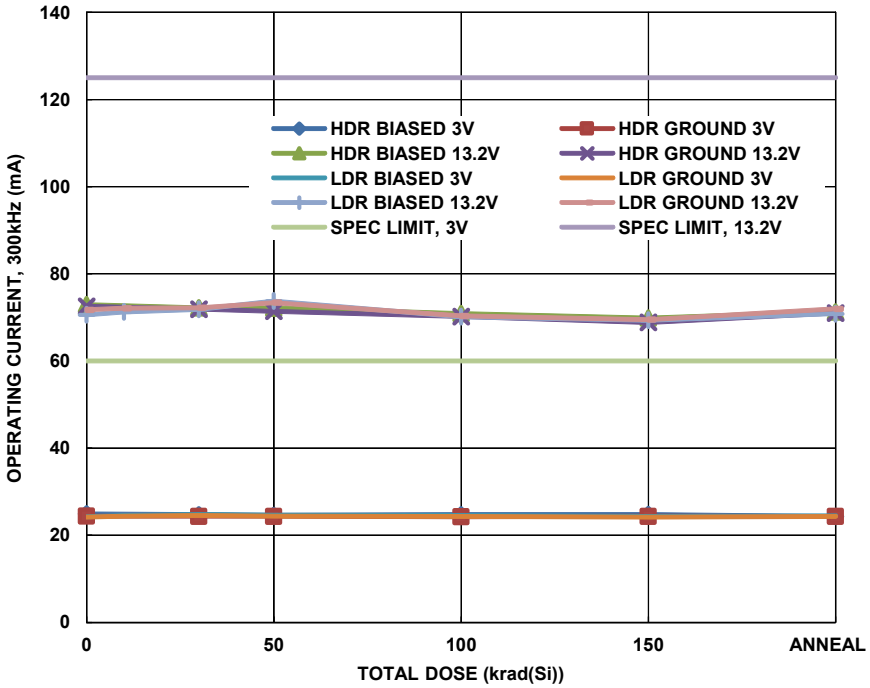

FIGURE 3. ISL70003SEH operating current at 300kHz, 3V, and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 60mA maximum (3V case) and 125mA maximum (13.2V case).

Variables Data Plots (Continued)

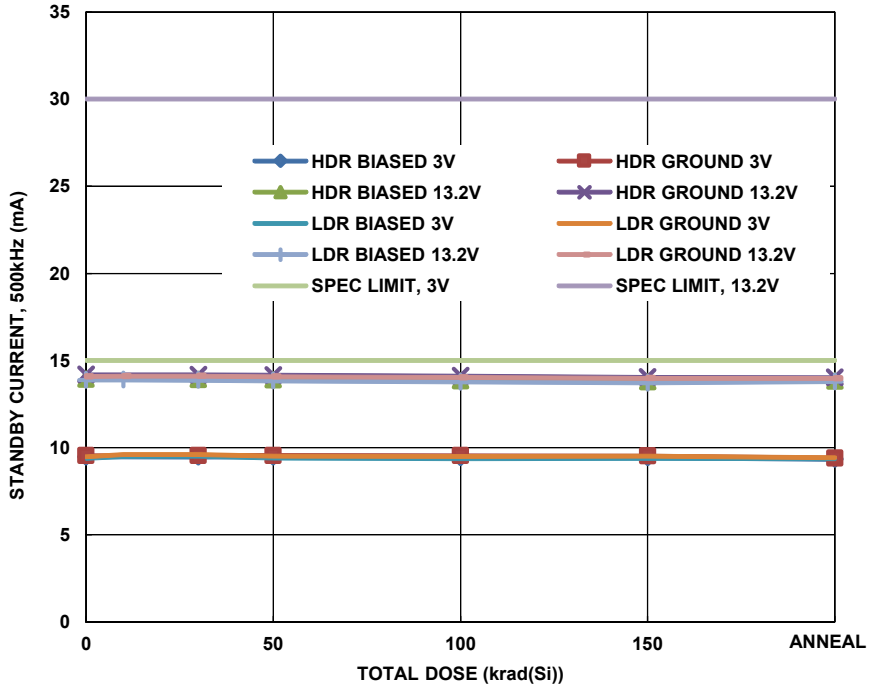

FIGURE 4. ISL70003SEH standby current at 500kHz, 3V, and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 15mA maximum (3V case) and 30mA maximum (13.2V case).

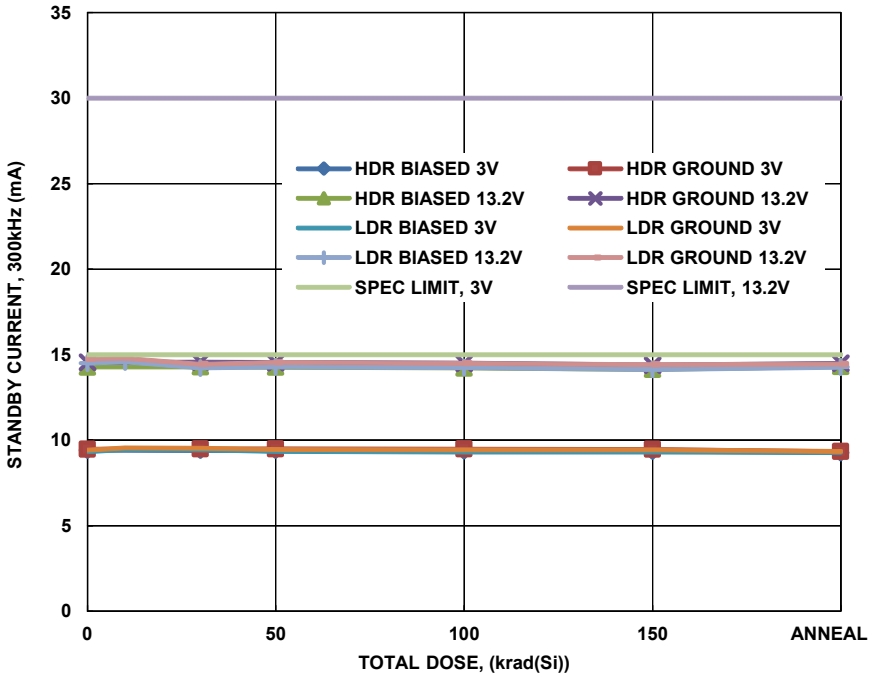

FIGURE 5. ISL70003SEH standby current at 300kHz, 3V, and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 15mA maximum (3V case) and 30mA maximum (13.2V case).

Variables Data Plots (Continued)

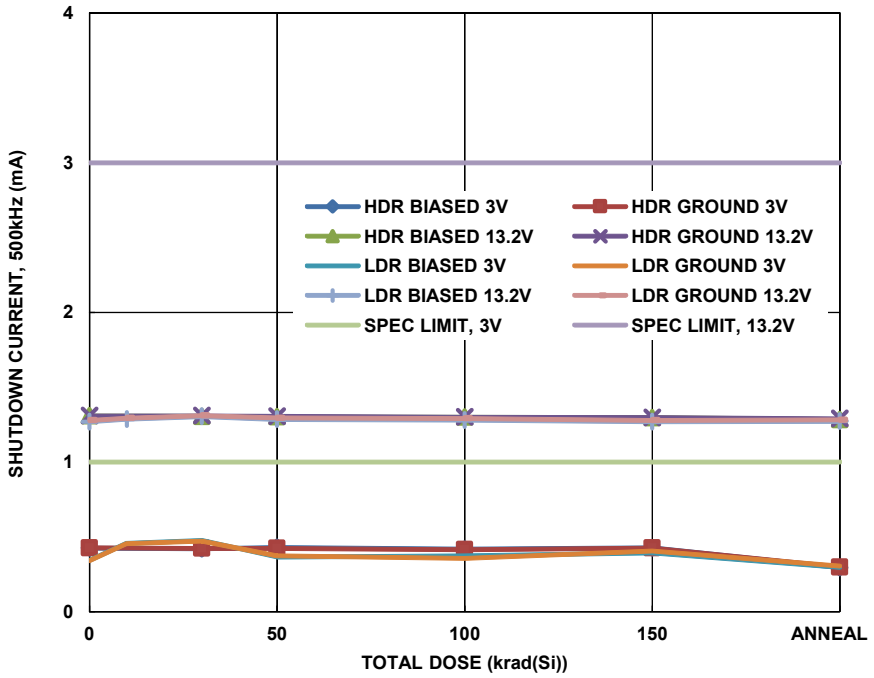

FIGURE 6. ISL70003SEH shutdown ('quiescent') supply current at 500kHz, 3V, and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 1mA maximum (3V case) and 3mA maximum (13.2V case).

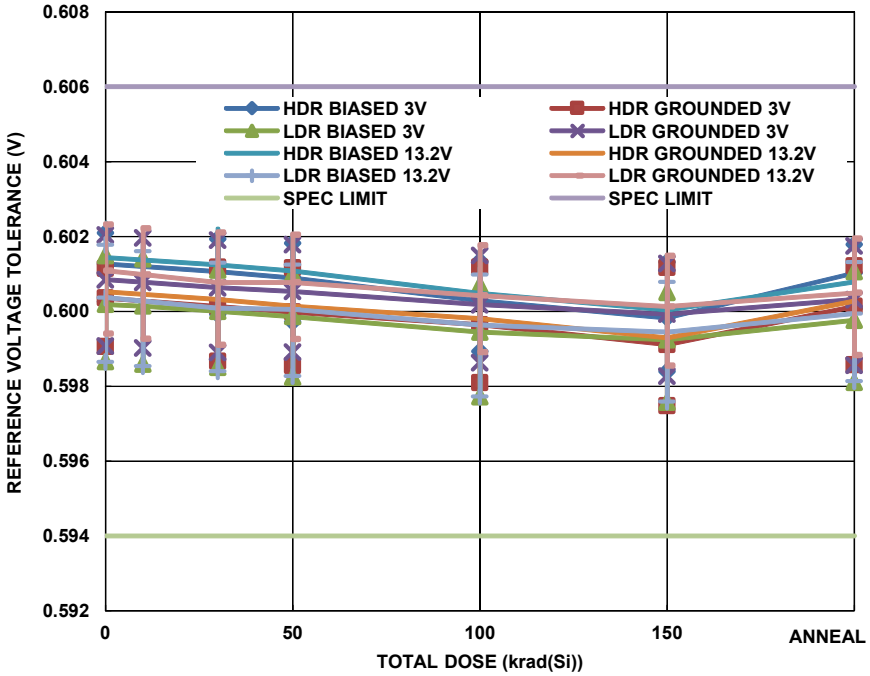

FIGURE 7. ISL70003SEH reference voltage tolerance (reference voltage + error amplifier offset voltage), 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 0.594V to 0.606V. The plot shows the average, minimum, and maximum at each downpoint.

Variables Data Plots (Continued)

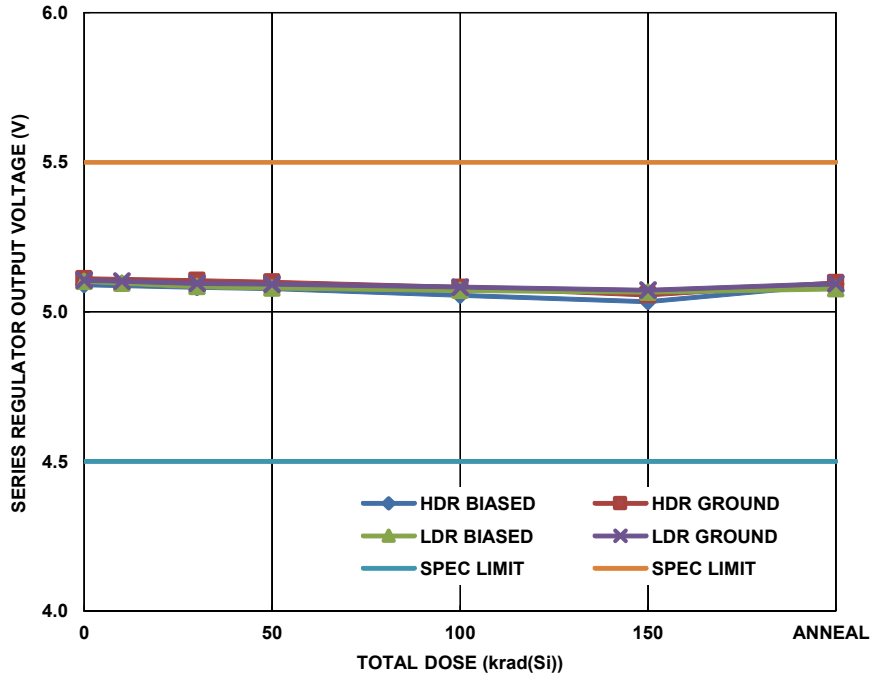

FIGURE 8. ISL70003SEH series regulator output voltage, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 4.5V to 5.5V.

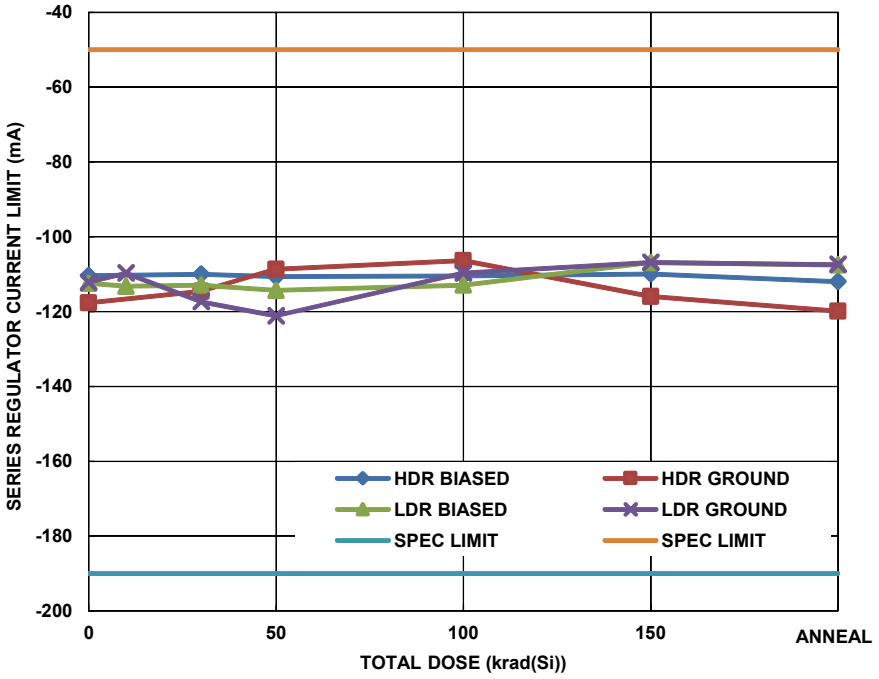

FIGURE 9. ISL70003SEH series regulator current limit, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are -50mA to -190mA.

Variables Data Plots (Continued)

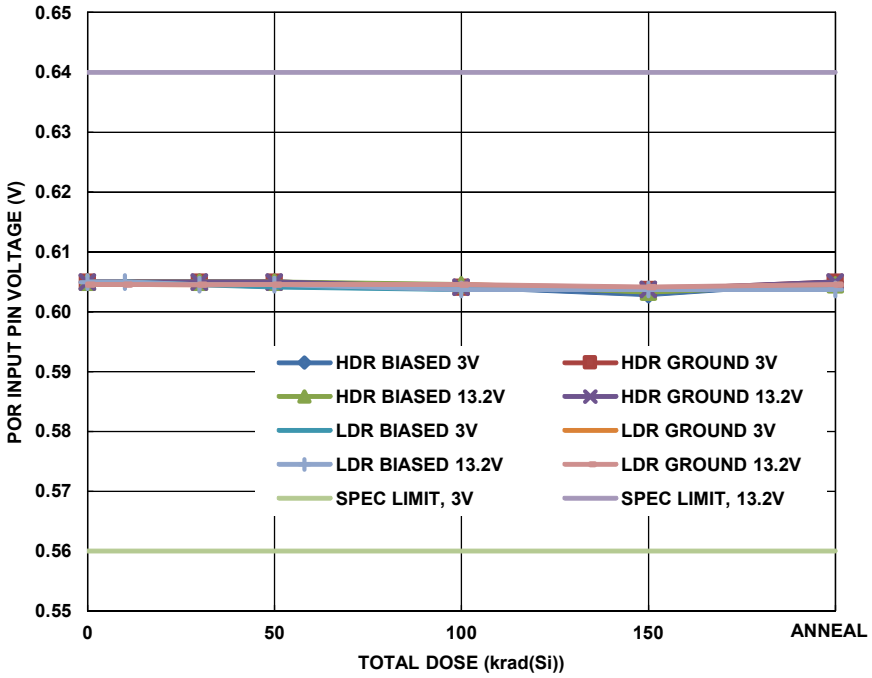

FIGURE 10. ISL70003SEH Power-On Reset (POR) input pin voltage, 3V and 13.3V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 0.56V to 0.64V.

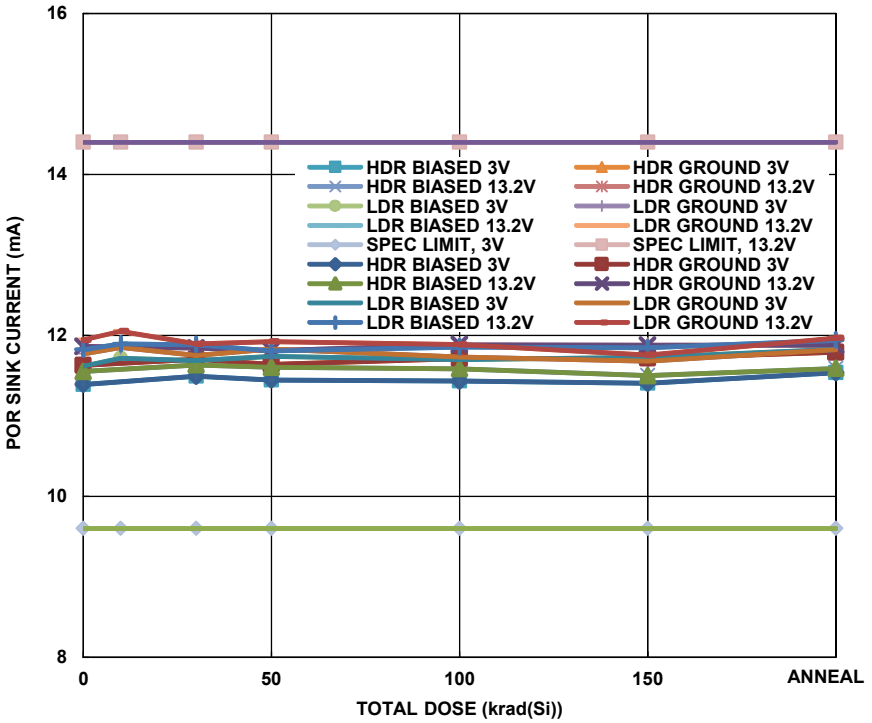

FIGURE 11. ISL70003SEH POR sink current, 3V and 13.3V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 9.6mA to 14.4mA.

Variables Data Plots (Continued)

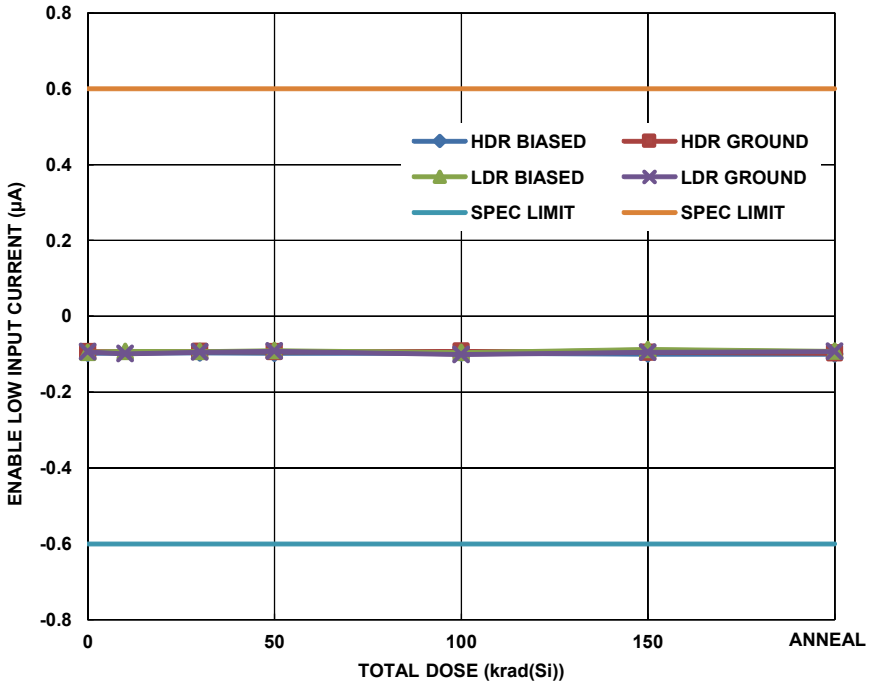

FIGURE 12. ISL70003SEH enable LOW input current, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The parameter is not specified in the SMD; the ATE limits are -0.6µA to +0.6µA.

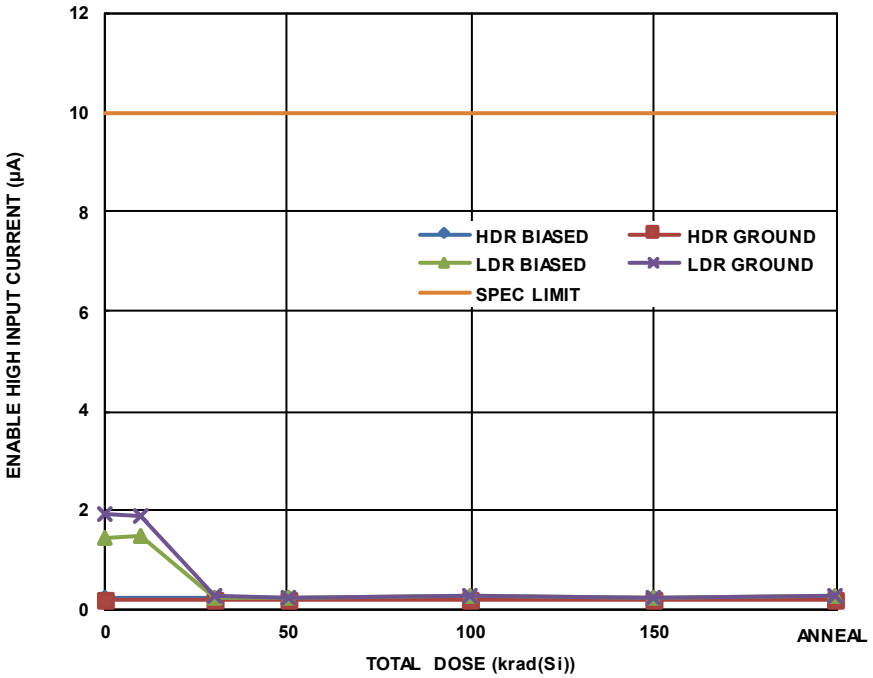

FIGURE 13. ISL70003SEH enable HIGH input current, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s Sample size for each cell was six. The SMD limit is 10.0µA maximum.

Variables Data Plots (Continued)

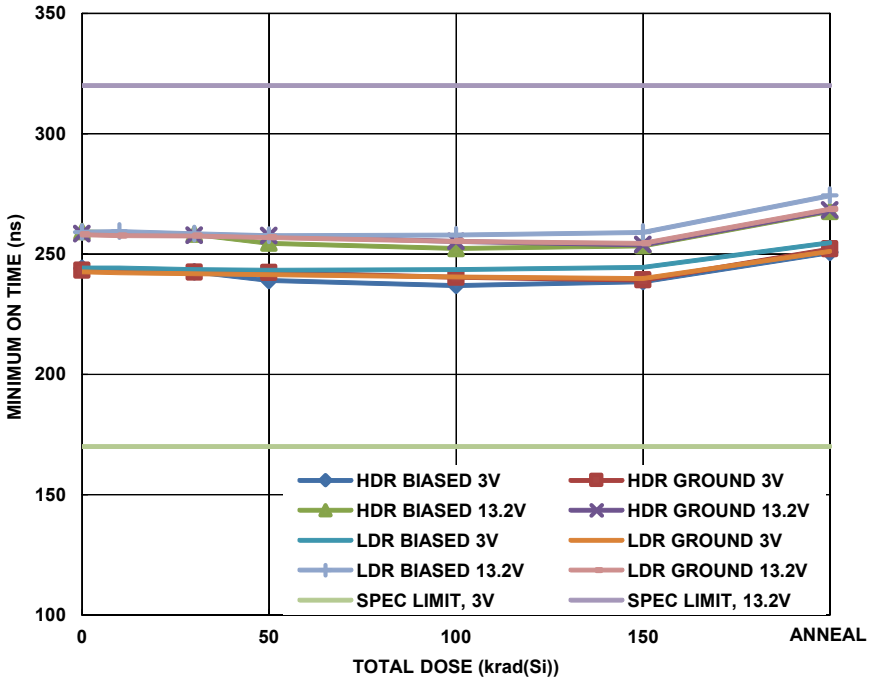

FIGURE 14. ISL70003SEH minimum ON time, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 320ns maximum; the 170ns lower bound is an ATE 'sanity' limit.

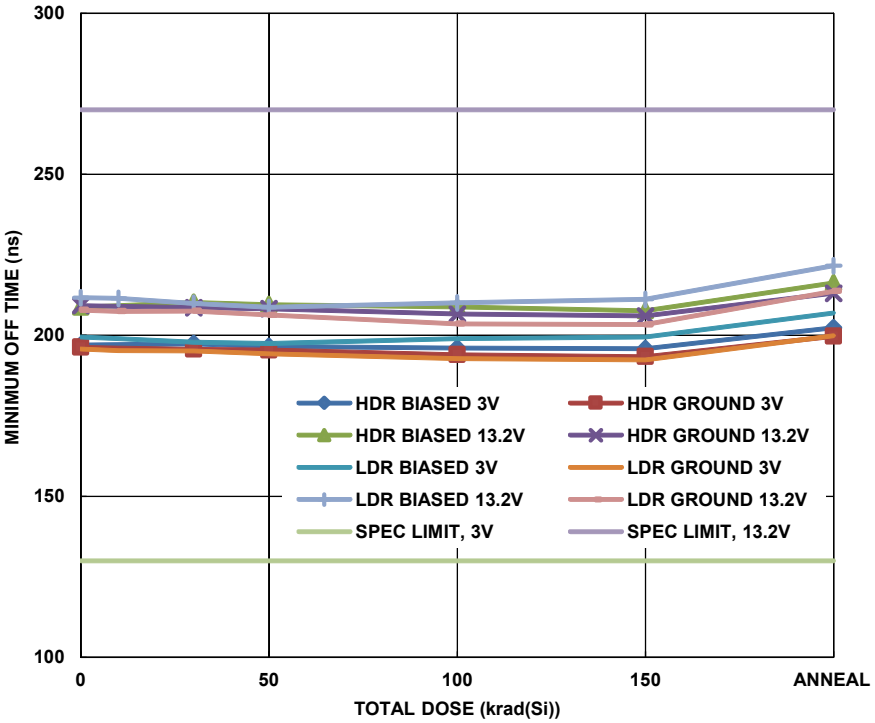

FIGURE 15. ISL70003SEH minimum OFF time, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 270ns maximum; the 130ns lower bound is an ATE 'sanity' limit.

Variables Data Plots (Continued)

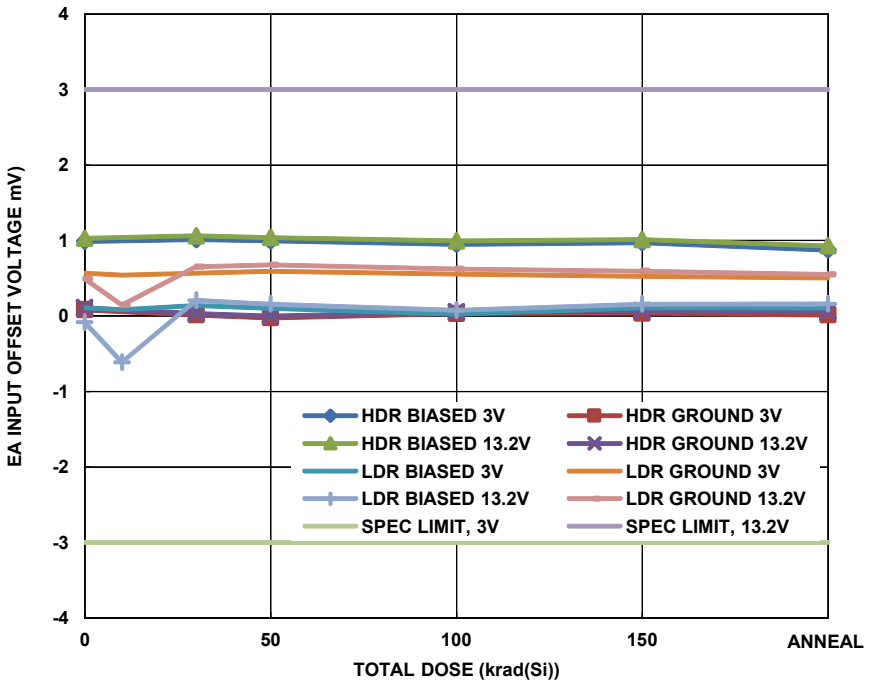

FIGURE 16. ISL70003SEH error amplifier input offset voltage, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are -3.0mV to 3.0mV.

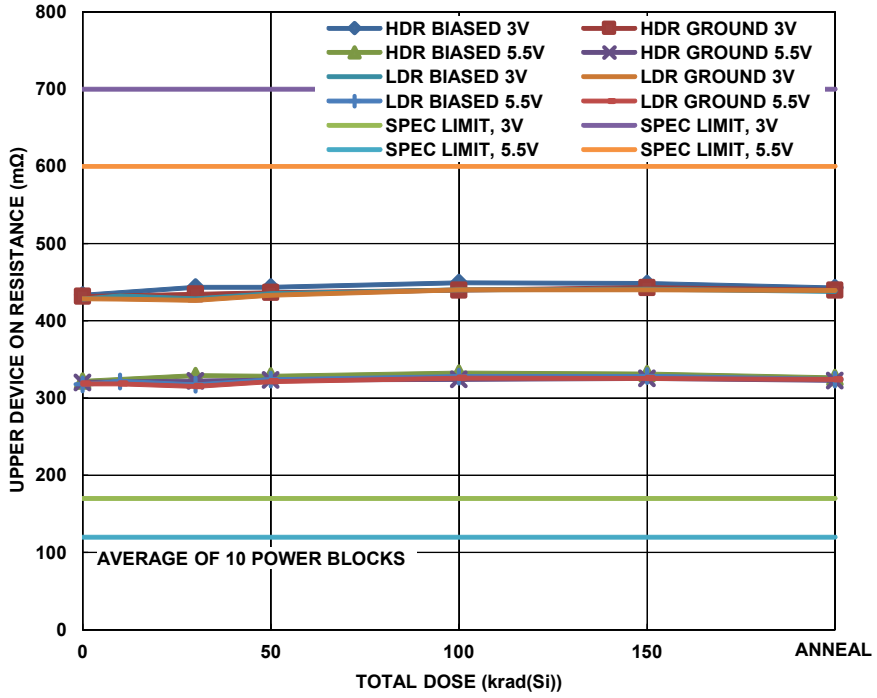

FIGURE 17. ISL70003SEH average upper device ON resistance, 3V and 5.5V supply cases, average of 10 power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 170mΩ to 700mΩ (3V supply) and 120mΩ to 600mΩ (5.5V supply).

Variables Data Plots (Continued)

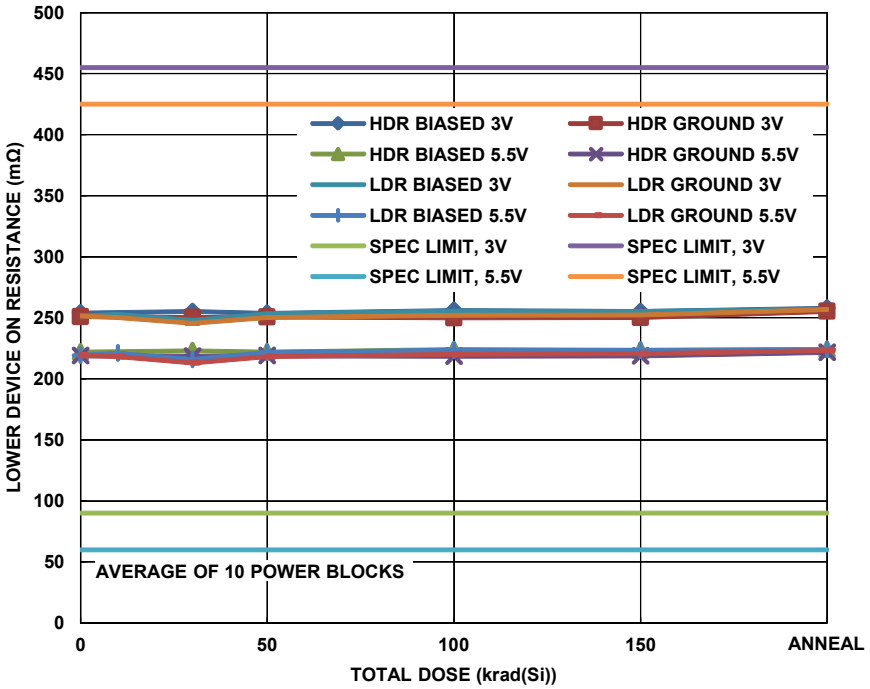

FIGURE 18. ISL70003SEH lower device ON resistance, 3V and 5.5V supply cases, average of 10 power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 90mΩ to 455mΩ (3V supply) and 60mΩ to 425mΩ (5.5V supply).

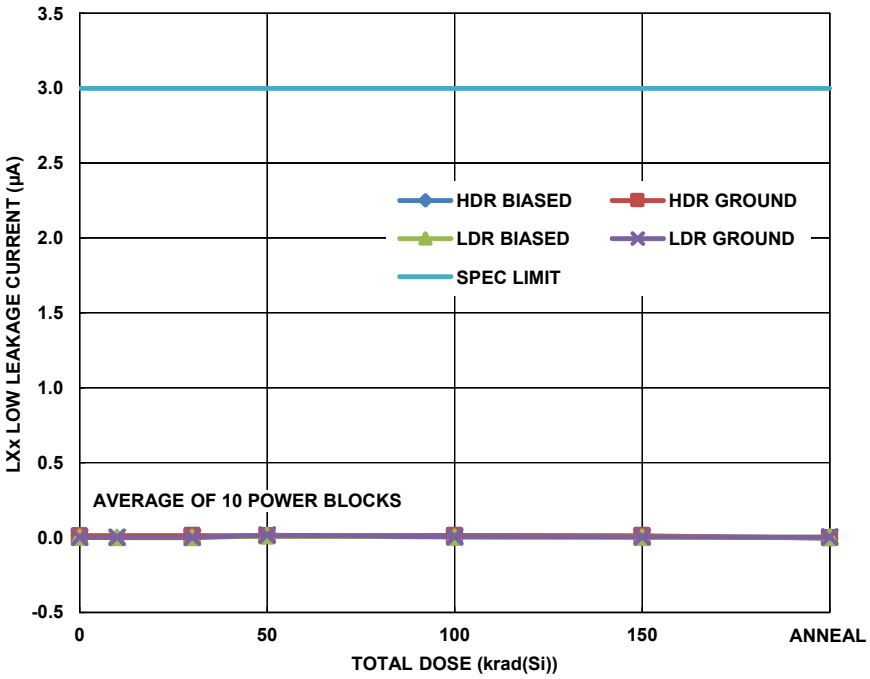

FIGURE 19. Average ISL70003SEH LXx LOW leakage current, average of 10 power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 3.0µA maximum.

Variables Data Plots (Continued)

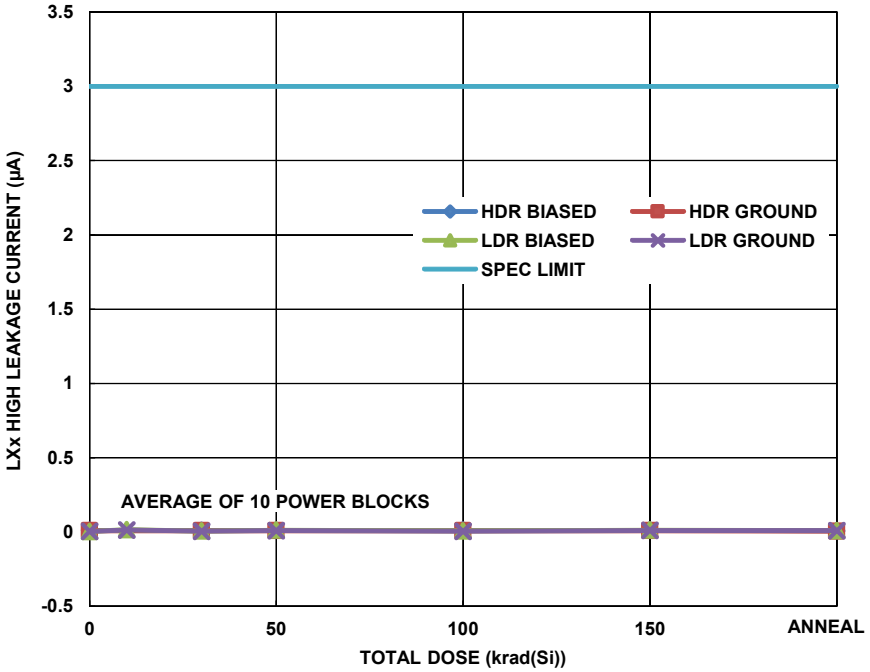

FIGURE 20. Average ISL70003SEH LXx HIGH leakage current, average of 10 power blocks, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 3.0µA maximum.

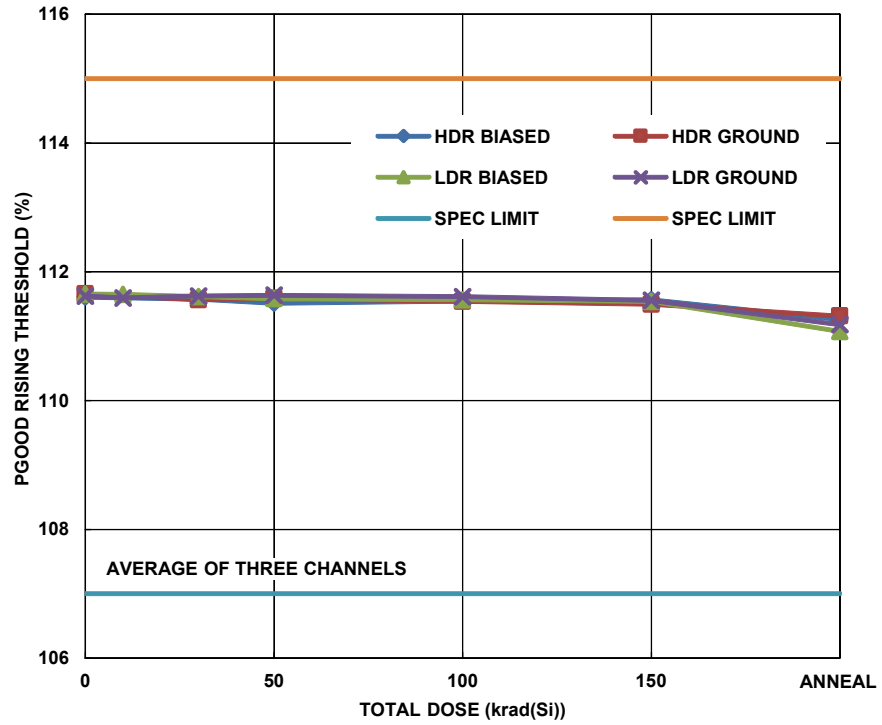

FIGURE 21. ISL70003SEH Power-Good (PGOOD) rising threshold, average of three channels, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 107% to 115%.

Variables Data Plots (Continued)

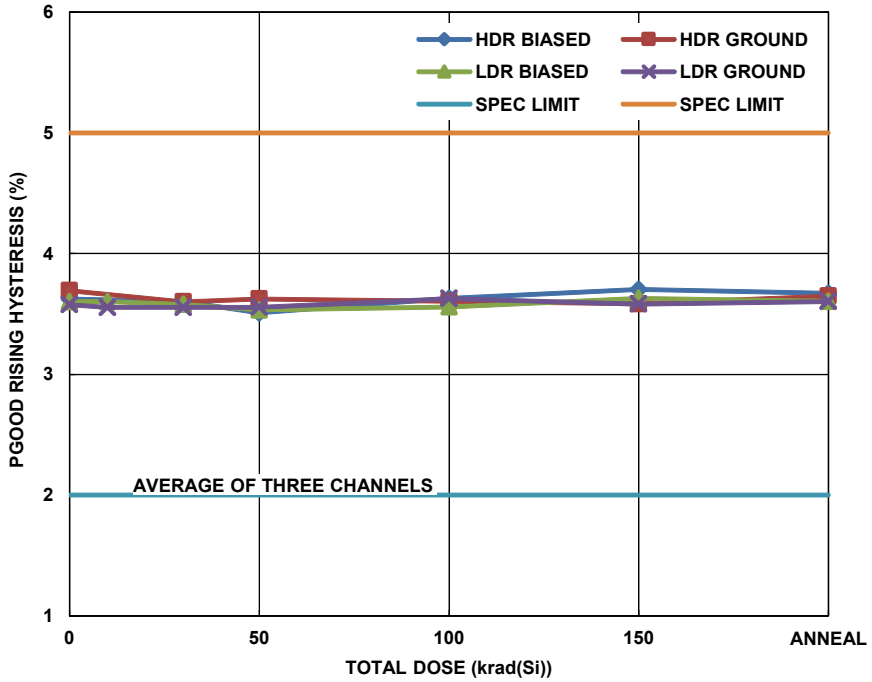

FIGURE 22. ISL70003SEH PGOOD rising hysteresis, average of three channels, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 2% to 5%.

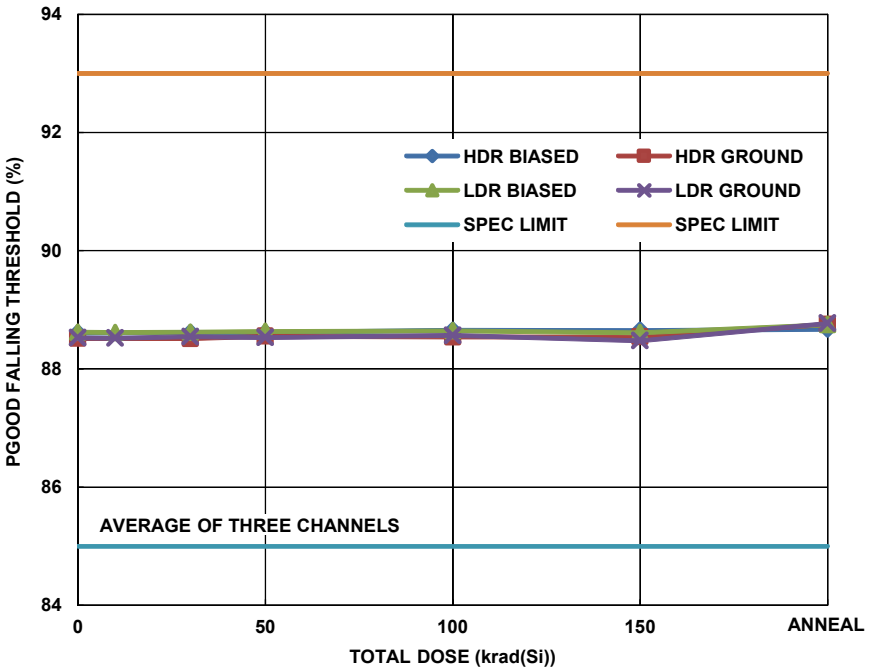

FIGURE 23. ISL70003SEH PGOOD falling threshold, average of three channels, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 85% to 93%.

Variables Data Plots (Continued)

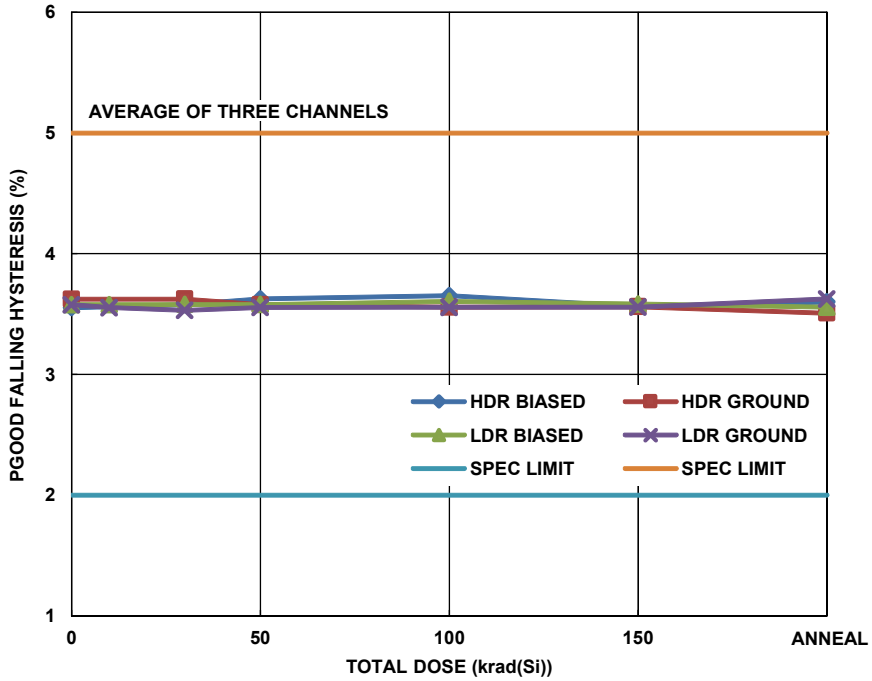

FIGURE 24. ISL70003SEH PGOOD falling hysteresis, average of three channels, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 2% to 5%.

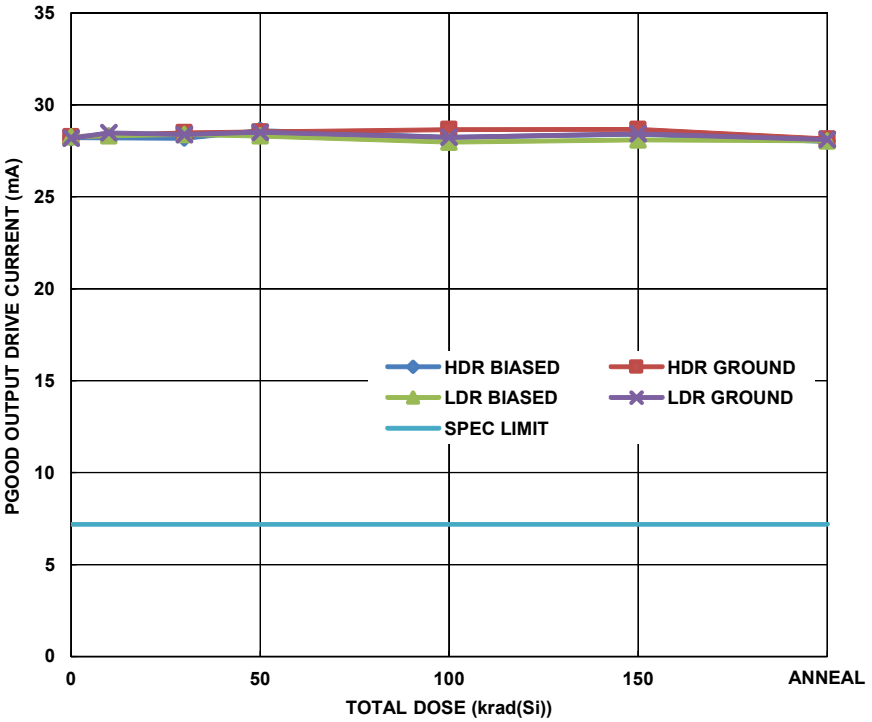

FIGURE 25. ISL70003SEH PGOOD output drive current, 3V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 7.2mA minimum.

Variables Data Plots (Continued)

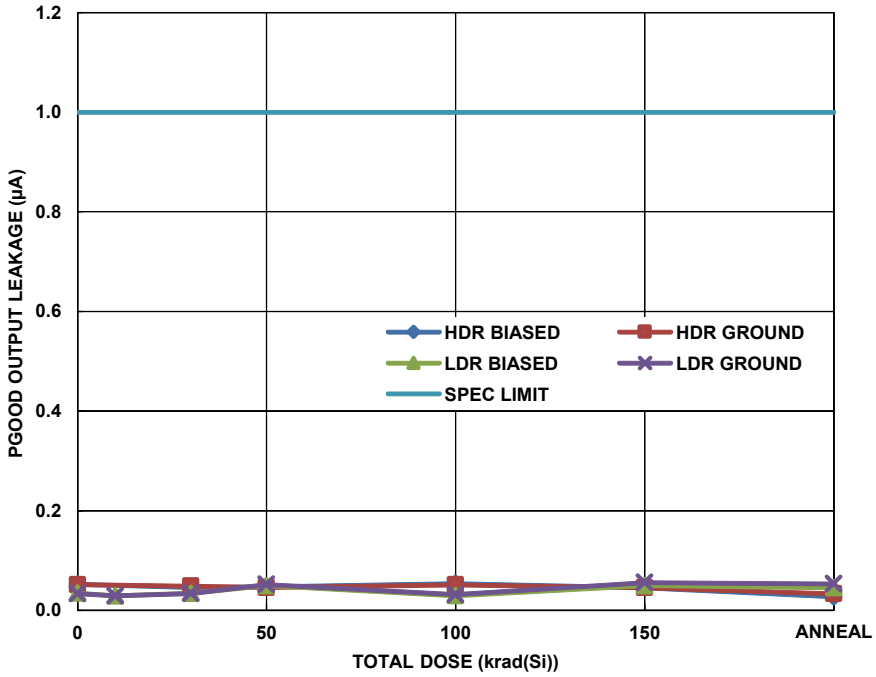

FIGURE 26. ISL70003SEH PGOOD output leakage, 13.2V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limit is 1.0µA maximum.

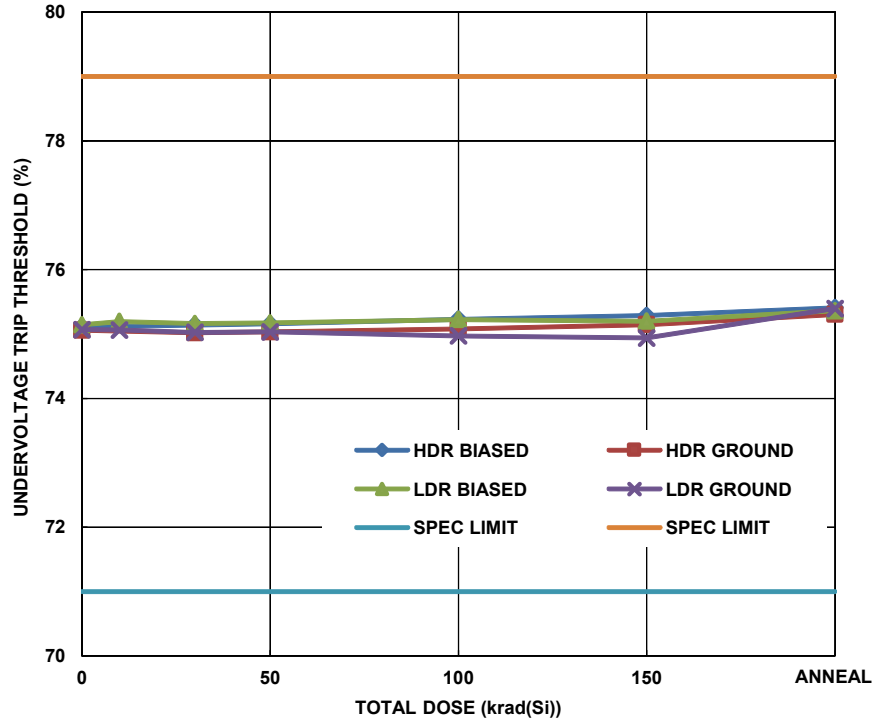

FIGURE 27. ISL70003SEH undervoltage trip threshold as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 71% to 79%.

Variables Data Plots (Continued)

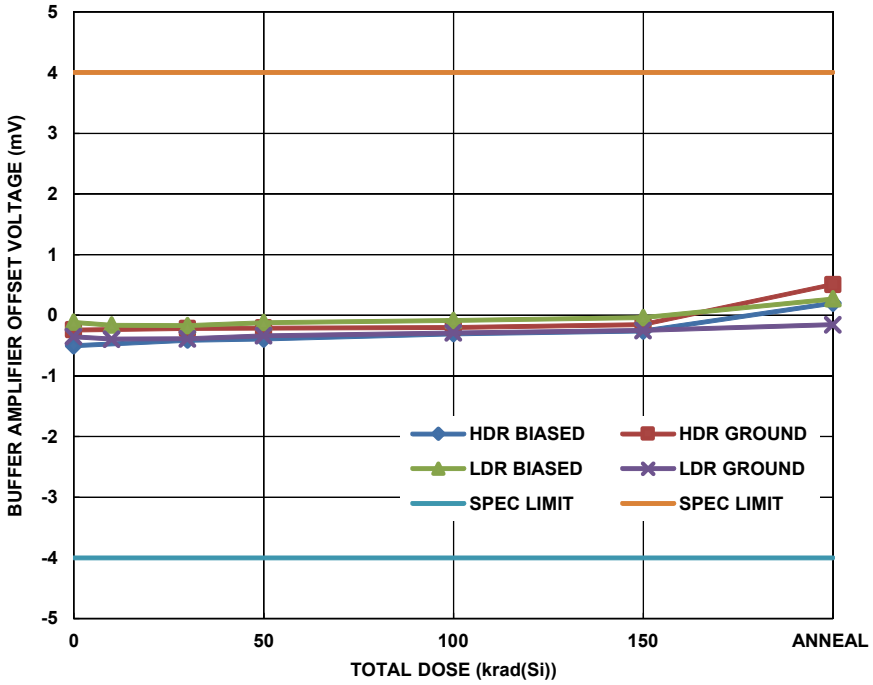

FIGURE 28. ISL70003SEH buffer amplifier input offset voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The data sheet limits are -4.0mV to 4.0mV.

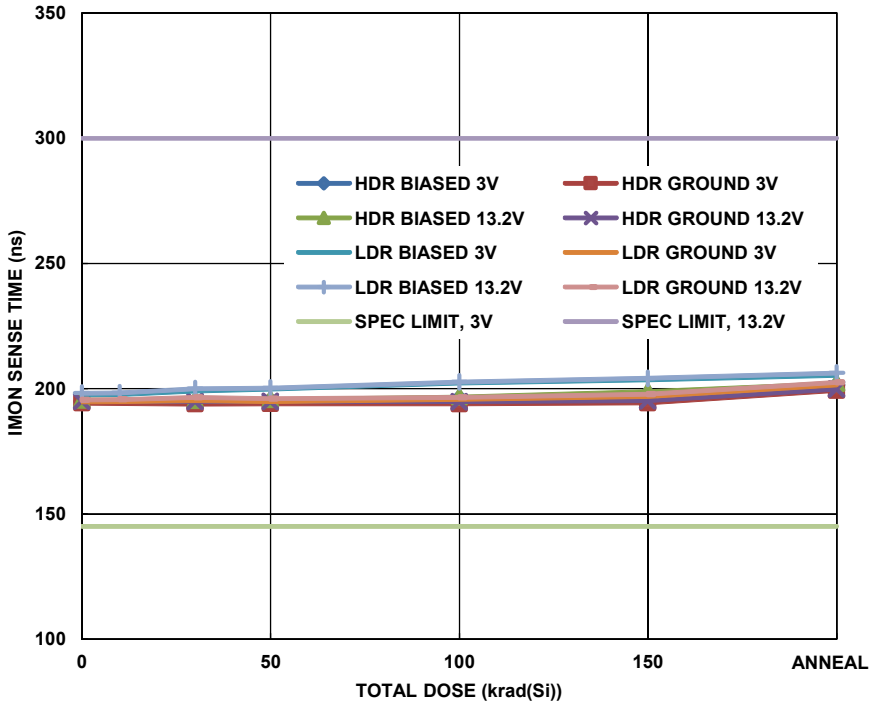

FIGURE 29. ISL70003SEH current monitor (IMON) sense time, 3V and 13.2V supply cases, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. The SMD limits are 145ns to 300ns.

Variables Data Plots (Continued)

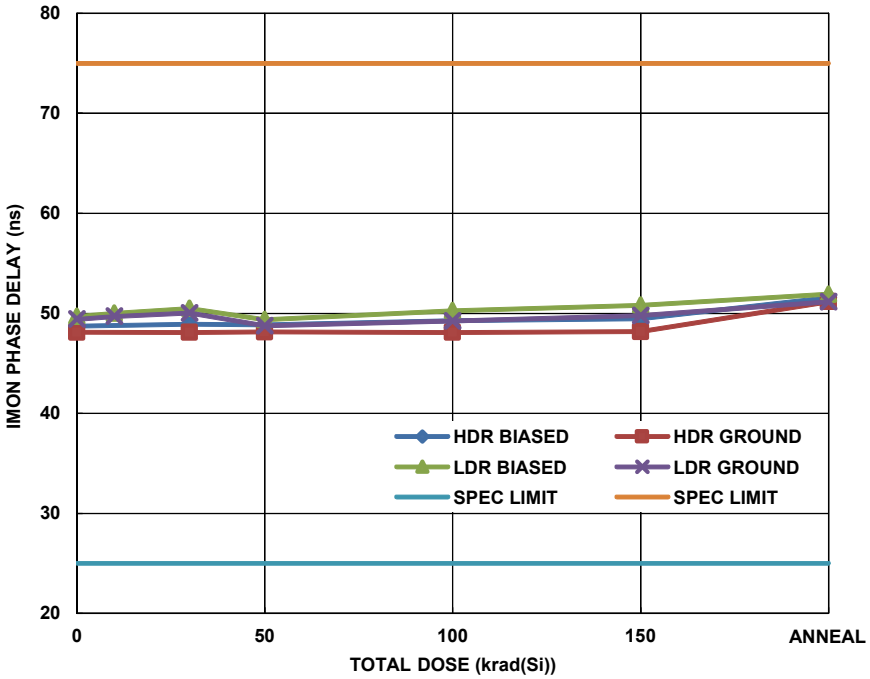

FIGURE 30. ISL70003SEH current monitor (IMON) phase delay time, 3V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The low dose rate was 0.01rad(Si)/s and the high dose rate was 64.9rad(Si)/s. Sample size for each cell was six. This is an informational parameter and is not formally specified; the ATE limits are 25ns to 75ns.

Discussion and Conclusion

This document reports the results of total dose testing of the ISL70003SEH radiation tolerant Point-Of-Load (POL) regulator. Parts were tested at low and high dose rate under biased and unbiased conditions, as outlined in MIL-STD-883 Test Method 1019, to a total dose of 150krad(Si) at high dose rate and to 150krad(Si) at low dose rate. The irradiations were followed by a biased high temperature anneal.

All samples showed excellent stability over irradiation and anneal, with no observed low dose rate sensitivity (or high dose rate sensitivity, for that matter). It should be noted that the SMD data tables contain no post-total dose limits; the pre- and post-irradiation limits are identical. This implies that the part has no dose rate sensitivity by definition, and this conclusion is fully confirmed by the data.

No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

References

[1] “Single Event Effects Testing of the ISL70003SEH, a 3V to 13.2V, 6A Synchronous Buck Regulator”, Intersil application note AN1913 (March 2015).

Appendices

Reported Parameters

FIGURE	PARAMETER	LIMIT, LOW	LIMIT, HIGH	UNITS	NOTES
2	Operating current, 500kHz	-	60.0/125.0	mA	3V and 13.2V_{IN}
3	Operating current, 300kHz	-	60.0/125.0	mA	3V and 13.2V_{IN}
4	Standby current, 500kHz	-	15.0/30.0	mA	3V and 13.2V_{IN}
5	Standby current, 300kHz	-	15.0/30.0	mA	3V and 13.2V_{IN}
6	Shutdown current, 500kHz	-	1.0/3.0	mA	3V and 13.2V_{IN}
7	Reference voltage tolerance	0.594	0.606	V	3V and 13.2V_{IN}
8	Series regulator output voltage	4.5	5.5	V	13.2V_{IN}
9	Series regulator current limit	-50.0	-190.0	mA	13.2V_{IN}
10	POR input pin voltage	0.56	0.64	V	3V and 13.2V_{IN}
11	POR sink current	9.6	14.4	mA	3V and 13.2V_{IN}
12	Enable LOW input current	-0.6	0.6	µA	13.2V_{IN}
13	Enable HIGH input current	-	10.0	µA	13.2V_{IN}
14	Minimum ON time	-	320.0	ns	3V and 13.2V_{IN}
15	Minimum OFF time	-	270.0	ns	3V and 13.2V_{IN}
16	Error amplifier input offset voltage	-3.0	3 .0	mV	3V and 13.2V_{IN}
17	Average upper device ON resistance	170	700	mΩ	3V_{IN}, average of 10 blocks
	Average upper device ON resistance	120	600	mΩ	5.5V_{IN}, average of 10 blocks
18	Average lower device ON resistance	90	455	mΩ	3V_{IN}, average of 10 blocks
	Average lower device ON resistance	60	425	mΩ	5.5V_{IN}, average of 10 blocks
19	Average LXx LOW leakage current	-	3.0	µA	3V_{IN}
20	Average LXx HIGH leakage current	-	3.0	µA	3V_{IN}
21	Average PGOOD rising threshold	107.0	115.0	%	3V_{IN}
22	Average PGOOD rising hysteresis	2.0	5.0	%	3V_{IN}
23	Average PGOOD falling threshold	85.0	93.0	%	3V_{IN}
24	Average PGOOD falling hysteresis	2.0	5.0	%	3V_{IN}
25	PGOOD output drive current	7.2	-	mA	3V_{IN}
26	PGOOD output leakage	-	1.0	µA	3V_{IN}
27	Undervoltage trip threshold	71.0	79.0	%	3V_{IN}
28	Buffer amplifier input offset voltage	-4.0	4.0	mV	3V_{IN}
29	Current monitor sense time	145.0	300.0	ns	3V_{IN}
30	Current monitor phase delay	25.0	75.0	ns	3V_{IN}

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(Rev.4.0-1 November 2017)

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