

**Separate Sheet**

**Main Specifications of the R-Car H3 SoC**

Item	R-Car H3 Specifications		
Product No	R-Car H3 (R8J77950 (SiP), R8A77950 (SoC))		
Power supply voltage	3.3/1.8 V (IO), 1.1V(LPDDR4), 0.8V (core), 2.5V (EthernetAVB)		
CPU core	ARM® Cortex™-A57 Quad	ARM® Cortex™-A53 Quad	ARM® Cortex™-R7 Dual Lock-Step
Cache memory	L1 Instruction cache: 48 KB L1 Operand cache: 32 KB L2 cache: 2 MB	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB L2 cache: 512 kB	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB
External memory	<ul style="list-style-type: none"> <li>• LPDDR4-SDRAM</li> <li>• Maximum operating frequency: 1600 MHz</li> <li>• Data bus width : 32 bits x 4 ch (12.8 GB/s x 4)</li> </ul>		
Expansion bus	PCI Express 2.0 (1 lane) x 2 ch		
Graphics	Imagination Technologies' PowerVR™ Series 6XT GX6650		
Video	Display Out x 3 ch		
	Video Input x 8 ch		
	Video codec module (H.265, H.264/AV, MPEG-4, VC-1 etc)		
	IP conversion module		
	TS Interface x 2 ch		
	stream and security processor		
	Video image processing (Up and down scaling, Dynamic this press release are trademarks or registered trademarks oresolution processing, Rotation, Visual near lossless image compression)		
Distortion compensation module x 4 ch (IMR-LSX4)			

	High performance real-time image recognition processor (IMP-X5)
Audio	Audio DSP
	Sampling rate converter x 10 ch
	Serial sound interface x 10 ch
	MOST DTCP
Storage interfaces	USB 3.0 host interface(DRD) x 1 port (wPHY)
	USB 2.0 host/function/OTG interface x 2 port (wPHY)
	SD host interface x 4 ch (SDR104)
	Multimedia card interface x 2 ch
	Serial ATA interface x 1 ch
In car network and automotive peripherals	Media local bus (MLB) Interface x 1 ch (3-pin interface)
	Controller Area Network (CAN-FD support) Interface x 2ch
	Ethernet AVB 1.0-compatible MAC built in Interface: RGMII Ethernet AVB (802.1BA)
	<ul style="list-style-type: none"> <li>• IEEE802.1BA</li> <li>• IEEE802.1AS</li> <li>• IEEE802.1Qav</li> <li>• IEEE1722</li> </ul>
Security	Crypto engine (AES, DES, Hash, RSA) x 2ch
	SystemRAM
Other peripherals	SYS-DMAC x 48 ch, Realtime-DMAC x 16 ch, Audio-DMAC x 32 ch, Audio(peripheral)-DMAC x 29 ch
	32bit timer x 26 ch
	PWM timer x 7ch
	I2C bus interface h-DMA
	Serial communication interface (SCIF) x 11 ch
	Quad serial peripheral interface (QSPI) x 2 ch (for boot, HyperFlash support)

	Clock-synchronized serial interface(MSIOF) x 4 ch (SPI/IIS)
	Ethernet controller (IEEE802.3u, RGMII, without PHY)
	Digital radio interface(DRIF) x 4 ch
	Interrupt controller (INTC)
	Clock generator (CPG) with built-in PLL
	On-chip debugger interface
Low power mode	Dynamic Power Shutdown
	AVS (Adaptive Voltage Scaling), DVFS (Dynamic Voltage and Frequency Scaling), DDR-SDRAM power supply backup mode
Package	1255-pin SiP module (42.5 mm x 42.5 mm, 0.8 mm pitch) 1384-pin Flip chip BGA (21 mm x 21 mm, 0.5 mm pitch)
Development environment	ICE for ARM CPU available from different vendors
Evaluation board	A user system development reference platform with the following features is also available to enable the users to carry out efficient system development. (1) Incorporates car information system-oriented peripheral circuits, providing users with an actual device verification environment. (2) Can be used as a software development tool for application software, etc. (3) Allows easy implementation of custom user functions.
Software Platform	Support OS: Linux, Android, QNX® Neutrino® RTOS, Integrity® etc
	OpenGL ES3.1 3D graphics library, Wide variety of H.265, H.264, MPEG-4 and VC-1 for video compliant with OpenMAX IL I/F in addition to BSPs compliant with OSs standard API are available to realize complete system concept.

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