

Separate Sheet 2

Main Product Specifications of the R-Car M3 SoC

Item	R-Car M3 Specifications			
Product No	R-Car M3 (R8J77960 (SiP), R8A77960 (SoC))			
Power supply voltage	3.3/1.8 V (IO), 1.1 V (LPDDR4), 0.9 V (core)			
CPU core	ARM® Cortex®-A57	ARM® Cortex®-A53	ARM® Cortex®-R7	
	Dual	Quad	Dual Lock-Step	
Cache memory	L1 Instruction cache:	L1 Instruction cache:	L1 Instruction cache:	
	48 KB	32 KB	32 KB	
	L1 Operand cache:	L1 Operand cache:	L1 Operand cache:	
	32 KB	32 KB	32 KB	
	L2 cache:	L2 cache:		
	1 MB	512 KB		
External memory	 LPDDR4-SDRAM Maximum operating frequency: 1600 MHz 			
	• Data bus width: 32 bits x 2 ch (12.8 GB/s x 2)			
3D Graphics	Imagination Technologies' PowerVR® Series 6XT GX6250			
Video	Display Out x 3 ch			
	Video Input x 8 ch			
	Video codec module (H.265, H.264/AV, MPEG-4, VC-1 etc.)			
	IP conversion module			
	Up and down scaling, 1-D LUT/3D-LUT/1D-Histogram/2D-Histgram,			
	color conversion, super resolution, rotate, ordered dithering,			
	sharpness, lossless compression/decompression, lossy compression			
	TS Interface x 2 ch			
	stream and security processor			
	Distortion compensation module x 4 ch (IMR-LX4)			
	High performance real-time image recognition engine (IMP-X5)			
Audio	Audio DSP			

	Sampling rate converter x 10 ch		
	Serial sound interface x 10 ch		
Storage interfaces	USB 3.0 host interface(DRD) x 1 port (wPHY)		
	USB 2.0 host interface x 1 port (wPHY)		
	USB 2.0 host/function/OTG interface x 1 port (wPHY)		
	SD host interface x 4 ch (SDR104)		
	Multimedia card interface x 2 ch		
	PCI Express 2.0 (1 lane) x 2 ch		
In car network and automotive	Media local bus (MLB) Interface x 1 ch (3-pin interface)		
	controller area network (CAN-FD support) Interface x 2ch		
	Ethernet AVB 1.0-compatible MAC built in		
	Interface: RGMII		
	Ethernet AVB (802.1BA)		
peripherals	● IEEE802.1BA		
	IEEE802.1AS		
	IEEE802.1Qav		
	• IEEE1722		
Security	Crypto engine (AES, DES, Hash, RSA) x 2ch		
	SystemRAM		
	SYS-DMAC x 48 ch, Realtime-DMAC x 16 ch,		
	Audio-DMAC x 32 ch, Audio(peripheral)-DMAC x 58 ch		
	32bit timer x 41 ch		
Other peripherals	PWM timer x 7 ch		
	I2C bus interface x 8 ch		
	Serial communication interface (SCIF) x 11 ch		
	SPI multi I/O bus controller (RPC) x 1 ch (HyperFlash™/QSPI support)		
	Clock-synchronized serial interface(MSIOF) x 4 ch (SPI/IIS)		
	Digital radio interface(DRIF) x 4 ch		
	Dynamic Power Shutdown		
Low power mode	AVS (Adaptive Voltage Scaling), DVFS (Dynamic Voltage and Frequency Scaling), DDR-SDRAM power supply backup mode		

Package	1255-pin SiP module (40 mm x 40 mm, 0.8 mm pitch)		
	1022- pin Flip chip BGA (29 mm x 29 mm, 0.8 mm pitch)		
Development	ICE for ARM CPU available from tool vendors		
environment			
Evaluation board	A user system development reference platform with the following		
	features is also available to enable the users to carry out efficient		
	system development.		
	(1) Incorporates car information system-oriented peripheral circuits,		
	providing users with an actual device verification environment.		
	(2) Can be used as a software development tool for application		
	software, etc.		
	(3) Allows easy implementation of custom user functions.		
Software Platform	Support OS: Linux, Android, QNX® Neutrino® RTOS, Integrity® etc.		
	OpenGL ES3.1 3D graphics library, Wide variety of H.265, H.264,		
	MPEG-4 and VC-1 for video compliant with OpenMAX IL I/F in		
	addition to BSPs compliant with OSs standard API are available to		
	realize complete system concept.		

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