

Clock Data Recovery Device

894D115i-01/-04

SECURE SUPPLY: IDT CLOCK DATA RECOVERY SOLUTION FOR THE INDUSTRY-STANDARD VSC8115 DEVICE IS NOW FULLY AVAILABLE IN PRODUCTION QUANTITIES.

TYPICAL APPLICATIONS:

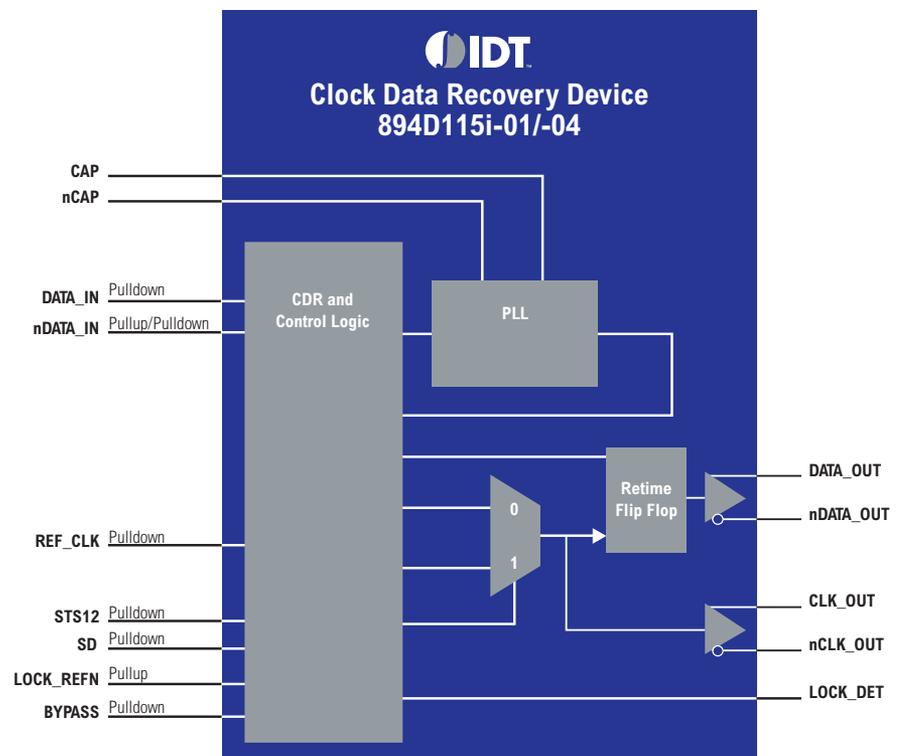
- Clock and data recovery of STM-1/-4 (OC-3/-12) data streams
- Wireless infrastructure; transport and backhaul
- Wired communication
- Line cards with electro-optical interface
- Core switches and ADM equipment

Description

Clock and data recovery (CDR) circuits are designed to extract the clock signal from NRZ-coded input data signals. The device input accepts 622.08 or 155.52 MBit/s data signals. The output signals of the device are the recovered clock and retimed data signals. An internal phased locked loop (PLL) is used for clock generation and recovery. An external clock input establishes an initial operating frequency for the clock recovery PLL and provides a clock reference in the absence of serial input data.

The CDR circuit uses differential inputs and outputs to support high clock and data rates for the best signal integrity. All control inputs and outputs are single-ended signals. The device supports a signal detect input and a lock detect output to facilitate interfacing with electro-optical modules. The 894D115i-01/-04 is pin and function compatible with the Vitesse VSC8115. The IDT CDR device family is released to production and fully available.

Block Diagram



Features chart

- Clock recovery for STM-4 (OC-12/STS-12) and STM-1 (OC-3/STS-3)
- Input: NRZ data (622.08 or 155.52 Mbit/s)
- Output: clock signal (622.08 MHz or 155.52 MHz) and retimed data signal at 622.08 or 155.52 Mbit/s
- Internal PLL for clock generation and clock recovery
- Differential inputs can accept LVDS and LVPECL levels
- Differential data and clock outputs
- Lock reference input and PLL lock output
- 19.44 MHz reference clock input
- Full 3.3V supply mode
- -40°C to 85°C operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Comparative specification chart for CDR devices

Part number	Description	Data input	Data and clock outputs	Package
894D115Bgi-01LF	STM-1/-4 (OC-3/-12) CDR	Differential	LVPECL	20-TSSOP
894D115AGi-04LF	STM-1/-4 (OC-3/-12) CDR	Differential	LVDS	20-TSSOP

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