Device Overview

The 89HPES34H16 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES34H16 is a 34-lane, 16-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high-performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to fifteen downstream ports and supports switching between downstream ports.

Utilizing standard PCI Express interconnect, the PES34H16 provides the most efficient I/O connectivity for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES34H16 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers. The PES34H16 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity.

Features

- ◆ High Performance PCI Express Switch
  - – *Sixteen maximum switch ports*
    - • Up to three x8 ports that bifurcate up to six x4 ports
    - • Ten x1 ports
  - – *Thirty-four 2.5 Gbps embedded SerDes*
    - • Supports pre-emphasis and receive equalization on per-port basis
  - – *Low-latency cut-through switch architecture*
  - – *Support for Max Payload Size up to 2048 bytes*
  - – *Supports two virtual channels and eight traffic classes*
  - – *PCI Express Base Specification Revision 1.1 compliant*
- ◆ Flexible Architecture with Numerous Configuration Options
  - – *Port arbitration schemes utilizing round robin algorithms*
  - – *Automatic per port link width negotiation from x8 to x4 to x2 or x1*
  - – *Automatic lane reversal on all ports*
  - – *Automatic polarity inversion on all lanes*
  - – *Supports locked transactions, allowing use with legacy software*
  - – *Ability to load device configuration from serial EEPROM*
  - – *Ability to control device via SMBus*

- ◆ Highly Integrated Solution
  - – *Requires no external components*
  - – *Incorporates on-chip internal memory for packet buffering and queueing*
  - – *Integrates thirty-four 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- ◆ Reliability, Availability, and Serviceability (RAS) Features
  - – *Redundant upstream port failover capability*
  - – *Supports optional PCI Express end-to-end CRC checking*
  - – *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - – *Supports optional PCI Express Advanced Error Reporting*
  - – *Supports PCI Express Hot-Plug*
    - • Compatible with Hot-Plug I/O expanders used on PC motherboards
  - – *Supports Hot-Swap*
- ◆ Power Management
  - – *Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)*
    - • Supports powerdown modes at the link level (L0, L0s, L1, L2/L3 Ready and L3) and at the device level (D0, $D3_{hot}$)
  - – *Unused SerDes disabled*
- ◆ Testability and Debug Features
  - – *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - – *Ability to read and write any internal register via the SMBus*
  - – *Ability to bypass link training and force any link into any mode*
  - – *Provides statistics and performance counters*
- ◆ Thirty-two General Purpose Input/Output pins
  - – *Each pin may be individually configured as an input or output*
  - – *Each pin may be individually configured as an interrupt input*
  - – *Some pins have selectable alternate functions*
- ◆ Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing

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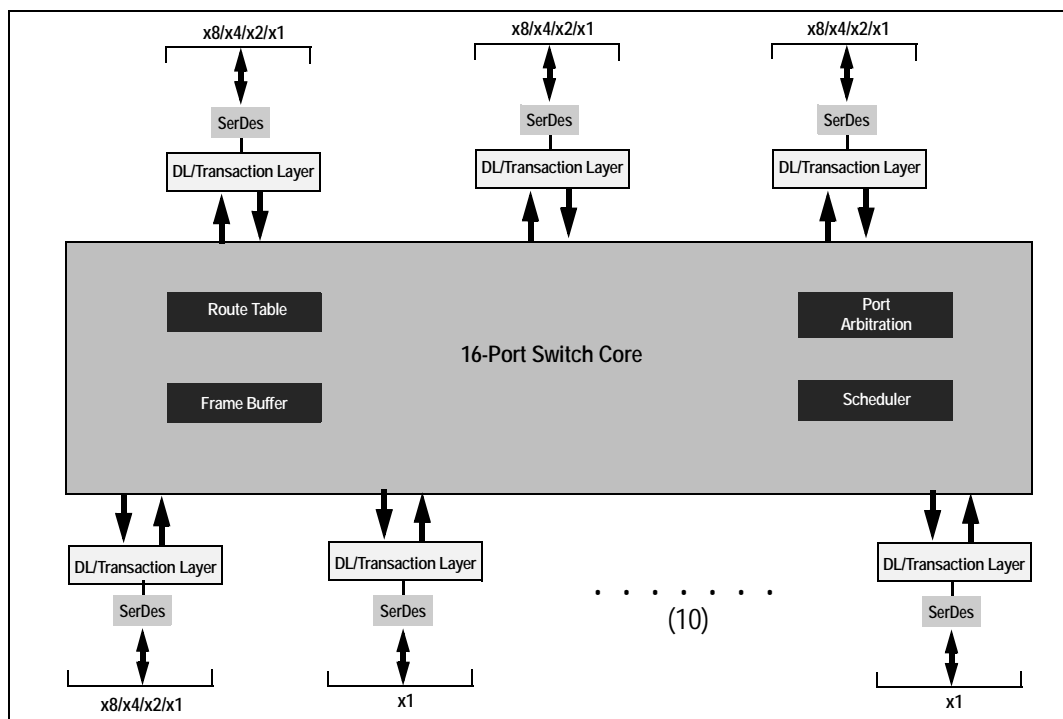
Block Diagram

34 PCI Express Lanes
Up to 6 x4 ports and 10 x1 Ports

Figure 1 PES34H16 Block Diagram

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