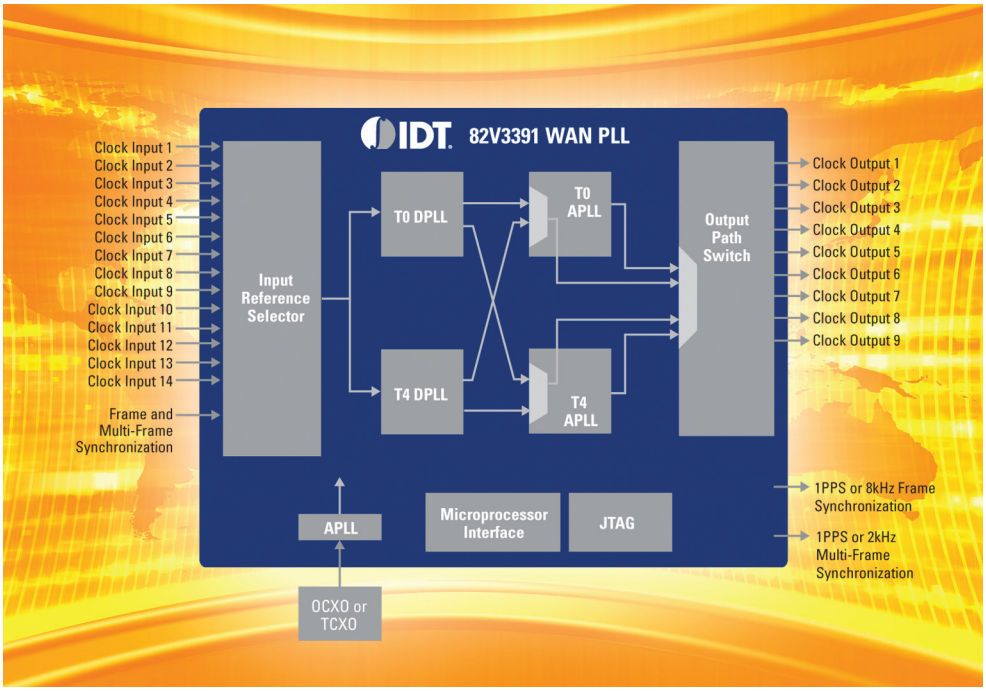
IDT 82V3391
Synchronous Ethernet WAN PLL

FEATURES AND BENEFITS

- Single chip timing source
- Low jitter outputs for synchronous Ethernet and SONET/SDH clocks
- 1 PPS input and output options
- Automatic hitless switching with less than 0.61ns transient
- Aligns outputs to reference input phase with offset control
- Programmable loop bandwidth and damping factor
- Precise hold-over
- 14 input clocks and 9 output clocks
- Input reference frequencies from 1 PPS to 644.53125 MHz
- Single ended CMOS and PECL/LVDS inputs and outputs
- Composite clock reference input and output
- BITS/SSU clock input and output
- Automatic switching between free-run, locked and holdover
- Frame synchronization inputs and outputs
- Master clock calibration
- Automatic master/slave switching mechanism for redundant clock applications
- I²C, SPI, parallel microprocessor interface or EPROM control
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3V operation with 5V tolerant CMOS I/Os
- 100-pin TQFP package

APPLICATIONS

- 2G, 3G and 4G wireless backhaul
- Carrier Ethernet transport
- Service provider core and access switches
- Internet, enterprise and service provider routers
- DWDM and ROADM cross-connect and transmission equipment
- OTN client muxponders and transponders
- Central office and remote central office timing distribution
- Broadband xDSL and multi-service access equipment



Device Overview

The IDT 82V3391 is an integrated timing source for Stratum 3, Stratum 4E, Stratum 4, SMC, EEC-Option 1 and EEC-Option 2 clocks. Systems use IDT 82V3391 for synchronization of broadband wireline access, SONET, SDH, synchronous Ethernet, optical transport and wireless. A typical application receives as input one or more clock sources: clocks recovered from synchronous Ethernet, optical TDM and PDH data interfaces; centralized timing sources such as GPS; network time protocol using IP; precision time protocol version 2 using IEEE 1588 or IEEE 802.1AS.

The device fully supports the synchronous equipment timing source T0 and T4 paths for SDH, SONET and synchronous Ethernet described in ITU-T standards. The T0 path provides a high performance and highly configurable system clock. The T4 path is a simpler, fixed path that may be used as a timing source for legacy BITS and SSU equipment.

Each IDT 82V3391 timing path automatically or manually selects inputs and switches automatically or manually between free-run, locked and holdover modes. Two independent digital PLLs provide stable performance under varying operating environments independent of silicon process variations, while two high performance analog PLLs provide low jitter SONET and Ethernet clock outputs.

An external master clock provides enhanced performance or low overall cost depending on the holdover and free-run performance required. Whichever master clock oscillator is chosen, the IDT 82V3391 can calibrate the ppm frequency of the master clock.

Access to read and write registers is through a standard microprocessor interface including I²C, SPI, parallel microprocessor interface or EPROM control. The registers optionally provide real time control of both digitally controlled oscillators and make available direct-write frequency synthesis to system software. The IDT 82V3391 supports Master/Slave operation so that two devices, running in different system boards, work together to provide the dual redundant clock paths needed by system processors and line cards.

Synchronous Ethernet

TDM SONET/SDH and PDH networks transport timing information and the IDT 82V3391 provides the Synchronous Equipment Timing Source (SETS) for these applications. Newer standards allow network providers to use similar techniques for clock synchronization over Ethernet. The IDT 82V3391 is configured through a control interface such as I^2C for compliance with the ITU-T G.8262 synchronous Ethernet equipment clock (EEC).

1 PPS Timing Reference

Wireless networks require synchronization (operation at the same phase), as well as syntonization (operation at the same frequencies). 1 PPS reference pulses indicate and track the network phase reference independently of frequency. The IDT 82V3391 can receive a 1 PPS signal as input and can generate a 1 PPS output.

Global Positioning System (GPS) Reference

GPS receivers accurately recover the network primary clock reference. Combined with a local, stable frequency reference, GPS based timing references achieve sub microsecond accuracy. The IDT 82V3391 can synchronize to both the 10MHz clock and 1 PPS reference generated by GPS receivers.

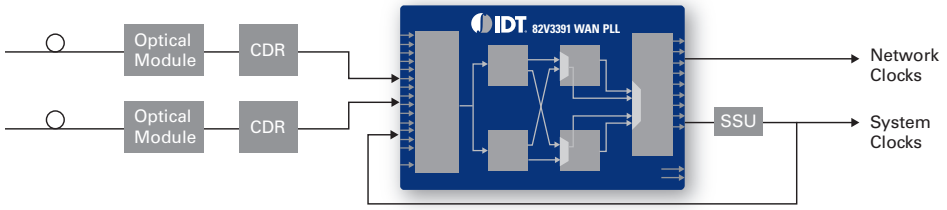
Direct-Write Digitally Controlled Oscillator

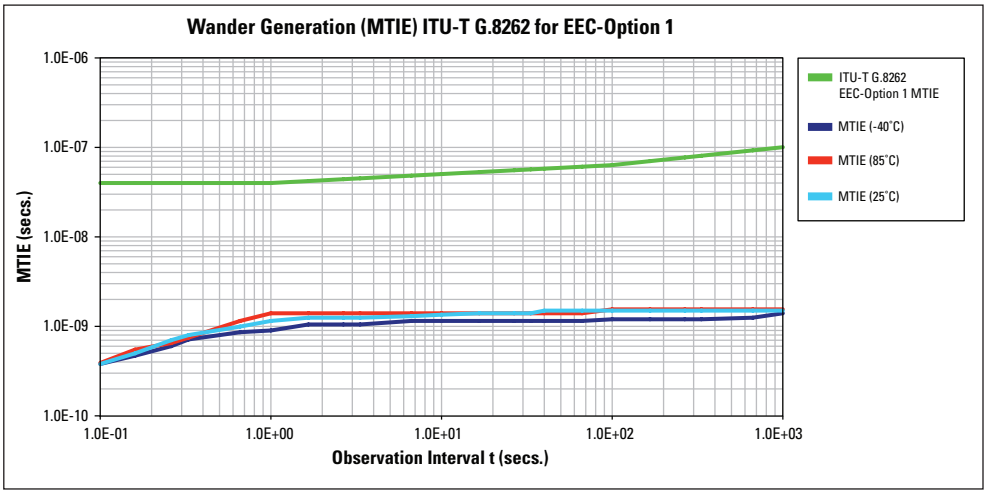
As an option, system software may need to control the frequency and phase of output clocks. In packet timing applications having no input reference clock or when the input reference clock is unavailable, the system may determine the output clock frequency and phase offset by writing to registers in the IDT 82V3391.

Redundant Clock Sources Using Two IDT 82V3391

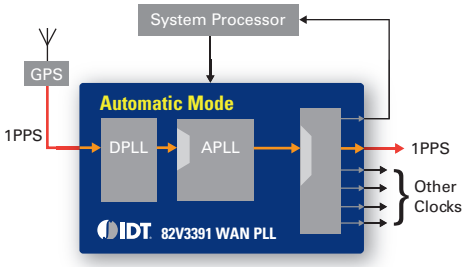
Where network redundancy is used to provide multiple reference clocks, a single IDT 82V3391 can automatically select an alternative input when one or more inputs fail. A single point of failure is avoided by providing the same set of input references to two IDT 82V3391 devices located on different boards and connected together using their master/slave interfaces. The corresponding two sets of outputs are identical in frequency and phase. If one of the timing boards fails or is removed for maintenance, the system remains locked to the corresponding output from the other board without disturbance.

Synchronous Ethernet Application

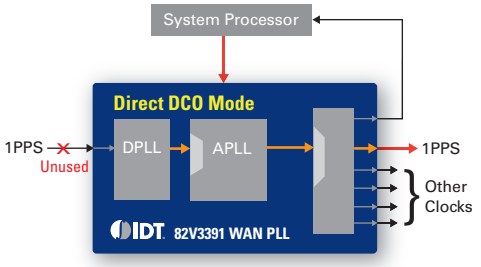




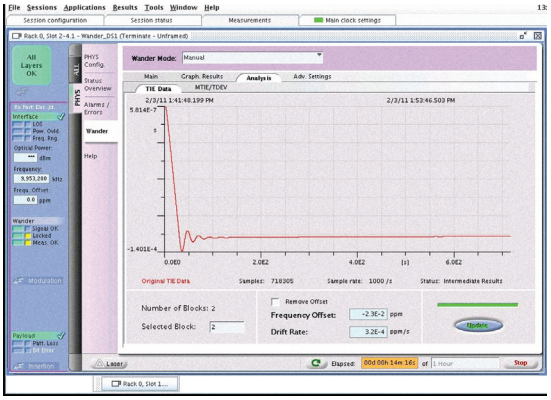
1 PPS Reference Application



1 PPS Input Reference Option



System Processor Controlled 1 PPS Reference



Data collection using JDSU ONT-506 at room temperature showing 1PPS lock time from free run mode. The fast lock feature provides a lock time of around 100 seconds.