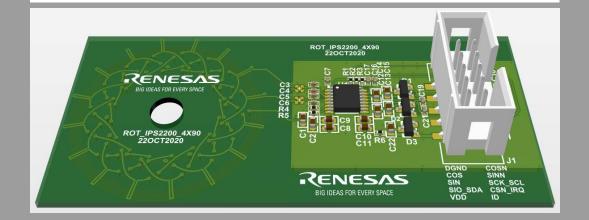
# INDUCTIVE POSITION SENSOR (IPS) DESIGN GUIDELINES

2021-03-08
RENESAS ELECTRONICS CORPORATION

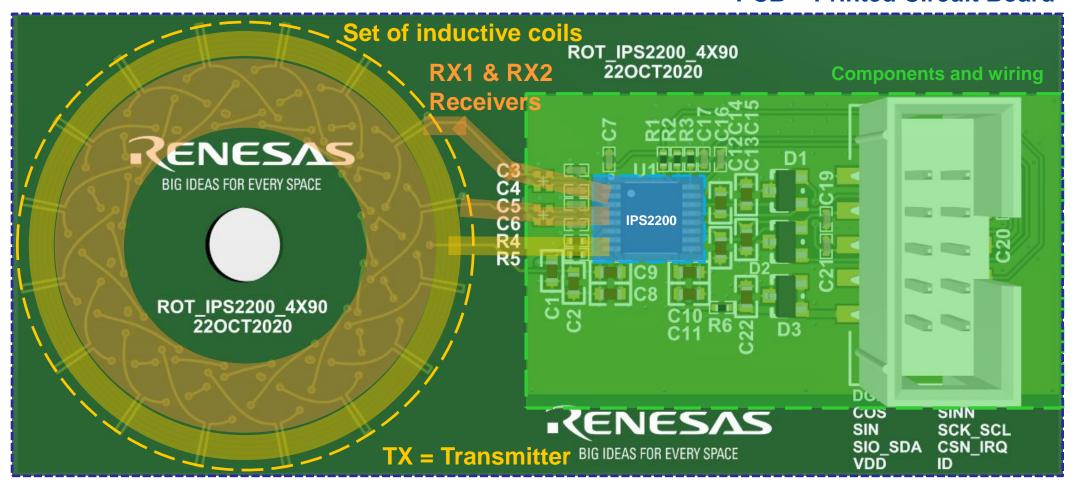


#### **CONTENTS**

- Introduction
  - What is an IPS design?
  - Tools for design generation
- Working with custom generated coils (ICOT)
  - How to import and adjust Gerber data?
  - How to export Gerber to PCB?
  - Design hints Altium Designer
- Working with templates
  - How to obtain the templates?
  - How to connect the sensor coils?
  - Basic EMC recommendations
  - PCB Target design

# WHAT IS AN IPS DESIGN?

#### **PCB = Printed Circuit Board**



# **TOOLS FOR DESIGN GENERATION**

**Catalog Design** ☑ Optimized Sensor Coils ROT\_IPS2200\_4X90 **ICOT** 22OCT2020 **Inductive Coil** ☑ Sensor PCB **Optimization Tool** ☑ Gerber Files ENESAS ☑ Optimized Sensor Coils BIG IDEAS FOR EVERY SPACE ☑ Design Documentation ☑ Gerber Files IPS2200 ☑ Measurement Report ☑ Simulation Results ☑ 3 Air Gap Variations **WEBINAR** ROT\_IPS 22OC **Best Design Practices PCB** Design **TEMPLATES** ☑ Training Video IESAS ☑ Schematic Design with EMC Components ☑ How to import Gerber S FOR EVERY SPACE ☑ Fully placed and wired PCB Design ☑ How to connect Coils ☑ Gerber Files ☑ Design Hints https://www.renesas.com/buy-sample/locations ☑ Full Altium Project ☑ Good and Bad Examples https://www.renesas.com/products/sensor-products/position-sensors

**CRB** 

#### **HOW TO IMPORT GERBER?**

☑ Gerber Files of Optimized Sensor Coils



Save and unpack ZIP container

Dear User.

Your coil design optimization results are attached in the email.

Please send an email to "Teamsupport@coildesign" if any questions.

Send the legal disclaimer as a PDF to the customer upfront.

The Legal Disclaimer can be found on Seismic as "Renesas Inductive Position Sen

Do not deliver the results and the Gerber files without the customer acknowledging Attach the disclaimer again when the results and the Gerber files are sent.

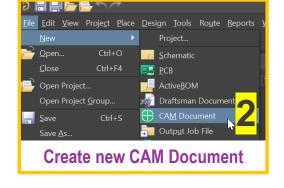
Note

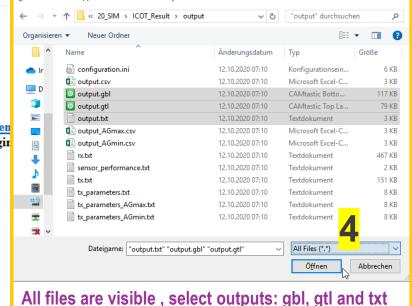
The attached ZIP file is encrypted with you user password.

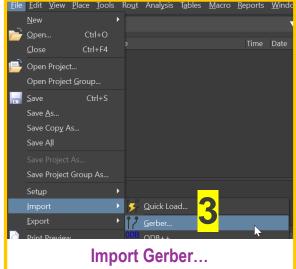
Regards,

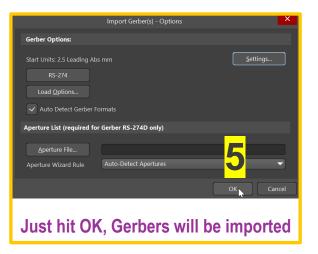
AASBD Apps support team

NB: This is a generated email please do not reply.



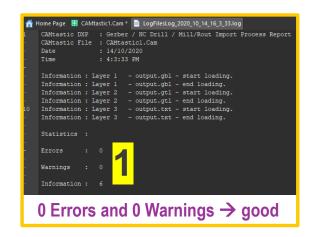


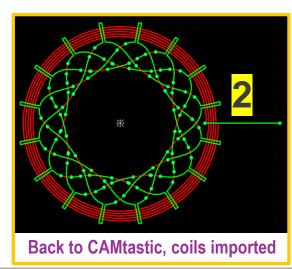


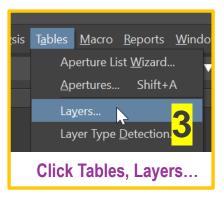


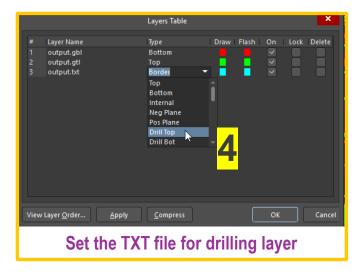
Select Gerber File(s) - use Shift or Ctrl for multiple files

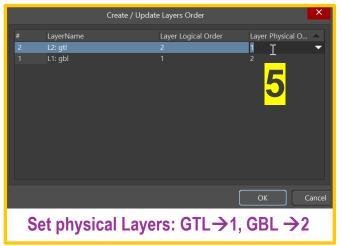
# **HOW TO SET THE LAYERS?**





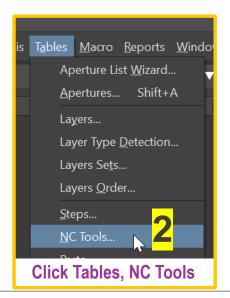


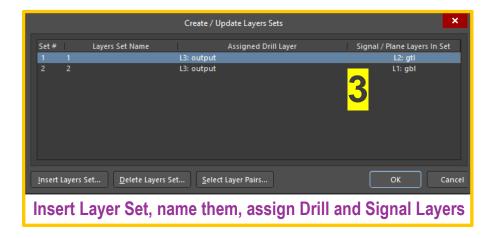


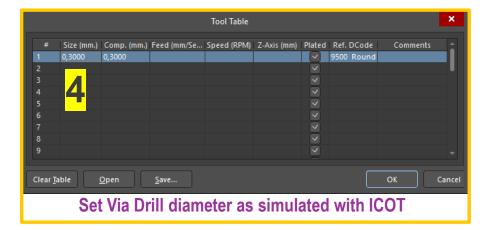


# **HOW TO SET THE VIAS?**

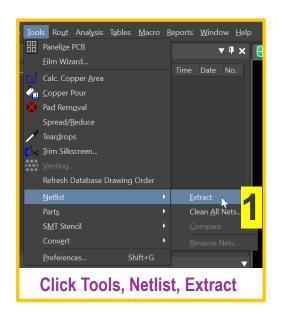


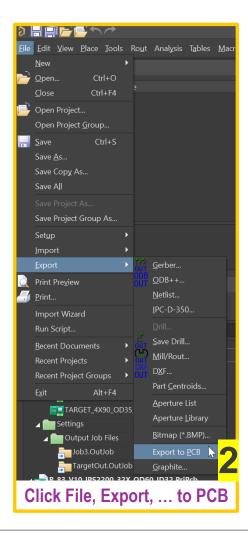


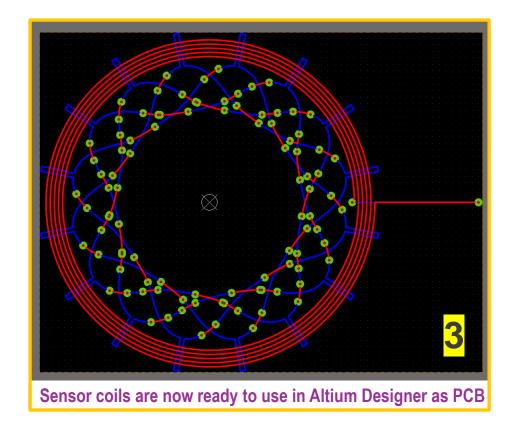




# **HOW TO EXPORT TO PCB?**



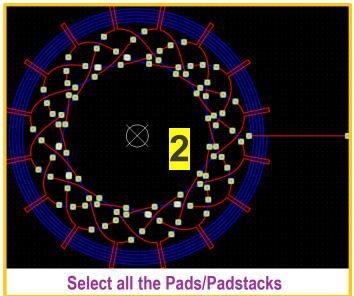


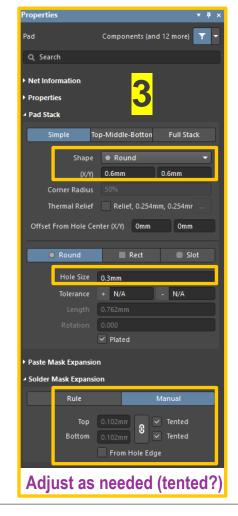


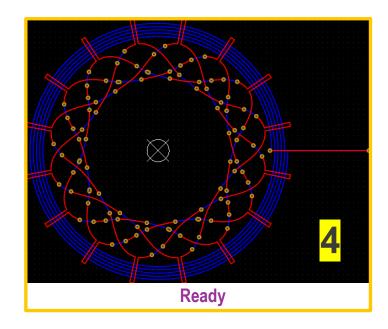


# **DESIGN HINT FOR ADJUSTING VIAS**



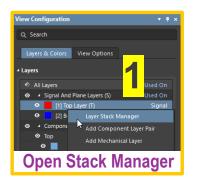








# **DESIGN HINT FOR SHIFTING LAYERS**

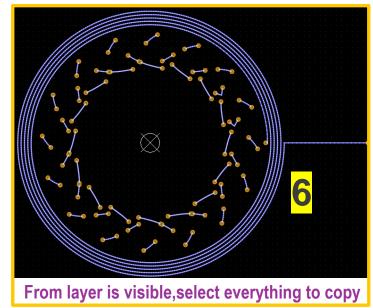






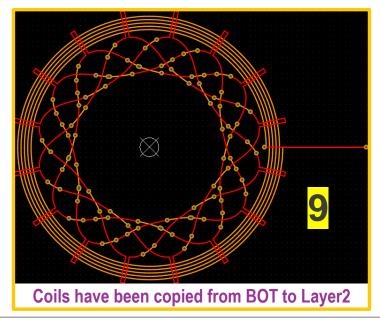










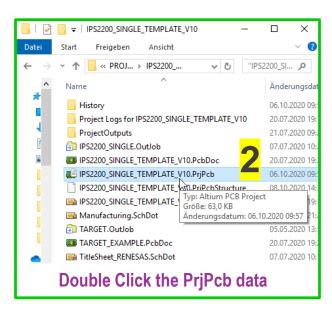


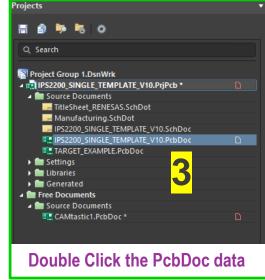


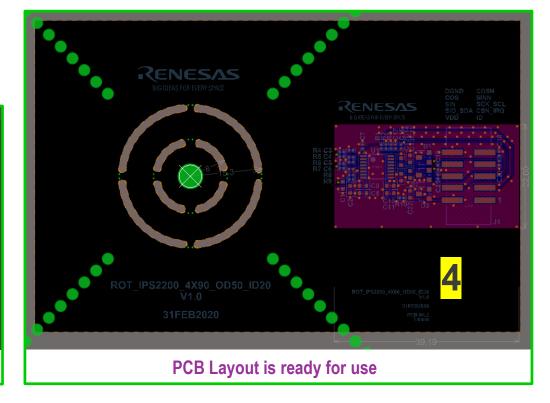
# **HOW TO OPEN THE TEMPLATE?**

☑ Download Templates – Altium Project Files







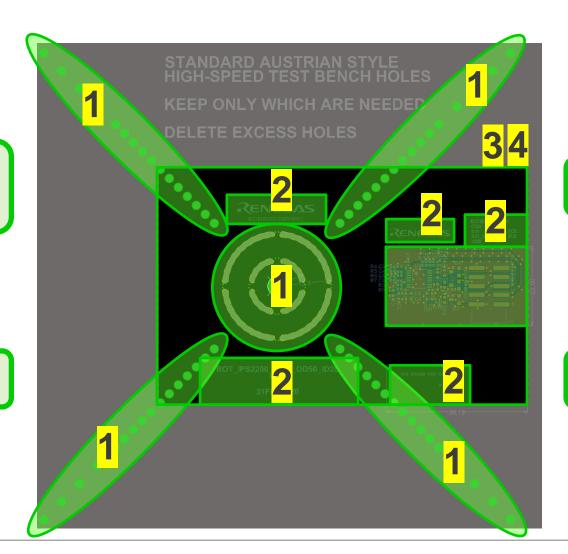


# **HOW TO ADJUST THE TEMPLATE?**

☑ Remove unused Mounting Holes

☑ Or add/adjust as needed

☑ Remove/adjust Text, Logo, etc. 2



☑ Adjust Board Shape freely

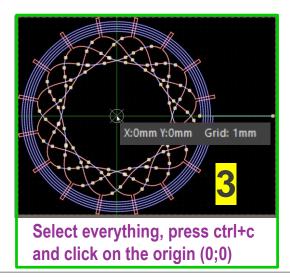
☑ Adjust Layer Stack

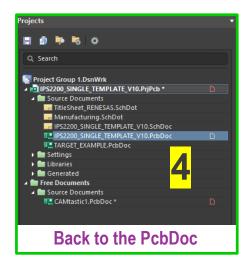
4

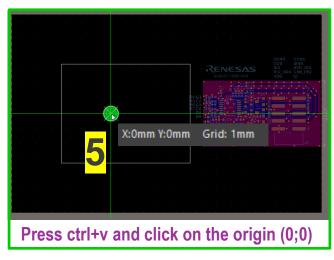
# **HOW TO COPY/PASTE THE COILS?**

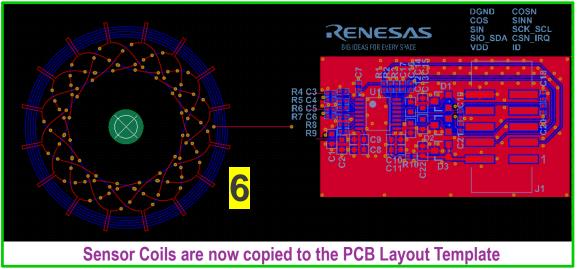






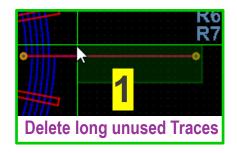


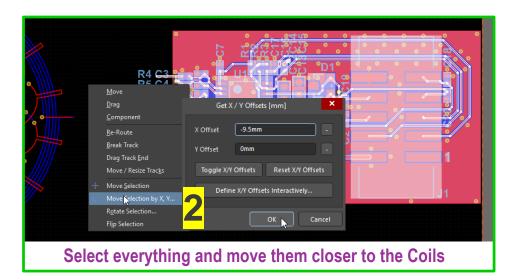






# DESIGN HINT FOR COMPACTING THE BOARD



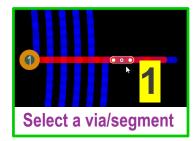


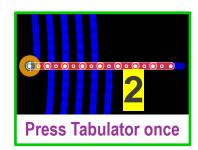
To eliminate the unwanted influence of large metallic objects:

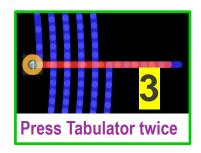
☑ Keep 3mm minimum distance from copper planes to the coils!

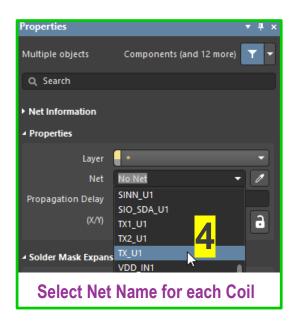
☑ Keep **5mm** or larger safety distance if your design lets you!

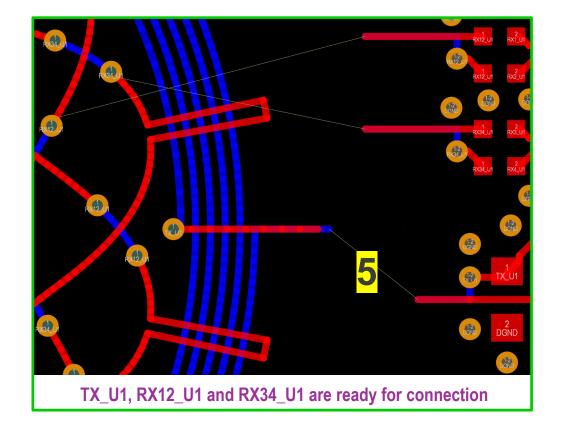
# **HOW TO RENAME THE COILS?**



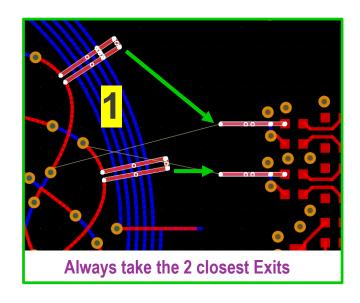








# **HOW TO CONNECT THE COILS?**

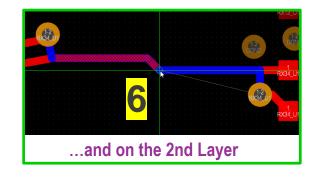


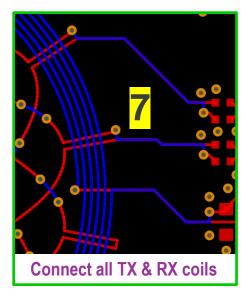










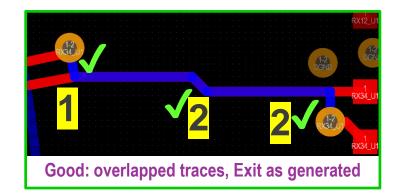


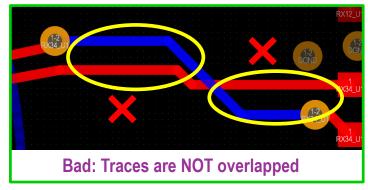


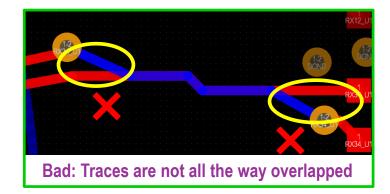
# DESIGN HINT FOR COIL ROUTING

To eliminate the unwanted influence of bad wiring:

- ☑ Always use the Exits as simulated
- ☑ Always route the Coils overlapped on neighboring Layers!
  - ☑ Don 't change the Renesas Layout Template



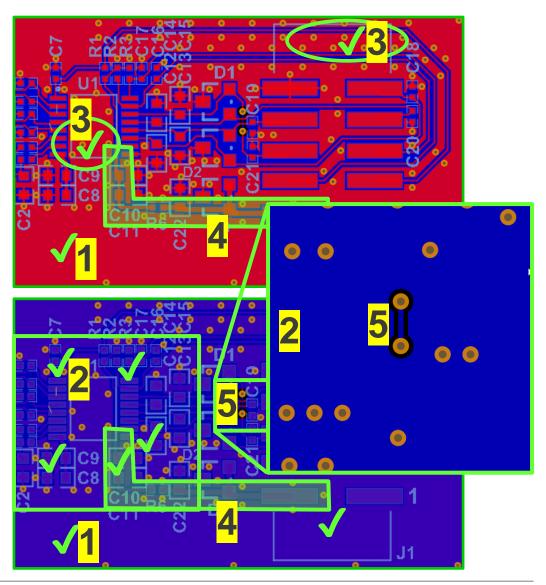




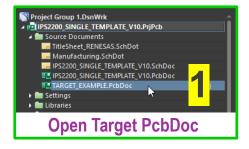


# **DESIGN HINT FOR GND PLANES**

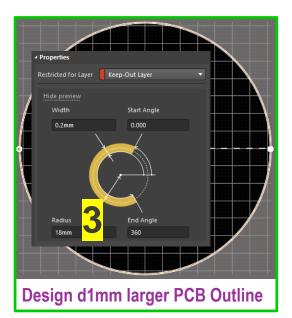
- ☑ Always fill all the Copper Layers with GND Planes
- ☑ Have at least one fully filled GND Layer below IPS2200
- ☑ Use GND Vias to connect the Layers on every 1-2mm
- ☑ Consider return Current Paths especially for VDD Supply
- ☑ Only very short Tracks are allowed on GND Layer

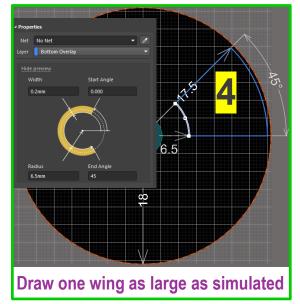


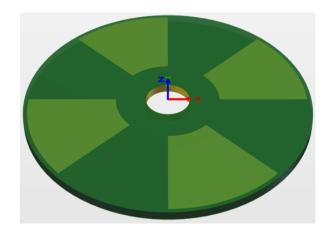
# **HOW TO DESIGN A PCB TARGET?**

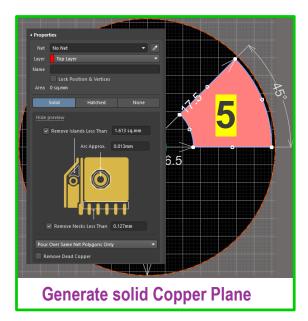


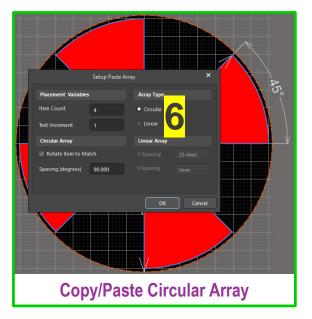








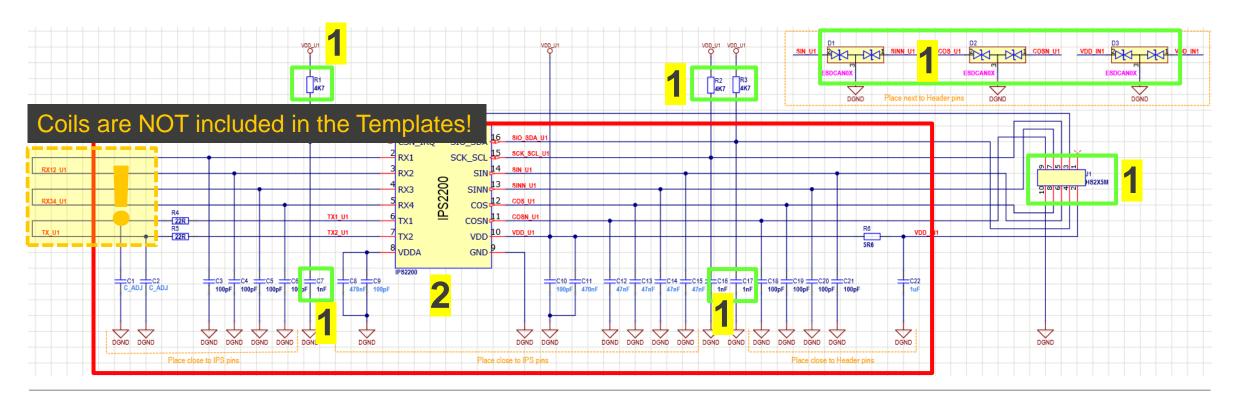




# **IPS2200 SCHEMATIC TEMPLATES**

Remove Components if unused or change them freely to your needs!

We advise NOT to change the rest of the schematic!



# THANK YOU FOR YOUR ATTENTION!