Tsi578 Ballmap (Document number 80B803A_PN003_04)
Note: This is the ballmap when looking through the top of the package. This ballmap represents the PCB footprint for the Tsi578.

Note: 11	ils is the ba	ilimap wiei 2	3	d 4	op or the pa 5	6	balimap re 7	presents tri 8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	NO_BALL	VSS	VSS	VSS	VSS	VSS	SP14_TD_P	VSS	SP14_TC_N	VSS	SP14_TB_P	VSS	SP14_TA_N	VSS	SP6_TD_P	VSS	SP6_TC_ N	VSS	SP6_TB_P	VSS	SP6_TA_N	VSS	VSS	VSS	VSS	VSS
В	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP14_TD_N	VSS	SP14_TC_P	SP_VDD	SP14_TB_N	VSS	SP14_TA_P	SP_VDD	SP6_TD_ N	VSS	SP6_TC_P	SP_VDD	SP6_TB_N	VSS	SP6_TA_P	SP_VDD	VSS	S_CLK_P	S_CLK_N	VSS
С	SP0_TA_N	SP0_TA_P	SP_VDD	SPO_RA_P	SPO_RA_N	SP_VDD	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	REF_AVDD	VSS	REF_AVDD
D	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP14_RD_N	VSS	SP14_RC_P	SP14_REXT	SP14_RB_N	VSS	SP14_RA_P	VSS	SP6_RD_ N	VSS	SP6_RC_ P	SP6_REX T	SP6_RB_ N	VSS	SP6_RA_P	VSS	VSS	VSS	VSS	VSS
E	SP0_TB_P	SP0_TB_N	SP_VDD	SPO_RB_N	SP0_RB_P	SP_VDD	SP14_RD_P	SP14_AVDD	SP14_RC_N	SP14_AVDD	SP14_RB_P	SP_VDD	SP14_RA_N	VSS	SP6_RD_ P	SP6_AVD D	SP6_RC_ N	SP6_AVD D	SP6_RB_P	SP_VDD	SP6_RA_ N	VSS	VSS	VSS	VSS	VSS
F	VSS	SP_VDD	VSS	SP0_REXT	SP0_AVDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS
G	SP0_TC_N	SP0_TC_P	SP_VDD	SP0_RC_P	SP0_RC_N	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP_VDD	SP12_RD_P	SP12_RD_N	SP_VDD	SP12_TD_N	SP12_TD_P
н	VSS	VSS	VSS	VSS	SP0_AVDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP12_AVDD	VSS	VSS	VSS	VSS
J	SP0_TD_P	SP0_TD_N	SP_VDD	SPO_RD_N	SP0_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RC_N	SP12_RC_P	SP_VDD	SP12_TC_P	SP12_TC_N
к	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP_VDD	VSS	VDD	VSS	V00	VSS	VDĐ	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	SP12_AVDD	SP12_REXT	VSS	SP_VDD	VSS
L	SP8_TA_N	SP8_TA_P	SP_VDD	SP8_RA_P	SP8_RA_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RB_P	SP12_RB_N	SP_VDD	SP12_TB_N	SP12_TB_P
М	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	VDD	VSS	V00	VSS	VDĐ	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS
N	SP8_TB_P	SP8_TB_N	SP_VDD	SP8_RB_N	SP8_RB_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP12_RA_N	SP12_RA_P	SP_VDD	SP12_TA_P	SP12_TA_N
Р	VSS	SP_VDD	VSS	SP8_REXT	SP8_AVDD	VSS	SP_VDD	VSS	VED	VSS	VDD	VSS	VDD	VSS	VDB	VSS	VDB	VSS	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP_VDD	VSS
R	SP8_TC_N	SP8_TC_P	SP_VDD	SP8_RC_P	SP8_RC_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	SP4_RD_ P	SP4_RD_ N	SP_VDD	SP4_TD_ N	SP4_TD_P
т	VSS	VSS	VSS	VSS	SP8_AVDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	12C_SA[0]	SP_VDD	VSS	SP4_AVD D	VSS	VSS	VSS	VSS
U	SP8_TD_P	SP8_TD_N	SP_VDD	SP8_RD_N	SP8_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	12C_SA[1]	VSS	SP_VDD	SP4_RC_ N	SP4_RC_ P	SP_VDD	SP4_TC_P	SP4_TC_ N
٧	VSS	VDD_IO	VSS_IO	VSS	VSS_IO	VDD_IO	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	BCE	SP_VDD	VSS	SP4_AVD D	SP4_REX T	VSS	SP_VDD	VSS
w	VSS_IO	SP4_PWRDN	SP5_PWRDN	VDD_10	SP6_PWRDN	SP7_PWRDN	SP14_PWRD N	VSS_IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS_JO	I2C_SEL	SP_VDD	SP4_RB_P	SP4_RB_ N	SP_VDD	SP4_TB_N	SP4_TB_P
Υ	SP8_PWRDN	VDD_IO	SP9_PWRDN	SP10_PWRD N	VSS_IO	SP11_PWRD N	VDD_IO	SP15_PWRD N	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS_IO	SP_RX_SWA P	SP_TX_SWA P	VSS	SP_VDD	VSS	VSS	VSS	VSS
AA	VSS_J0	SP12_PWRD N	SP13_PWRD N	VDD_IO	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP_VDD	SP4_RA_ N	SP4_RA_P	SP_VDD	SP4_TA_P	SP4_TA_N
AB	SP4_MODES EL	VDD_10	SP6_MODES EL	SP8_MODES EL	VSS_JO	SP2_RA_N	SP_VDD	SP2_RB_P	SP2_AVDD	SP2_RC_N	SP2_AVDD	SP2_RD_P	VSS	SP10_RA_N	SP_VDD	SP10_RB_P	SP10_AVDD	SP10_RC_N	SP10_AVDD	SP10_RD_P	VSS	VSS	VSS	VSS	SP_VDD	vss
AC	VSS_J0	INT_B	SP10_MODE SEL	VDD_IO	VSS	SP2_RA_P	VSS	SP2_RB_N	SP2_REXT	SP2_RC_P	VSS	SP2_RD_N	VSS	SP10_RA_P	VSS	SP10_RB_N	SP10_REXT	SP10_RC_P	VSS	SP10_RD_N	VSS	SP_IO_SP EED[0]	SP_IO_SP EED[1]	I2C_DISABL E	VD0_10	TMS
AD	N/C	VDD_IO	SW_RST_B	N/C	VSS_IO	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS_IO	SP0_MOD ESEL	SP2_MODES EL	MCES	TDO	TDI
AE	VSS_J0	N/C	VSS	VDD_IO	SP_VDD	SP2_TA_P	VSS	SP2_TB_N	SP_VDD	SP2_TC_P	VSS	SP2_TD_N	SP_VDD	SP10_TA_P	VSS	SP10_TB_N	SP_VDD	SP10_TC_P	VSS	SP10_TD_N	VSS	I2C_MA	SP2_PWR DN	I2C_SD	VDD_IO	TRST_B
AF	P_CLK	HARD_RST_ B	SP12_MODE SEL	SP14_MODE SEL	VSS	SP2_TA_N	VSS	SP2_TB_P	VSS	SP2_TC_N	VSS	SP2_TD_P	VSS	SP10_TA_N	VSS	SP10_TB_P	VSS	SP10_TC_N	VSS	SP10_TD_P	VSS_IO	SP1_PWRDN	SP3_PWRDN	VSS_IO	I2C_SCLK	TCK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24														24	25	26										
		Legend	VSS and \	/ee IO			JTAG					Coriol D	dIO Into-f-	00.0			Coriol D	idlO loto d-	00.9							
			VSS and V			SP_VDD and SPx_AVDD					Serial RapidIO Interface 0 Serial RapidIO Interface 2						Serial RapidlO Interface 8 Serial RapidlO Interface 10									
						S_CLK_x					Serial RapidIO Interface 4						Serial RapidiO Interface 10 Serial RapidiO Interface 12									

Serial RapidIO Interface 6

Serial RapidIO Interface 14

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August 2009, 80B803A_PN003_04 -- No technical changes. Formatting was changed to reflect IDT