Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **I-0607-01** DATE: **July 21, 2006**

Product Affected: 89HPES24N3 & 89HPES12N3

Date Effective: **August 21, 2006**

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ■ Product Mark — Change in Ordering part Number
- ☐ Back Mark
- ■ Date Code
- ☐ Other

Contact: Bimla Paul
Title: Quality Assurance Manager
Phone #: (408)574-6419
Fax #: (408) 284-8362
E-mail: Bimla.Paul@idt.com

Attachment:: ■ Yes ☐ No

Samples: N/A

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other

Device stepping change from "YB" to "YC" to enhance device performance. There will be a change in ordering part number as a result of the change in device stepping.

There is no change to process and technology.

RELIABILITY/QUALIFICATION SUMMARY: See attached data. There is no change to die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: I- 0607-01

PCN Type: Die Stepping Change

Data Sheet Change Yes

Detail of Change Device stepping change from "YB" to "YC" to enhance device performance. There will be a change ordering part # as a result of the change in device stepping.

The new die revision will address the known errata items as follows:

For PES24N3 and PES12N3 "YB" Errata

1. Eliminate errata item 1: INTx messages that should be transmitted to RC may be dropped under certain conditions.
2. Eliminate errata item 4: Byte Data swapped for transparent mode MSIs
3. Eliminate errata item 7: PME enable bit in PMCSR for port A not sticky - fails compliance test
4. Eliminate errata item 9: Captured Slot Power Limit Value/Scale in incorrect endian representation.
5. Eliminate errata item 10: Legacy interrupts for hot-plug events malfunction
6. Eliminate errata item 12: Unable to change I/O Expander settings through EEPROM based initialization.
7. Eliminate VGA feature support
8. Modified revision ID

For PES24N3 and PES12N3 Data Sheet

Feature Listings (pg 1)

Remove "Supports IEEE 1149.6 JTAG"

Pin Characteristic Table (Table 6, pg. 7 of 24N3 & Table 7, pg 7 of 12N3)

For the following Serial link type I/O pins, change Buffer entry from "LVDS" to "CML"
PEARN, PEARP, PEATN, PEATP, PEBRN, PEBRP, PEBTN, PEBTP, PECRN, PECRP, PECTN, PECTP

For the following Serial link type I/O pins, change Buffer entry from "LVDS" to "LVPECL/CML"
PEREFCLKN, PEREFCLKP

These changes affect all speed grades and package options. There is no change in die technology/process.

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: I-0607-01

Detail of Change (cont'd) - Data Sheet

Power Consumption Section (pg 13., including Table 12 for 24N3)

Change From:

Typical power is measured under the following conditions: 25C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.
Maximum power is measured under the following conditions: 70C Ambient, 85% total link usage on all ports, typical voltages defined in Table 14.

Number of Connected Lanes Port-A/Port- B/ Port-C	Core 1.0 V supply		PE 1.0 V supply		PEA 1.0 V supply		TT 1.5 V supply		I/O (W) 3.3 V supply		Total (W)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
8/4/4	0.5	**0.71**	0.7	**1**	0.31	**0.39**	0.555	**0.7**	0.002	**0.01**	2.07	**2.81**
8/8/8	0.57	**0.8**	0.91	**1.33**	0.36	**0.45**	0.795	**0.91**	0.002	**0.01**	2.64	**3.50**

Change To:

Typical power is measured under the following conditions: 25C Ambient, 35% total link usage on all ports, typical voltages defined in Table 10.
Maximum power is measured under the following conditions: 70C Ambient, 85% total link usage on all ports, typical voltages defined in Table 10.
All power measurements assume that the part is mounted on a 10 layer printed circuit board, with 0 LFM airflow.

Number of Connected Lanes Port-A/Port-B/Port-C	Core 1.0 V supply		PE 1.0 V supply		PEA 1.0 V supply		TT 1.5 V supply		I/O (W) 3.3 V supply		Total (W)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
8/4/4	0.59	**0.84**	0.75	**1.08**	0.33	**0.42**	0.62	**0.78**	0.002	**0.01**	2.30	**3.12**
8/8/8	0.68	**0.95**	0.98	**1.43**	0.38	**0.48**	0.88	**1.01**	0.002	**0.01**	2.92	**3.88**

These changes affect all speed grades and package options.There is no change in die technology/ process.

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: I-0607-01

Detail of Change (cont'd) - Data Sheet

Power Consumption Section (pg 13., including Table 12 for 12N3)
Change From:

Typical power is measured under the following conditions: 25C Ambient, 35% total link usage on all ports, typical voltages defined in Table 10.
Maximum power is measured under the following conditions: 70C Ambient, 85% total link usage on all ports, typical voltages defined in Table 10.

Number of Connected Lanes Port-A/Port-B/Port-C	Core(W) 1.0 V supply		PCIe Digital(W) 1.0 V supply		PCIe Analog(W) 1.0 V supply		PCIe Termination(W) 1.5 V supply		I/O (W) 3.3 V supply		Total (W)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
1/1/1	0.36	**0.47**	0.22	**0.29**	0.17	**0.2**	0.13	**0.15**	0.002	**0.01**	0.88	**1.12**
4/1/1	0.39	**0.53**	0.38	**0.47**	0.24	**0.26**	0.255	**0.3**	0.002	**0.01**	1.27	**1.57**
4/4/4	0.45	**0.62**	0.55	**0.66**	0.27	**0.32**	0.44	**0.6**	0.002	**0.01**	1.71	**2.21**

Change To:

Typical power is measured under the following conditions: 25C Ambient, 35% total link usage on all ports, typical voltages defined in Table 10.
Maximum power is measured under the following conditions: 70C Ambient, 85% total link usage on all ports, typical voltages defined in Table 10.
All power measurements assume that the part is mounted on a 10 layer printed circuit board, with 0 LFM airflow.

Number of Connected Lanes Port-A/Port-B/Port-C	Core(W) 1.0 V supply		PCIe Digital(W) 1.0 V supply		PCIe Analog(W) 1.0 V supply		PCIe Termination(W) 1.5 V supply		I/O (W) 3.3 V supply		Total (W)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
1/1/1	0.52	**0.67**	0.27	**0.36**	0.13	**0.16**	0.11	**0.13**	0.01	**0.01**	1.04	**1.33**
4/1/1	0.56	**0.76**	0.47	**0.58**	0.19	**0.21**	0.22	**0.26**	0.01	**0.01**	1.44	**1.81**
4/4/4	0.65	**0.89**	0.68	**0.81**	0.21	**0.25**	0.38	**0.51**	0.01	**0.01**	1.92	**2.47**

On Part Ordering Information Page (for both 24N3 and 12N3)

add "YC" to part order number

Change From	Change To
89HPES24N3BX	89HPES24N3YCBX
89HPES24N3BXG	89HPES24N3YCBXG
89HPES12N3BC	89HPES12N3YCBC
89HPES12N3BCG	89HPES12N3YCBCG

These changes affect all speed grades and package options.There is no change in die technology/ process.

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: I-0607-01

Qualification Data

Test Vehicle: IDT89HPES24N3

Qualification Test Plan and Results:

Test Description	Sample Size/# Of Fails	Test Results (SS/# Of Fails
Dynamic High Temp Operating Life Test	77/0	77/0
* Temperature Cycling (-65 °C to 150 °C, 500 cycle)	45/0	**45/0
* Highly Accelerated Stress Test (HAST) (130 °C,85% RH, 100 Hrs)	45/0	**45/0
ESD HBM	3/0	**3/0
ESD CDM	3/0	**3/0

Notes: * Test requires Moisture Pre-Conditioning sequence.
** Test results from previous revison of device qualification