Product Change Notice (PCN)

Subject: Electrical Specification Change to Standard Microcircuit Drawing 5962-12228 for Intersil Products ISL70417SEH*
Publication Date: 1/7/2016
Effective Date: 4/7/2016

Revision Description:
Initial Release

Description of Change:
This notice is to inform you of changes to the electrical specifications in DLA (Defense Logistics Agency) SMD (Standard Microcircuit Drawing) 5962-12228 for the listed ISL70417SEH* products. The offset voltage, input bias current, and input offset current limits have been changed as shown in Appendix B.

Reason for Change:
The change aligns the SMD with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following page. The updated SMD is available on the DLA web site at: http://www.landandmaritime.dla.mil/Programs/Smcr/

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Qualification status: Complete, see attached
Sample availability: 1/7/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Appendix A – Affected Products List (see attached)
Appendix B – SMD changes (see attached)

Appendix A – Affected Products List

Standard microcircuit drawing	Intersil Part Number	Standard microcircuit drawing	Intersil Part Number
	ISL70417SEHF/PROTO	5962F1222801V9A	ISL70417SEHVX
5962F1222801VXC	ISL70417SEHVF		ISL70417SEHX/SAMPLE

Appendix B – SMD changes

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C ±V_S = ±15 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Offset voltage	VOS		1	1	01		~~75~~ 85	µV
				2,3			110	
			M,D,P,L,R,F	1			110	
Offset voltage drift	TCVOS	3/		2,3	01		1	µV/°C
Input bias current	IIB		1	1	01	~~-1~~ -2.5	~~+1~~ +2.5	nA
				2,3		-5	+5	
			M,D,P,L,R,F	1		~~-5~~ -15	~~+5~~ +15	
Input bias current temperature coefficient	TCIIB	3/		2,3	01	-5	+5	pA/°C
Input offset current	IOS		1	1	01	~~-1.5~~ -2.5	~~+1.5~~ 2.5	nA
				2,3		-3	3	
			M,D,P,L,R,F	1		~~-3~~ -10	~~+3~~ 10	
Input offset current temperature coefficient	TCIOS	3/		2,3	01	-3	+3	pA/°C

3/ Guaranteed but not tested. The limits are characterized at initial qualification and after any design or process changes which may affect the product characteristics but are not production tested.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C ±V_S = ±5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	VOS		1	01		150	µV
			2,3			250	
		M,D,P,L,R,F	1			250	
Offset voltage drift	TCVOS	3/	2,3	01		1	µV/°C
Input bias current	IIB		1	01	~~±1~~ -2.5	~~±1~~ +2.5	nA
			2,3		-5	+5	
		M,D,P,L,R,F	1		~~±5~~ -15	~~±5~~ +15	
Input bias current temperature coefficient	TCIIB	3/	2,3	01	-5	+5	pA/°C
Input offset current	IOS		1	01	~~±1.5~~ -2.5	~~±1.5~~ 2.5	nA
			2,3		-3	3	
		M,D,P,L,R,F	1		~~±3~~ -10	~~±3~~ 10	
Input offset current temperature coefficient	TCIOS	3/	2,3	01	-3	+3	pA/°C

3/ Guaranteed but not tested. The limits are characterized at initial qualification and after any design or process changes which may affect the product characteristics but are not production tested.