Product Change Notice (PCN)

Subject: Data Sheet Specification Change for Listed Intersil ISL8200M* Products
Publication Date: 6/10/2015
Effective Date: 9/10/2015

Revision Description:
Initial Release

Description of Change:
This notice is to inform you that Intersil has changed the recommended operating conditions (Vin, PVCC and Vcc), PVCC Voltage Level and Enable Sink Current/Impedance.

Reason for Change:
The change aligns the data sheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following page. The updated data sheet is available on the Intersil web site at:

http://www.intersil.com/content/dam/intersil/documents/isl8/isl8200m.pdf

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Qualification status: Complete, see attached
Sample availability: 6/10/2015
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Appendix A – Affected Products List (see attached)
Appendix B – Datasheet changes (see attached)

Appendix A – Affected Products List
ISL8200MIRZ   ISL8200MIRZS2751   ISL8200MIRZ-T   ISL8200MIRZ-TS2751

Appendix B – Datasheet changes
Recommended Operating Conditions
From:

Absolute Maximum Ratings

Input Voltage, PVIN, V_{IN} . . . . -0.3V to +27V
Driver Bias Voltage, PVCC . . . . -0.3V to +6.5V
Signal Bias Voltage, V_{CC} . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT} . . . . -0.3V to +36V
Phase Voltage, V_{PHASE} . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage,
   V_{BOOT} - V_{PHASE} . . . .-0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . .-0.3V to V_{CC} + 0.3V
ESD Rating
   Human Body Model (Tested per JESD22-A114E) 2kV
   Machine Model (Tested per JESD22-A115-A) 200V
   Charge Device Model (Tested per JESD22-C101C) 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . 100mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W) θ_{JC} (°C/W)
   QFN Package (Notes 4, 5)   13   2.0
Maximum Storage Temperature Range . . . -40°C to +150°C
Pb-free reflow profile . . . . .see link below
   http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Voltage, PVIN, V_{IN} .3V to 20V
Driver Bias Voltage, PVCC . . . . .3V to 5.6V
Signal Bias Voltage, V_{CC} . . . . 3V to 5.6V
Boot to Phase Voltage (Overcharged),
   V_{BOOT} - V_{PHASE} · <6V
Commercial Ambient Temperature Range. . . . . 0°C to +70°C
Industrial Ambient Temperature Range . . . . -40°C to +85°C
Junction Temperature Range . . . . -40°C to +125°C

To:

Absolute Maximum Ratings

Input Voltage, PVIN, V_{IN} . . . .-0.3V to +27V
Driver Bias Voltage, PVCC . . . . -0.3V to +6.5V
Signal Bias Voltage, V_{CC} . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT} . . . .-0.3V to +36V
Phase Voltage, V_{PHASE} . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage,
   V_{BOOT} - V_{PHASE} · -0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
   Human Body Model (Tested per JESD22-A114E). 2kV
   Machine Model (Tested per JESD22-A115-A). 200V
   Charge Device Model (Tested per JESD22-C101C). 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W) θ_{JC} (°C/W)
   QFN Package (Notes 4, 5)   13   2.0
Maximum Storage Temperature Range . . . .-40°C to +150°C
Pb-Free Reflow Profile . . . . see Figure 40

Recommended Operating Conditions

Input Voltage, V_{IN} . . . . 4.5V to 20V
Input Voltage, PVIN. . . . . 3V to 20V
Driver Bias Voltage, PVCC . . . . 4.5V to 5.6V
Signal Bias Voltage, V_{CC} . . . . 4.5V to 5.6V
Boot to Phase Voltage
   V_{BOOT} - V_{PHASE} · <6V
Industrial Ambient Temperature Range . . . . -40°C to +85°C
Junction Temperature Range . . . .-40°C to +125°C

Internal Linear Regulator

From:

INTERNAL LINEAR REGULATOR						
Maximum Current	I_{PVCC}	PVCC = 4V TO 5.6V			250		mA
		PVCC = 3V TO 4V			150		mA
Saturated Equivalent Impedance	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)			1		Ω
PVCC Voltage Level (Note 7)	PVCC	I_{PVCC} = 0mA to 250mA	5.1	5.4	5.6	V

To:

INTERNAL LINEAR REGULATOR						
Maximum Current	I_{PVCC}	PVCC = 4V			320		mA
Saturated Equivalent Impedance	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)			1		Ω
PVCC Voltage Level (Note 7)	PVCC	I_{PVCC} = 0mA, V_{IN} = 12V	5.15	5.4	5.95	V

Enable Hysteresis Sink Current

From:

ENABLE (Note 7)						
Maximum Input Voltage	V_{EN}		**VCC**			V
Turn-On Threshold Voltage			**0.75**	0.8	**0.86**	V
Hysteresis Sink Current	I_{EN_HYS}		25	30	35	µA
Undervoltage Lockout Hysteresis	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.5		V
Sink Current	I_{EN_SINK}				15	mA
Sink Impedance	R_{EN_SINK}	I_{EN_SINK} = 5mA			65	Ω

To:

ENABLE (Note 7)						
Turn-On Threshold Voltage			0.75	0.8	0.86	V
Hysteresis Sink Current	I_{EN_HYS}		23	30	35	µA
Undervoltage Lockout Hysteresis	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.6		V
Sink Current	I_{EN_SINK}	V_{EN} = 1V	15.4			mA
Sink Impedance	R_{EN_SINK}	V_{EN} = 1V			64	Ω